

THE USE OF MOSFETS IN HIGH-DOSE-RATE RADIATION ENVIRONMENTS

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ABSTRACT

In military switching applications, the power MOSFET has become the device of choice. Military applications require survival, if not operation, during the prompt gamma pulse resulting from a nuclear explosion. This paper discusses the behavior of MOSFETs in high-dose-rate radiation environments, relating the performance to the device's structure. This understanding is used as a starting point for improving system performance by optimizing both device and circuit parameters.

INTRODUCTION

Power electronic circuits are widely used in military equipment which must survive the prompt gamma pulse from a nuclear weapon detonation. This pulse is characterized by short duration (20 to 50 ns) and a high rate of change (10^{12} to 10^{15} rads/s). The total pulse dose is typically low, under a few hundred rads.

Due to the widespread use of power MOSFETs in military equipment, their response to the prompt pulse is a matter of concern. A MOSFET that is biased off, will turn-on and conduct if the radiation dose rate is sufficiently high. This behavior is similar to that of other semiconductor devices. If uncontrolled currents are allowed to flow, it is possible to destroy the device so the equipment no longer functions. From a design point of view, such a scenario is unacceptable.

Three general approaches may be used to prevent failure. First, reduce the radiation level through the use of shielding. While this solution is often used, it can be heavy, expensive, and mechanically awkward. The second solution is to redesign the MOSFETs to be "radiation hardened." To meet this requirement, power MOS transistors must be capable of surviving the inrush of current that occurs following a prompt pulse. To absorb this energy, a unique set of terminal and internal conditions are required. The third solution is to design the circuit such that the devices are not overstressed by the circuit itself during and after a prompt pulse.

During the past two years, significant advances have been made towards hardening power MOSFETs as the understanding of the device physics of power MOSFETs in a radiation environment has improved. This paper examines one possible mechanism leading to power MOSFET failure following a prompt pulse. This mechanism, turn-on of the intrinsic bipolar transistor, is discussed in detail and a model for device failure is proposed. Based on this model, several methods for hardening power MOSFETs to prevent prompt-pulse failures are covered. Following this discussion, the interaction between a MOSFET and the applicable circuit is

examined. A clear understanding of this interaction is essential to the design of systems capable of surviving and operating in a prompt-pulse environment.

The Power MOSFET: A Bipolar Transistor in Masquerade

The introduction and subsequent acceptance of power MOSFETs was based, in part, on their advantages over bipolar transistors. In addition to higher input impedance and higher frequency operation, their ruggedness and lack of secondary breakdown allow power MOSFETs to be used in applications where bipolar transistors are not acceptable.

Examining the cross section of a conventional vertical DMOS transistor shown in Figure 1a, reveals that the structure includes a bipolar transistor with an emitter-to-base short. Figure 1b. shows the equivalent circuit of this power MOSFET.

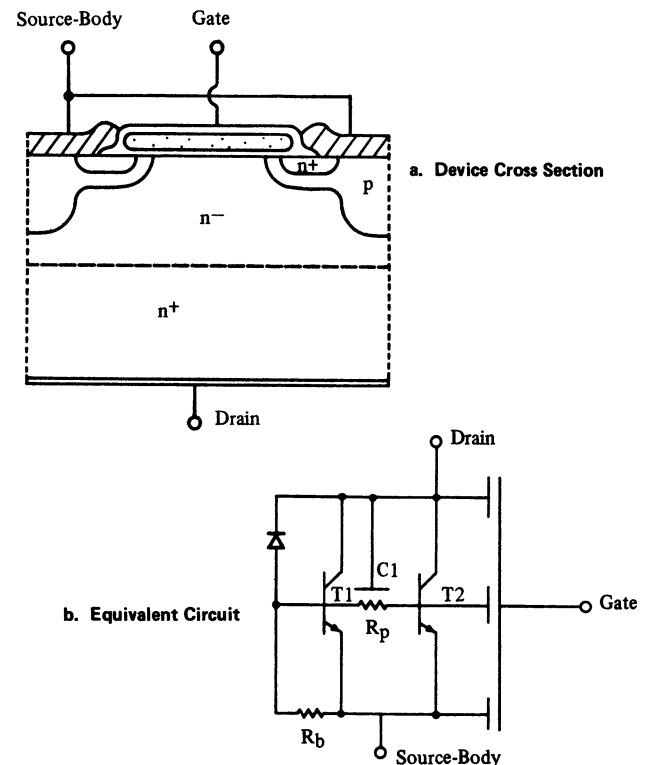


Figure 1. Cross Section of A Power MOSFET and Its Equivalent Circuit

In this figure, the distributed nature of the bipolar transistor is emphasized. The pinched resistor formed by the body region beneath the source and between the channel region and the source-body contact is labeled R_p . The resistance between the body contact and the pinched body region is labeled R_b . In normal operation, the metallization at the source-body contact prevents the intrinsic bipolar transistor from becoming active.

Early power MOSFETs occasionally failed during rapid voltage increases on the drain terminal. These failure were understood when the effect of the body-drain capacitance (labeled C_1 in Figure 1b.) became understood. As the dV/dt on the drain terminal increased, the displacement current associated with this capacitance increased [$I = C(dV/dt)$]. If the displacement current produced a voltage drop in excess of 0.6 V across the pinched resistor R_p , transistors T_1 and T_2 at the extremes of the distributed NPN structure became decoupled, the the breakdown voltage that T_2 can sustain decreases from its BV_{CES} to its BV_{CEO} , as shown in Figure 2. This trigger current, called I_T in Figure 2, allows transistor T_2 to become active. Figure 2 shows the decrease in sustaining voltage that occurs when T_2 becomes active. (The BV_{CES} of transistor T_2 equals the BV_{DSS} of the power MOSFET.)

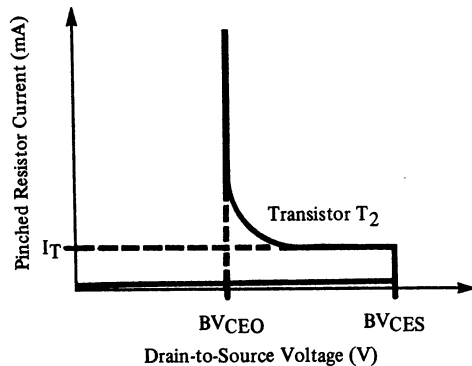


Figure 2. Latchback Phenomenon Observed in Power MOSFET Structures When Transistor T_2 Turn On

This model, first developed to understand the breakdown and transient behavior of power MOS devices, also sheds light on their performance in ionizing radiation. A prompt pulse creates hole-electron pairs throughout the device. A fraction of the carriers are collected along the distributed body-drain junction, forming one side of resistor R_p . If these carriers produce a voltage drop greater than 0.6 V as they flow laterally through the resistor, the intrinsic bipolar transistor becomes active. The sustaining voltage of the MOSFET drops rapidly, and the presence of an active bipolar transistor may lead to secondary breakdown.

Based on the device structure, this physical behavior is plausible; but experimental results are necessary to gain further insight into device behavior. Therefore, a test device was designed to determine both the bipolar and the power MOS characteristics of the four-terminal structure. The data from measurements made on devices with BV_{DSS} values ranging from 100 V to 500 V is contained in Table 1. Of particular interest is the significant difference in sustaining voltage (greater than a factor of two) between the test structure measured as a bipolar and as a power MOSFET. This difference significantly decreases device operating

voltage if determined by the characteristics of the intrinsic bipolar transistor.

Table 1. Four-Terminal MOSPOWER Transistor Data

Voltage Rating	VNDE10 100 V	VNDH20 200 V	VNDH40 400 V	VNDH50 500 V
Gain at 10 mA	40	30	30	40
BV_{CEO}	57 V	104 V	225 V	225 V
BV_{CES}	135 V	225 V	480 V	540 V
BV_{DSS}	135 V	225 V	480 V	540 V
V_T @ 1 mA	4.2 V	3.8 V	4.3 V	4.5 V

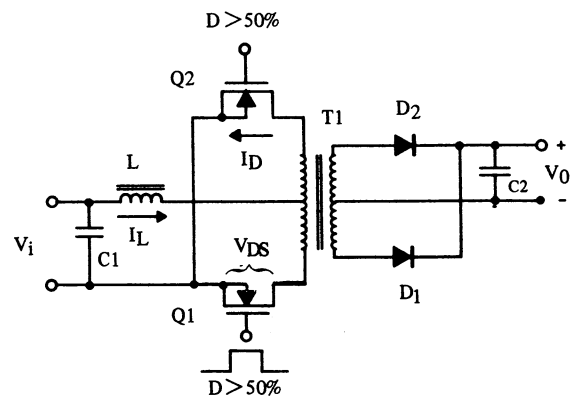
The device cross section and accompanying circuit model shown in Figure 1 are used as a starting point for developing power MOSFETs capable of withstanding large prompt pulses. Approaches that promise to increase the ruggedness include:

1. decreasing the carrier lifetime in the device bulk so fewer carriers are collected in the pinched resistor R_p
2. decreasing the value of the pinched resistor R_p
3. decreasing the current gain of the intrinsic bipolar transistor

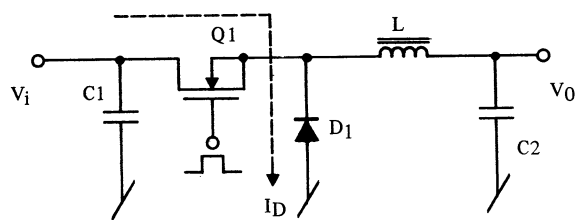
Work in these areas has produced power MOSFETs capable of surviving prompt pulses that are 10 to 100 times greater than those previously available.

Turn-On from A Circuit Point of View

Broadly speaking, power circuits will fall into two categories: those with series drain impedance sufficiently large to limit the drain current (I_D) and reduce the drain source voltage (V_{DS}), and those with insufficient drain impedance to limit I_D and/or V_{DS} . Figure 3 shows an example of each type.



3(a). A Type of Boost Converter

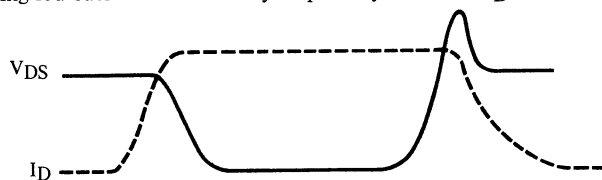


3 (b). A Buck Converter

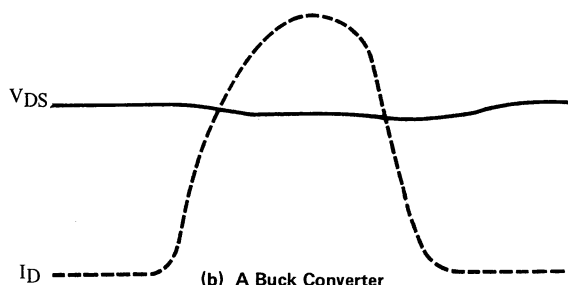
Figure 3. Typical Power Circuits

When the boost converter of Figure 3 (a) is irradiated, Q_1 , Q_2 , D_1 , and D_2 conduct and the inductor current (I_L) is divided between Q_1 and Q_2 . For the short time (0.5 to $2 \mu s$) it takes for Q_1 and Q_2 to recover, I_D is limited by L and does not rise appreciably.

Representative voltage and current waveforms during a transient event are shown in Figure 4 (a). Capacitor C_2 discharges through D_1 and D_2 , and if the currents are reasonably balanced, the transformer is essentially short circuited with little current being fed back from secondary to primary to add to I_D .



(a) A Boost Converter



(b) A Buck Converter

Figure 4. Switching Waveforms During A Prompt Pulse

Under irradiation, the buck converter of Figure 3(b) reacts somewhat differently. Both Q_1 and D_1 conduct simultaneously while connected in series across C_1 . The conduction impedance of Q_1 and D_1 determines the amplitude of I_D and the distribution of voltage drop across Q_1 and D_1 . In a real circuit, C_1 is quite large, typically 5 to $150 \mu F$. If the radiation level is not high enough for C_1 to self-discharge internally (this is often the case), I_D may not be large enough to discharge C_1 significantly in 0.5 to $2 \mu s$, and the voltage across C_1 remains close to V_i . The switching waveform in Figure 4(b) results when a worse case is assumed ($V_{DS} = V_i$). This waveform is much more severe when a higher current pulse and a large V_{DS} value occur simultaneously.

The radiation induced turn-on of the internal BJT is similar to normal switching in a power circuit. With care, the concepts

of Forward Bias Safe Operating Area (FBSOA) can be applied. The analogy can be carried further by including snubber circuits which would be used for a BJT but not necessarily with a MOSFET. Although not perfectly correct, this analogy is close enough to allow the use of circuit protection, load line shaping, etc. to protect the device as in a normal BJT switch.

Figure 5 shows a typical $1\text{-}\mu s$ FBSOA curve for the parasitic BJT with the two switching waveforms shown as load lines. The V_{DS} boundary is the BV_{CEO} rating for the internal BJT, *not* the BV_{DSS} rating for the MOSFET. As shown earlier, BV_{CEO} can be less than $BV_{DSS}/2$ in a normal FET and can be higher in a hardened device.

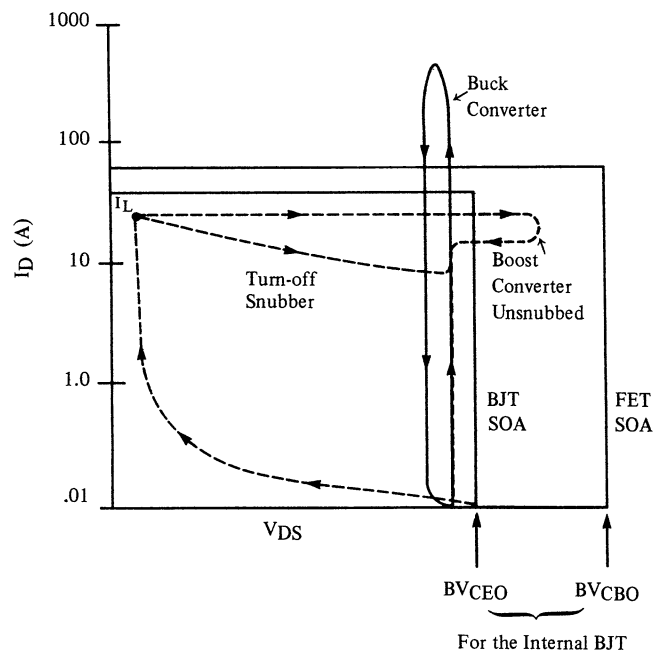


Figure 5. Parasitic BJT, $1\text{-}\mu s$ pulse, Forward Bias Safe Operating Area

When normal MOSFETs are used, the exact values for BV_{CEO} are not often known, even by the manufacturer. Without this information, it is wise to use a device with a BV_{DSS} value that is twice the anticipated peak voltage. When 100-V devices are needed, it is possible to use 200-V devices, but if the circuit needs a 500-V device, doubling the voltage rating may not be possible. Increasing BV_{DSS} also increases $r_{DS(on)}$, so it may be necessary to use a larger device to keep $r_{DS(on)}$ low. Radiation hardening is particularly helpful in the high-voltage devices.

In the boost converter, turn-off after a prompt pulse is not very different from normal BJT operation. During normal operation, a voltage spike may occur which must be snubbed or otherwise limited to a voltage less than BV_{DSS} . This degree of control *may* not be adequate for turn-off from a prompt pulse where the BV_{CEO} rating applies. This problem can be overcome by using a conventional turn-off snubber, such as the one shown in Figure 6 (a). However, the snubber must be designed to meet the requirements of BV_{CEO} rather than BV_{DSS} . The design procedure should be essentially the same as for normal BJT switching.

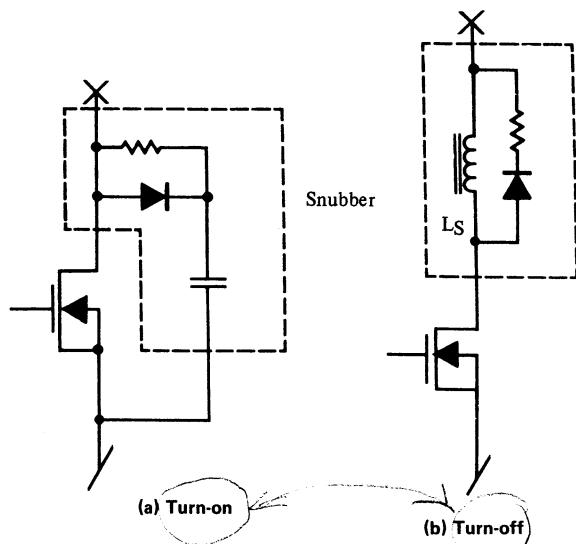


Figure 6. Typical Snubber Circuits

The buck converter switching conditions can be much worse. If the BJT is turned on while V_{DS} remains high, large currents can flow, resulting in almost astronomical peak powers. The peak power need not be extremely high to destroy the device when it is functioning as a BJT rather than as a FET. Actual pulse waveforms for an IRF250, in a buck converter, with a pulse of 2×10^{10} rads/s are shown in Figure 7.

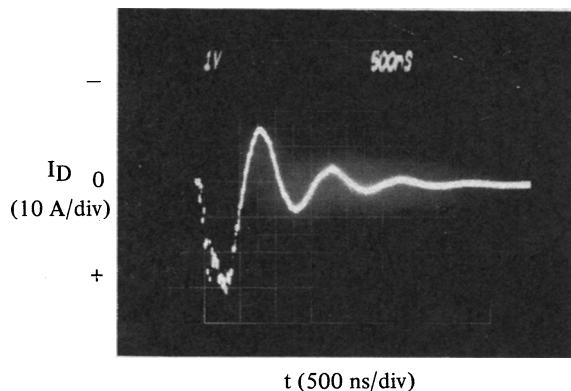


Figure 7. Typical Current Pulse in A Buck Converter for An IRF250, $V = 10$ A/div, $V_{DS} = 30$ V, pulse = 2×10^{10} rads/s for 28 ns (Note current sense is inverted with the positive I_D downward. Ringing is due to circuit parasitic inductance.)

This radiation rate is relatively low and V_{DS} is low, so pictures may be taken without destroying the device. As large as the pulse is, it would be much higher at 10^{12} to 10^{15} rads/s with a higher drain-source voltage (especially $V_{DS} > 100$ V). This observation underscores the severity of the stress for operation under these conditions. Several things can be done to improve the survivability.

1. Use a hardened device which has the smallest possible peak current and a rapid recovery time. For presently envisioned devices, it is necessary to take additional measures above 10^{12} to 10^{13} rads/s.
2. A turn-on snubber, such as the one shown in Figure 6(a), can be used to limit the peak current and to reduce V_{DS} . This idea sounds good, but there is a problem. The MOSFET would normally turn on in 20 to 50 ns in a switching application. The snubber action, however, needs to be effective for 0.5 to 2 μ s. If the snubber inductor (L_S) is sufficiently large to protect the device, it may also be large enough to interfere with normal switching action. The effectiveness of a turn-on snubber depends on the device chosen and its recovery time. For normal FETs, the recovery time may be as long as 5 μ s and the snubber might not work at all. For a fast recovery FET, such as a FRED-FET (Siemens) which uses heavy metal doping as a lifetime killer, the snubber may be very effective.

The usefulness of a turn-on snubber with a hardened device depends on specific device characteristics. As noted earlier, there are several options for hardening a MOSFET. One is to include lifetime killers which greatly reduce the recovery time and make a snubber more effective.

3. When a prompt pulse occurs, the FET channel can be deliberately turned on to divert the current away from the BJT. This concept is shown in Figure 8. For short periods of time (0 to 5 μ s), the MOSFET is capable of passing large pulse

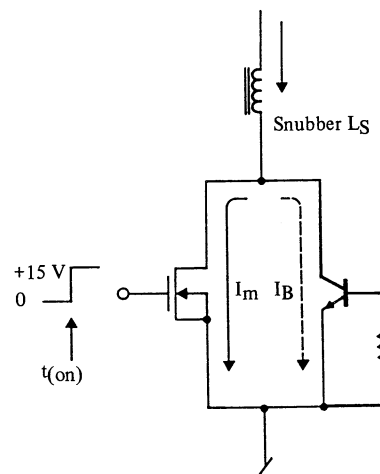


Figure 8. Turn-on of the MOSFET Channel to Divert Current Away from the Parasitic BJT.

NOTE: In Figure 8, a snubber inductor is used to reduce V_{DS} . If there is no drain impedance and the sources are stiff, turning on the FET channel might not change I_B . It is assumed that L_S is relatively small so the current rises to a high value – hopefully through the FET and not the BJT. It is necessary to have a turn-off snubber to absorb the voltage spike created by L_S .

currents safely. To minimize the impedance of the MOSFET, a fairly large gate drive of 15 to 18 V should be used. Any current diverted away from the BJT increases the survival level. Tests run to verify this concept showed that the device survives at a dose level 10 times higher than without MOSFET turn-on. If the recovery time of the BJT is known, it appears reasonable to keep the FET on until the BJT has recovered. (The authors are not aware of any definitive tests on the maximum time FET should be left in the on state.)

4. Another possible energy diversion scheme is shown in Figure 9. The SCR, which is readily triggered by radiation, diverts the energy effectively. However, turning off the SCR may be a problem. If the circuit lends itself to commutation or another means of current flow interruption, an SCR can be effective.

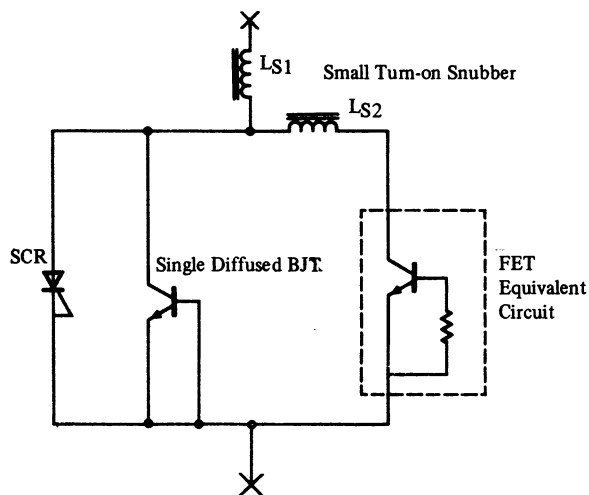


Figure 9. Energy Diversion Methods

A few single-diffused BJTs are still available. While not noted for their switching speeds, these devices are extremely rugged with a good FBSOA. For a given time (5 to 10 μ s), they will reset themselves, circumventing the problem of SCR commutation. However, with this approach, the shunt or "crowbar" switch may not turn on as rapidly as the FET BJT. A small turn-on snubber can be used, as shown in Figure 9, to divert the current. To be effective, the shunt device should be large compared to the protected device(s).

5. One of the most effective means for device protection is to minimize the available stored energy and to limit the I_D rise rate. The circuit in Figure 9 illustrates current limitation using a large inductor. In the buck converter, it is important to minimize the size of C_1 . This requirement may increase the ripple voltage at the input, but the input filter inductor can be increased to compensate. High-frequency operation in converters can also be used to reduce the capacitor sizes.

6. For the buck converter and similar circuits, I_D is strongly affected by the reaction of D_1 to the radiation. If the impedance of D_1 is kept high compared to the MOSFET, then the peak current will be reduced and the voltage across the FET reduced. D_1 should be as hard as possible and should be selected with the protection of Q_1 in mind.
7. Finally, it is possible to use local shielding to reduce the exposure level to the point where survival is guaranteed. For buck converters, shielding the diode alone may be advantageous. If the diode impedance remains high, a large current pulse will not occur. In some cases, shielding only the diode may save weight.

Some Thoughts On Test Circuits

A great deal of flash x-ray testing has been done on MOSFETs, sometimes with contradictory results. The test circuit used can have a profound effect on the failure level of the device. In some cases, one device may appear better than another in a given test circuit, but the results may be reversed if the circuit is changed. Also, some test circuits expose devices to current and voltage stress levels that would not be present in the actual circuit, making the test data difficult to relate to reality. From a designer's point of view, the only useful test circuit closely replicates the actual layout and component values being used.

CONCLUSIONS

While present MOSFETs are affected by the prompt gamma pulse, progress has been made in the design of more reliable radiation-resistant devices for military applications. An understanding of the device physics during a prompt pulse has already produced power MOSFETs capable of surviving radiation levels 10 to 100 times greater than before. These new power MOSFETs, along with circuit circumvention techniques and modest shielding, should be available in the near future for use in the most demanding environments.