

dV_{DS}/dt Turn-on In MOSFETs

Rudy Severns
April 1984

INTRODUCTION

Under certain conditions, when a rapidly rising voltage waveform is applied from drain to source of a supposed "off" MOSFET, the device will turn-on. dV/dt turn-on is well known in SCRs and bipolar junction transistors (BJTs). This phenomena in MOSFETs is similar in many respects except that dV/dt turn-on occurs at much higher rates than it does in either SCRs or BJTs. Because spurious turn-on can be destructive, it is of serious concern in those applications where it might occur.

Several different modes of dV_{DS}/dt turn-on have been identified, and in most cases, turn-on may be eliminated or the effect of turn-on may be reduced to an acceptable level.

To eliminate this problem, the mechanisms of the turn-on modes, the consequences of spurious turn-on, the means for reducing or eliminating turn-on, and the applications where turn-on is likely to be a problem, must be understood. The following discussion intends to provide the basic information on dV_{DS}/dt turn-on needed by the design engineer.

Equivalent Circuit Model

Figure 1 is an equivalent circuit model for a power MOSFET which includes the parasitic elements within the device and within the drive circuit (R_D , L_D , V_d).

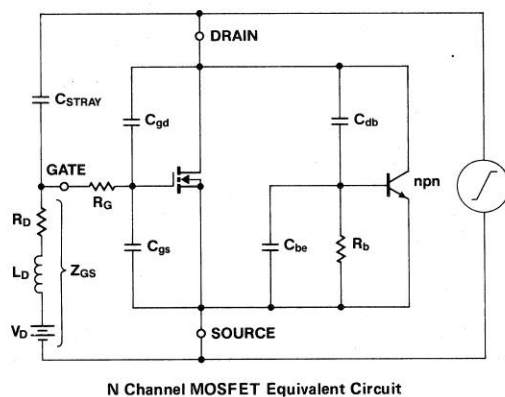


Figure 1

The parasitic NPN BJT, an integral part of the device structure, is present in all VMOS and DMOS devices. To minimize the effect of the BJT, R_b is made as small as possible, and H_{FE} is low. None the less, in some circumstances the BJT can be turned on.

The impedance of the drive circuit (Z_{gs}) may take many forms, but the series R , L , battery is representative. R_D comes from several sources: resistance deliberately placed in series to limit the peak current or reduce the rise time of V_{gs} , bypass capacitor ESR, wiring resistance, the on resistance of drive switches, etc. L_D is due to the physical size and layout of the drive circuit. If a transformer is used for drive isolation, the primary-to-secondary leakage inductance will add to L_D . When series diodes or BJTs are used in the drive circuit, an equivalent series battery (V_D) is present. In some cases, a DC bias may be present, so V_D could be either positive or negative. C_{stray} represents the parasitic capacitance from drain to gate due to the circuit layout. This capacitance may be as large or larger than the intrinsic C_{gd} if careful layout is not used.

R_G is the internal gate resistance. The value of this resistance varies from 0.05 to 5.0Ω depending on the manufacturer and the size of the device. Siliconix devices typically run from 0.5 to 4.0Ω .

The intraterminal capacitances of a MOSFET are functions of V_{DS} as shown in Figure 2*. Because C_{gd} and C_{ds} are functions of V_{DS} , spurious turn-on will depend on both dV_{DS}/dt and V_{DS} , which complicates the analysis. In the following discussion, the body-drain diode will be mentioned. This diode is the base-collector junction of the parasitic BJT.

* NOTE: Because $C_{be} \gg C_{db}$, $C_{db} \sim C_{ds}$

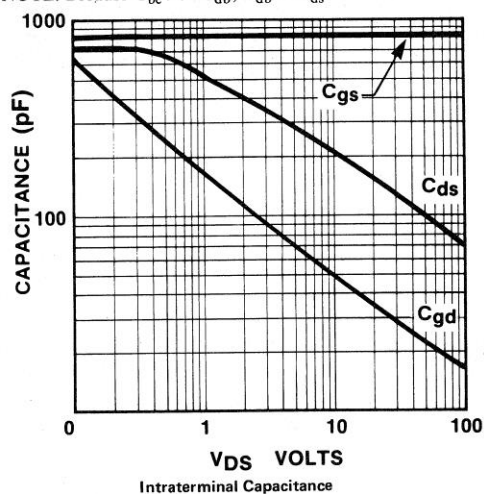


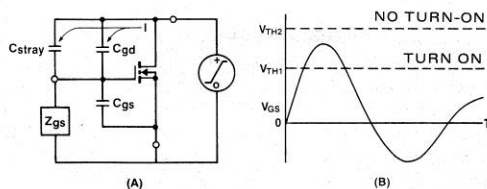
Figure 2

The following modes of dV_{DS}/dt turn-on have been observed:

1. Device quiescent: Z_{gs} high, MOSFET turns on.
2. Device quiescent: Z_{gs} low, BJT turns on.
3. Body-drain diode conducting: Z_{gs} low, BJT turns on.
4. Body-drain diode conducting: Z_{gs} low, BJT goes into avalanche breakdown.

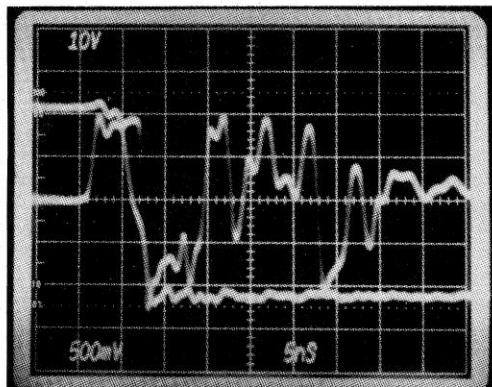
MODE 1 TURN-ON

The equivalent circuit for mode 1 turn-on is given in Figure 3 along with a generalized waveform for V_{gs} . The exact nature of the V_{gs} waveform will be a function of Z_{gs} and C_{stray} , but in general, the lower the impedance presented by Z_{gs} and the lower the value for C_{stray} , the lower the peak value of V_{gs} . If V_{gs} exceeds V_{th} , the device will turn on. In most applications, the amplitude of I_D , during turn-on will be limited by $R_{DS(on)}$. This mode of turn-on is not usually destructive, although it will increase the power losses. Figures 4 and 5 show actual turn-on waveforms when Z_{gs} is resistive.



Mode 1 Equivalent Circuit

Figure 3



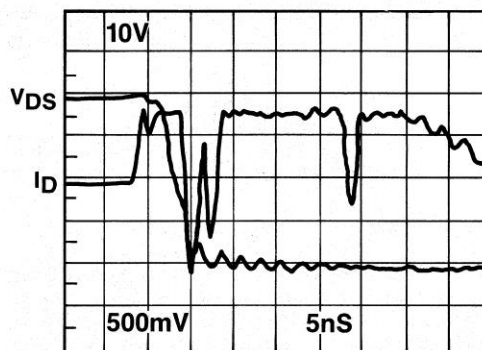
Mode 1 Spurious MOSFET Turn-On $R_g = 10 \text{ OHMS}$

Figure 4

Even when the FET is not turned on, a pulse of drain current will be present due to the intraterminal capacitances. An idealized waveform for this case is shown in Figure 6A, and a more realistic waveform is shown in Figure 6B. There will always be some series inductance which, when combined with the nonlinear capacitances, produces a distorted, damped sinusoid.

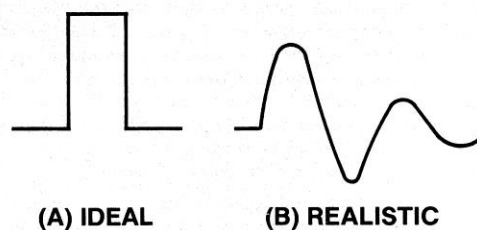
This current pulse will be reflected into the switch which is generating the positive dV_{DS}/dt .

One additional complication to mode 1 turn-on has been suggested but not observed. If the FET is turned on, it is possible for parasitic oscillations to occur. This would raise V_{gs} and increase the power dissipation. It is possible for the gate to be ruptured if V_{gs} becomes large; however, if oscillation is not present during normal switching, it is unlikely that it will occur during mode 1 turn-on.



Mode 1 Spurious MOSFET Turn-On $R_g = 50 \text{ OHMS}$

Figure 5



Pulse Drain Current Waveforms

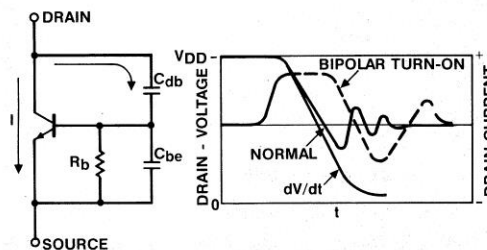
Figure 6

The best way to detect potential mode 1 turn-on is to observe the gate-to-source voltage waveform with an oscilloscope. If a significant voltage spike appears during the drain voltage transition then some positive action will have to be taken to reduce the pulse amplitude.

MODE 2 TURN-ON

The equivalent circuit for mode 2 turn-on is given in Figure 7, along with V_{DS} and I_D waveforms. The mechanism for this mode of turn-on is quite simple. As V_{DS} slews, current will flow through C_{db} . If enough current flows so that the voltage across R_b exceeds $\sim 0.65V$, some of the current will flow into the base, turning on the BJT. In contrast to mode 1, the acceptable dV_{DS}/dt rate is only a function of the device design, not of the external circuit elements.

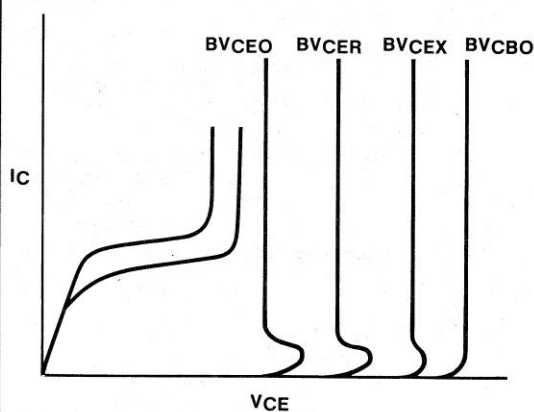
The result of Mode 2 turn-on can be harmless or catastrophic depending on V_{DS} and the magnitude of the base current.



Mode 2 Turn-On Equivalent Circuit and Typical Waveform

Figure 7

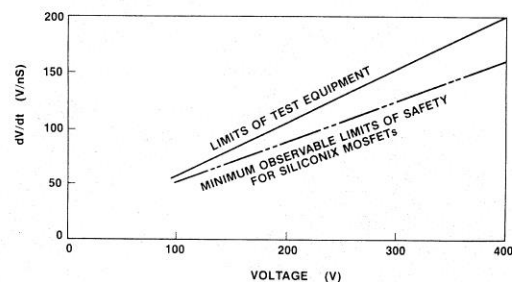
In a BJT, the collector-emitter breakdown voltage is a function of base-emitter impedance and of the current flowing in the device. This point is illustrated in Figure 8. For low values of R_b and zero base current injection, BV_{DSS} is equal to BV_{CEX} for the BJT. This is the data sheet voltage rating for the device. Once base current is injected, however, the breakdown voltage drops dramatically to a level $< BV_{CEO}$, which may be as low as $\frac{1}{2} BV_{CEX}$. If V_{DS} is $> BV_{CEO}$ and base current is injected, the device will go into avalanche breakdown. Furthermore, if I_D is not limited by the external circuit, the device can go into secondary breakdown and will be destroyed.



Breakdown in a BJT

Figure 8

So much for the bad news. Now for the good news. In modern MOSFETs, the dV_{DS}/dt rate at which mode 2 turn-on can be initiated is generally very much higher than most applications will ever see. The dV_{DS}/dt limits for Siliconix devices are shown in Figure 9. Realize that the rates shown correspond to transition times of one to three nsec. Very few applications require transitions this rapid. Even testing at these rates is a formidable problem.

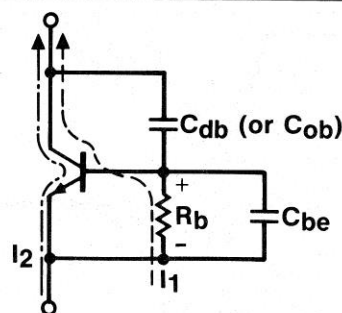


dV_{DS}/dt Limits in Power MOSFET

Figure 9

MODE 3 AND MODE 4 TURN-ON

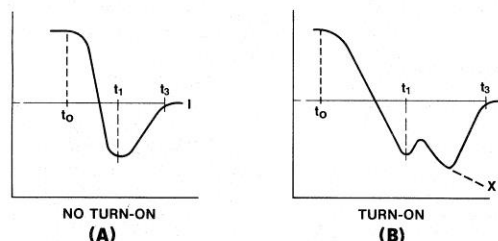
Frequently the body-drain diode is used as a catch diode for an inductive load. In a few applications, such as sinewave synthesis or some motor control schemes, the positive dV_{DS}/dt is applied while the diode is conducting. Figure 10 shows the equivalent circuit for this condition. Just prior to the application the voltage ramp, I_R is flowing through the BJT in a reverse direction. Much of the current will flow through R_b and the collector-base diode. Even in the inverted mode, however, the BJT will have some current gain, and



Mode 3 Equivalent Circuit

Figure 10

a portion of I_R will flow in reverse through the emitter, as indicated. As a result of this current flow, the device is saturated with charge, i.e., it is hard on at the moment the dV_{DS}/dt is applied. Typical voltage and current waveforms for mode 3 operation, with and without turn-on, are shown in Figure 11. Figure 11A shows the waveforms for the case where the BJT does *not* turn-on and thus acts like a normal P-N junction diode. Looking at the waveforms, the sequence is initiated by a switch closure at $t = t_0$. The current through the diode begins to reverse at a rate (dI/dt) which is determined by the switch transition time and/or the circuit series inductance. If the switch transition is very rapid, the circuit inductance will dominate; conversely, if the transition is slow, the switch dominates. During the interval t_0-t_1 , V_{DS} changes only slightly (-1 to $+1$ volt). V_{DS} does not change significantly until I_D reaches its maximum value and begins to fall. At $t = t_1$, V_{DS} begins rising rapidly. The rate of dV_{DS}/dt at this point is determined by the circuit series inductance, the peak current *and* the recovery characteristic of the diode. The recovery characteristic is in turn a



Mode 3 Waveforms

Figure 11

function of the initial dI/dt . This relationship is illustrated by Figure 12. The more rapid dI/dt , the greater will be the peak amplitude of I_D , Q_{rr} will be larger and t_{rr} shorter. More important, the dI_D/dt during the interval t_1-t_3 becomes greater as the initial dI/dt is increased. In some diodes, dI_D/dt can increase dramatically and can form a sharp step or snap as indicated in Figure 13. At lower levels of initial dI_D/dt , the step may not be present, but as the initial dI_D/dt is increased, the step appears. This current step during recovery can generate extremely high rates of dV/dt in the circuit.

A further complication exists: the diode recovery characteristics are also influenced by the magnitude of I_D during reverse conduction. This relationship is shown qualitatively in Figure 14.

Figure 11B shows the waveforms when turn-on is present. Two cases are shown: recovery without damage and catastrophic

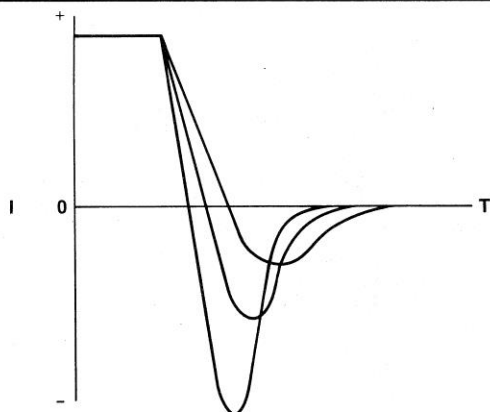
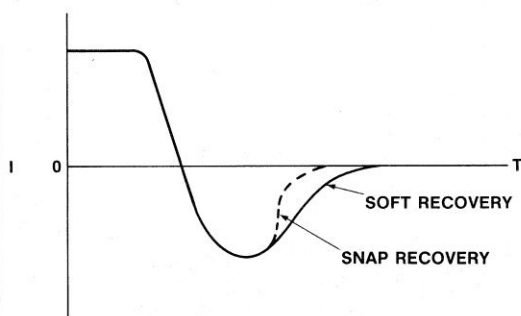
Variations in T_{rr} and Q_{rr} with di/dt

Figure 12



Soft Versus Snap Diode Recovery Waveform

Figure 13

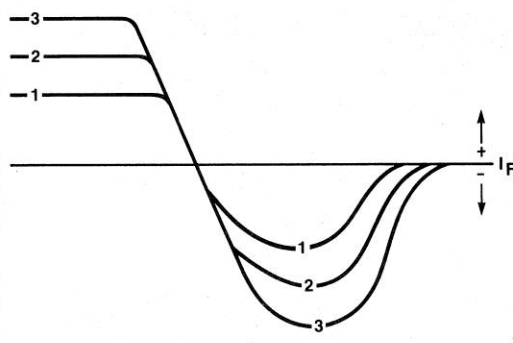
Variation in T_{rr} with I_F

Figure 14

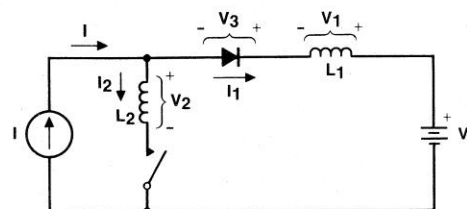
failure. Notice that the BJT turn-on occurs during the interval t_1 - t_3 and is triggered by the dV_{DS}/dt resulting from the recovery characteristic of the diode. The dV_{DS}/dt during the interval t_1 - t_3 is related to the switch transition time, but it is *not* a direct function. This is very different from modes 1 and 2 where the current waveforms are coincident with and directly proportional to the transition time.

Mode 3 turn-on is an indirect function of transition time and is more directly controlled by the circuit and the recovery character-

istic of the device. In terms of rating the device for dV_{DS}/dt capability, the appropriate voltage transition is not the switch transition but rather the transition which appears across the diode during the second portion of the recovery interval.

This complex interaction deserves a more detailed examination. The following discussion uses a successive approximation to explain what happens during mode 3 operation.

An equivalent circuit for mode 3, where turn-on does not occur and the device can be viewed as a diode, is given in Figure 15. Note that the inductive load current is assumed to be constant during the recovery interval and is represented by a current source. L_1 and L_2 are the circuit parasitic inductances.



$$I = I_1 + I_2$$

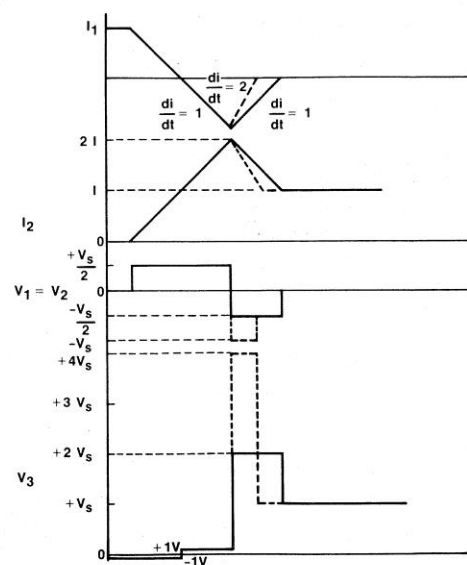
$$V_s = V_1 + V_2 + V_4$$

$$\text{If } L_1 = L_2, \frac{dI_1}{dt} = \frac{dI_2}{dt} \Rightarrow V_1 = V_2$$

Mode 3 Equivalent Circuit

Figure 15

The reverse recovery current waveform (I_1) can be approximated by triangular waveforms as shown in Figure 16. From this approximation, the voltage (V_3) across the diode is easily determined, as shown. The critical point in the waveform is the rapid and large positive transition which occurs when the waveform



Triangular Waveform Approximation

Figure 16

di/dt reverses. The amplitude of the transition is a function of di/dt during recovery—a diode characteristic. A diode with a snap characteristic would generate a very rapid, high amplitude voltage spike.

Figure 16 indicates an infinite dV_{DS}/dt , which is not what is observed. A better approximation would be to use a trapezoidal waveform as indicated in Figure 17. Figure 17 also shows the actual waveforms. From this figure, we see that the large voltage transient still exists. Its amplitude is essentially the same, but the dV_{DS}/dt is finite. We can see that the reverse recovery characteristic of the diode determines both dV_{DS}/dt and the amplitude of the transients.

The device could respond to the voltage transient in several ways:

1. If the amplitude is small and dV_{DS}/dt moderate, the device recovers normally.
2. Mode 3 turn-on could occur without avalanche breakdown.
3. Mode 4 turn-on could occur; i.e. the device avalanches before the BJT turns on.
4. Mode 3 turn-on could occur, lowering BV_{DSS} , leading to avalanche breakdown and perhaps second breakdown.

Each of these turn-on scenarios is potentially destructive.

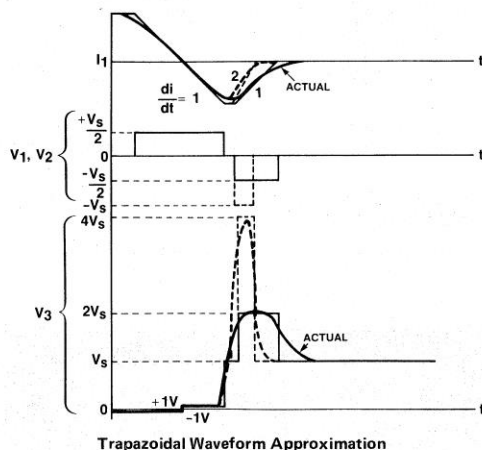
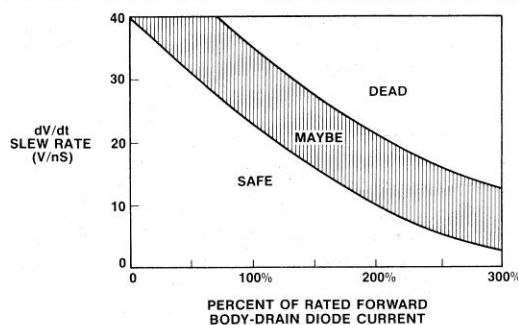


Figure 17

The complexity of the interaction between the parameters makes it difficult to characterize FETs for mode 3 and 4. Figure 18 displays the results of preliminary testing of Siliconix devices. Competitive devices were also tested and found to be no better at best, and much worse in some cases. While this curve is hardly definitive, it does show that modes 3 and 4 turn-on levels are an order of magnitude lower than mode 2. The dI/dt levels used in the testing were in the range of 150 A/usec. This is representative for motor control or low frequency AC synthesizer; however, LF transmitters and sonar transducer drivers would be expected to have much higher dI/dt rates which would further reduce the acceptable dV/dt .

Fortunately, mode 3 operation is restricted to a few special applications such as:

1. Motor drives and sinewave inverters where multiple repetitive pulsing of the switches occurs.
2. Highly reactive resonant loads, such as found in LF transmitters, sonar transducer drivers, and induction heating equipment.
3. Synchronous rectifiers where the body-drain diode is allowed to conduct.



Mode 3 Performance

Figure 18

The Effect of Radiation and T_j on dV_{DS}/dt

The effects of T_j and radiation on dV_{DS}/dt behavior have not been discussed. While little testing has been done, trends can be identified. V_{th} has a negative temperature coefficient of four to eight mV/°C, so that at high temperatures V_{th} is lower. This will lower the rate at which mode 1 turn-on occurs. At higher temperatures, V_{be} will decrease in the BJT, and the gain will increase. Both of these effects will reduce the acceptable dV_{DS}/dt rate for modes 2 and 3.

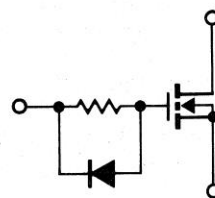
Ionizing radiation has two effects for total doses above 10KRad(Si). First V_{th} is reduced, and second the gain and diode recovery time of the BJT are reduced. This implies that mode 1 performance is degraded, but modes 2 and 3 should be improved.

How To Avoid dV_{DS}/dt Problems

In most circuits, dV_{DS}/dt turn-on may be avoided. There are many ways to accomplish this:

1. Reduce dV_{DS}/dt
2. Low impedance drive circuits
3. Good circuit layout practice
4. Negative gate bias
5. Series drain diode
6. Snubbers
7. Turn-on of the FET during commutation
8. Use MOSFETs with good dV/dt performance
9. Current fed topologies

The most obvious way to reduce dV/dt problems is to slow the switching speed. This can be accomplished easily by adding resistance in the gate as shown in Figure 19. The diode is added to provide a low impedance when the device is off so that mode 1 problems do not arise.

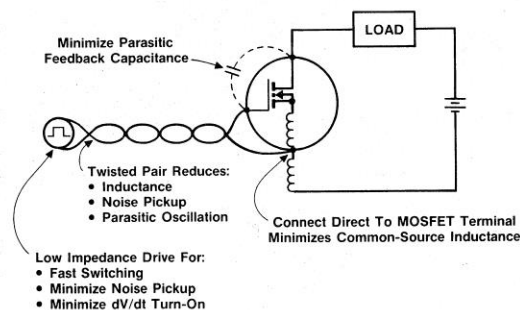


dV/dt Slowdown Circuit

Figure 19

The best means to avoid mode 1 turn-on is to use a low impedance driver and good circuit layout. Figure 20 illustrates how to design a good drive circuit. It is also very helpful to reduce the noise and ringing in the overall circuit.

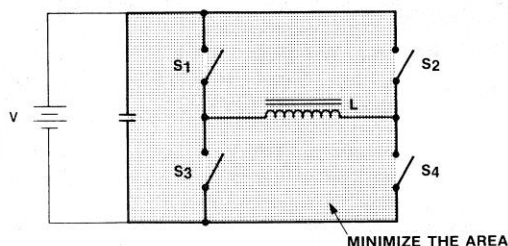
In very noisy environments, it may be necessary for V_{gs} to be negative during the switch off interval. The noise coupled to the gate will have to overcome a potential of $V_{th} + V_{bias}$.



Circuit Layout to Reduce Mode 1 Turn-On

Figure 20

Figure 21 shows how to lay out an H-Bridge switch-mode power converter primary to minimize noise, ringing, and coupling from one point of the circuit to another. The principle is quite simple; first identify those paths in the circuit where the switched currents are flowing and then minimize the inductance and radiating area of these current loops. These techniques will not only reduce dV_{DS}/dt turn-on but will be beneficial in reducing EMI, eliminating voltage spikes and generally cleaning up the circuit waveforms.



High di/dt Paths

Figure 21A

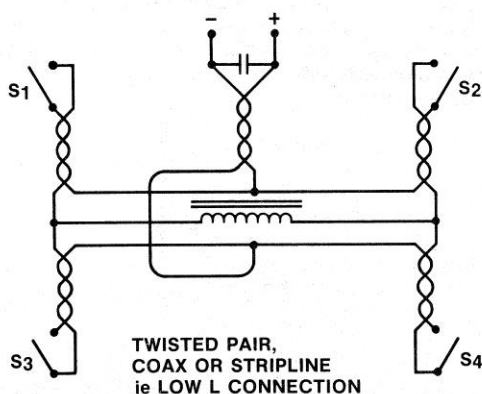


Figure 21B

Mode 3 performance may be improved by reducing or eliminating the current in the body-drain diode. Two ways to do this are shown in Figure 22. In (A) the FET channel is turned on to divert current away from the body diode. This can be very effective as shown in Figure 23. Figure 23 is a superposition of the FET and diode conduction characteristics in a VNE003A. In this particular device, the diode would not start conducting until $I_D > 30$ Amps.

Another method which eliminates diode conduction entirely is shown in (B). A low voltage diode is placed in series with either the drain or source, and a normal diode is added in parallel to carry the commutation current. This approach will eliminate mode 3 turn-on, but there is a penalty in the power cost in the series diode and in the extra cost of the external diodes.

In extreme cases, snubbers may be used to reduce the dV_{DS}/dt , the transient amplitude and to limit current pulses if turn-on should occur.

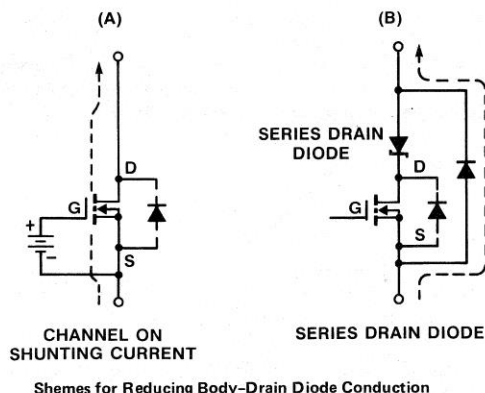
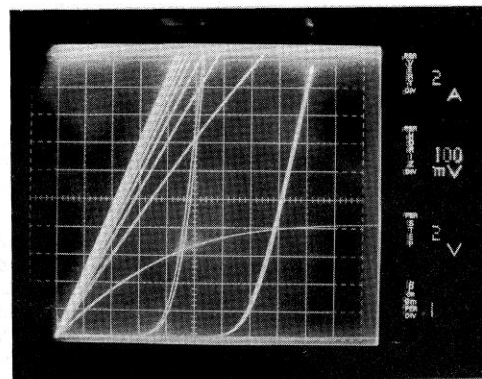


Figure 22

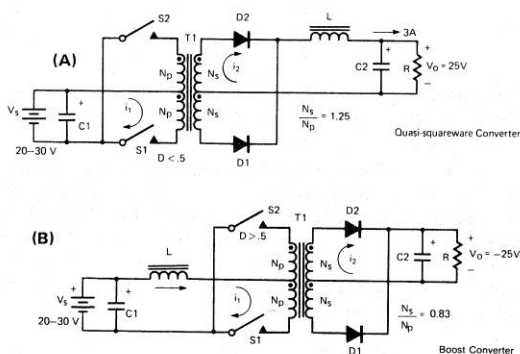


Body Diode/Forward Conduction Comparison

Figure 23

The effect of dV/dt turn-on will depend on the impedance of the circuit in which the device is being used. For example, the circuit shown in Figure 24A is a voltage fed switch-mode power converter. When S1 is closed, a positive dV_{DS}/dt will appear across S2. If S2 is turned on then a short circuit will appear across the transformer winding. There is little to limit the current because the source impedance is very low. Given the same circumstances in

Figure 24B, the series inductor will limit the rate of current rise. The probability of damaging the switches will be reduced.



Voltage and Current Fed Converters

Figure 24

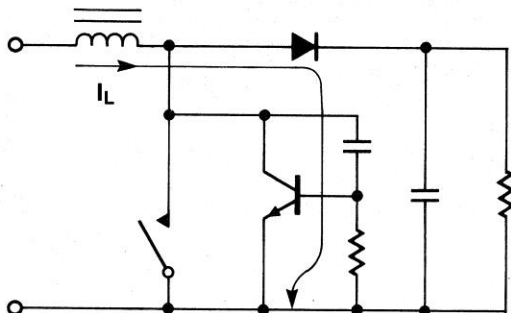
CONCLUSIONS

dV_{DS}/dt turn-on does exist in power MOSFETs, so the following conclusions may be drawn:

1. Mode 1 is primarily a circuit problem which can best be eliminated by using low impedance drives and good circuit layout techniques.
2. Mode 2 occurs only for very high values of dV_{DS}/dt ; therefore, this is seldom a problem.
3. Modes 3 and 4 are potentially the most troublesome but occur only in specialized applications. Modes 3 and 4 may be reduced or eliminated with circuit modifications.

APPENDIX

Another scenario for mode 2 turn-on has been postulated but not observed. Figure 25 shows a simplified boost converter where the MOSFET is represented by a perfect switch in parallel with the intrinsic BJT. When the switch is opened, some of the inductor current (I_L) will flow into C_{db} . If I_L is large enough, it is conceivable that the BJT could be turned on. The effect on the turn-off waveform would be similar to storage time in a BJT, i.e. extended turn-off time.



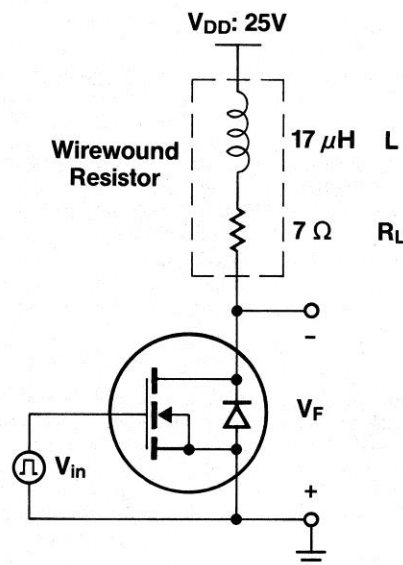
Postulated Mode 2 Turn-On Mechanism

Figure 25

Conceivably, several turn-off pulses could occur as the BJT turns on stealing base current. Like all mode 2 turn-on, this effect will only be possible for very rapid transitions.

A mode of anomalous turn-off ringing has been identified by Giadomenico (6). This ringing could easily be mistaken for the mode turn-on just discussed or for parasitic oscillation. The ringing occurs when there is excessive unclamped drain inductive and is described by Giadomenico, et al, as follows:

"When the power MOSFET inverter circuit shown in Figure 26 is suddenly turned off, the drain voltage rises quickly and then abruptly drops to the "on-voltage" where it remains for several microseconds before ringing and settling to the supply voltage (see Figure 27A). This behavior was initially thought to be due to dV/dt breakdown and was thought to be related to the "on-state" oscillations. However, this turn-off behavior is in fact due to the clamping diode between the drain and source which is intrinsically incorporated into the vertical MOSFET structure. A typical display of the drain voltage and current during turn-off is shown in Figure 27B from which the turn-off phenomenon can be explained.



The Power MOSFET Connected in an Inverting Configuration

Figure 26

When the device is turned off, the magnetic energy stored in the load inductance is transferred into the output capacitance and then returned to the inductor with the opposite current polarity. Neglecting the non-linearity of the output capacitance and the damping of the output load resistance, the time for the current reversal is:

$$t = \pi \sqrt{LC} \quad (1)$$

After this time, the parasitic diode is forward biased, and the voltage across the inductor is:

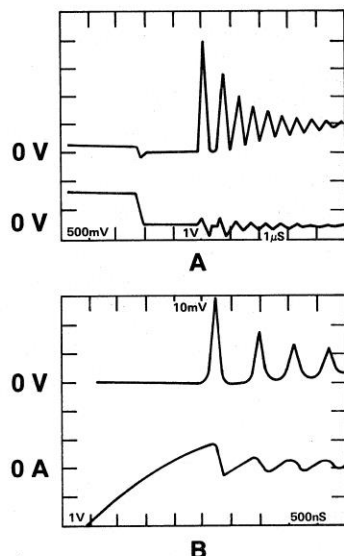
$$V_L = V_{DD} + V_F - I_D R_L \quad (2)$$

where V_F is the forward diode voltage. If the damping losses are neglected, then:

$$I_D \approx -V_{DD}/R_L \quad (3)$$

and

$$V_L \approx 2V_{DD} + V_F \quad (4)$$



Oscilloscope of the Turn-Off Behavior of the Power MOSFET Inverter. a) Upper Trace: $V_D=10V/Div$; Lower Trace: $V_{GS}=5V/Div$. b) Upper Trace: $V_D=10V/Div$; Lower Trace: $I_D=0.2A/Div$.

Figure 27

The drain voltage remains near zero during the time the diode is conducting. The current through the diode is dictated by the L-R circuit and is:

$$I_D = \frac{2V_{DD} + V_F}{R_L} \left(1 - e^{-t R_L/L} \right) - \frac{V_{DD}}{R_L} \quad (5)$$

Neglecting reverse recovery, the time at which the diode current is zero is:

$$t_{on} = \left(\frac{L}{R_L} \right) \ln \left[\frac{2V_{DD} + V_F}{V_{DD} + V_F} \right] \quad (6)$$

For a reasonably large supply voltage, $V_{dd} \gg 0.7$ volts, the above equation can be expanded in a Taylor series to give:

$$t_{on} = \left(\frac{L}{R_L} \right) \left[1 - \frac{V_F}{2V_{DD}} \right] \ln 2 \quad (7)$$

Neglecting the reverse recovery of the diode for the moment, the drain voltage rises at this time and then rings and settles to the supply voltage.

A comparison of experimental data with the calculated results of eq. (7) reveals a large discrepancy in the "on-time." Further, the oscillographs of Figure 27 show that the power MOSFET appears to turn on a third time. These discrepancies are due to the reverse recovery of the diode (see Figure 27B). Consequently, the total turn-on time expressed by equation (7) must be modified to include the reverse recovery time, t_{rr} :

$$t_{on} \approx \frac{L}{R_L} \left[1 - \frac{V_F}{2V_{DD}} \right] \ln 2 + t_{rr} \quad (8)$$

Since, after the diode's reverse recovery, the inductor once again has a downward current direction, the situation is the same as when the MOSFET first turned off but with a lower initial current level, and thus the cycle repeats again."

BIBLIOGRAPHY

1. J. Redonfey, "The dV/dt Phenomenon in Power Transistors," The power transistor in its environment, Thompson-CSF, Semiconductor Division, Applications book, 1978.
2. J. Rockot, "Reverse Transistor Action In Transistor Inverters," Westinghouse Power Semiconductor Division, Tech Tip, pp. 1-13.
3. R. Severns, "dV/dt Effects in MOSFET and Bipolar Junction Transistor Switches," Proceedings of the IEEE Power Electronics Specialists Conference, June 1981, Boulder CO.
4. D. Kuo, C. Hu & M. Chi, "dV/dt Breakdown in Power MOSFETs," IEEE Electron Device Letters, Volume EDL-4, No. 1, January 1983.
5. W. Slusark et al., "Catastrophic Burnout in Power VDMOS Field-Effect Transistors," Proceedings of the 21st annual IEEE, Reliability and Physics Symposium, 1983, pp. 173-177.
6. D. Giadomenico, et al., "Analysis and Prevention of Anomalous Oscillations and Turn-off Behavior in a Vertical Power MOSFET," private report done for Siliconix inc., later published in the proceedings of POWERCON 11, April 1984, Dallas.

Siliconix 2201 Laurelwood Road, Santa Clara, CA 95054

(408) 988-8000

TWX: 910-338-0227

The information contained in this data sheet is current at the time of publication. Siliconix incorporated reserves the right to make changes in the circuitry or specifications at any time without notice, henceforth, assumes no responsibility for the use of any circuits described herein and make no representations that they are free from patent infringement.

Readers are cautioned to verify currency of information in this publication prior to placing orders.

Printed in U.S.A.