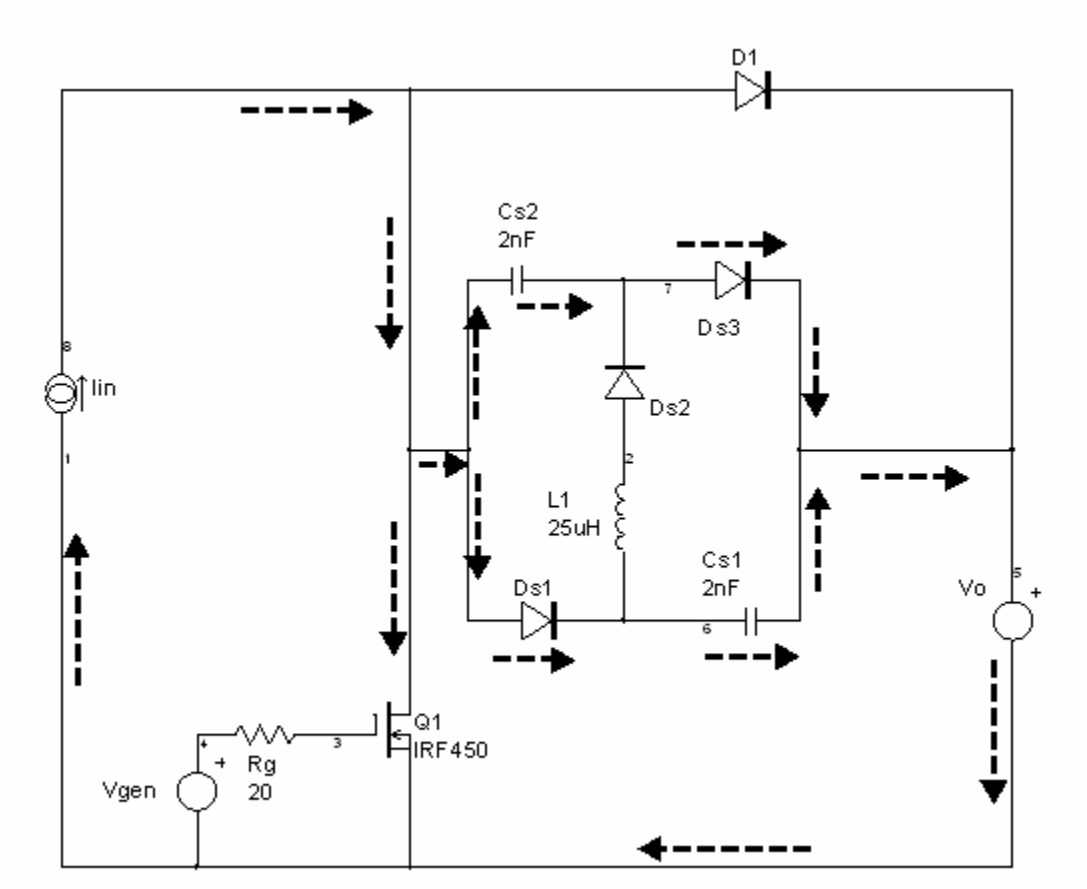
Snubber Circuits For Power Electronics

Rudy Severns



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A note from the author.

Preparing a book like this takes well over 1000 hours of effort and a substantial investment by the author and publisher. Hopefully, this book will prove to be a useful contribution to the power electronics art. When such books are successful and provide some reasonable return to their authors, there is motivation to write more such books on other important subjects. The result is of benefit to all in our profession. Honesty is a fundamental requirement for any professional engineer and is expected of those in the profession or training for it. Your help is requested in not making copies of this work and distributing it to others or in accepting any such copy.

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Preface

Switches play a major role in efficient power conversion and have a long history of use beginning with mechanical switches in the 1840's, vacuum and gas discharge devices during the first 60 years of the 20th century, through to today's wide variety of semiconductor devices. While switching device technology has changed dramatically over time, the need to use some form of auxiliary circuit to reduce switch stress and/or losses has been constant. In fact some of these auxiliary circuits, which are often referred to as "snubbers" or "switching aids", are the same today as they were in the 1850's, using the same components, in the same way, for the same reasons. Of course there have also been many new ideas as switch technology has evolved. Despite this long history, new and useful snubber variations still continue to appear. We still haven't invented everything when it comes to snubbers.

With so much activity over such a long period of time it's not surprising that there is a very extensive body of technical literature and patents on snubbers. As part of this book I have included an extensive bibliography (with over 500 entries!) but that's just a sample of the literature on the subject. Surprisingly, it does not appear that anyone has written a book on snubbers although there have been multi-page applications notes[388,441]. Although most power electronics texts at least touch on the subject of snubbers, for the most part we still have to search through the literature to get detailed information on snubbers and their applications. This lack of a text which provides information on the design of snubbers and points the way to the wider literature is my motivation for creating this book. In the process I learned a very great deal which I wish I had known much earlier.

There is no pretence that this book is a complete source even though the subject is discussed at book length. Because of the breadth of the subject and the incredible variety of snubber circuits, all I've been able to do in the space available is to illustrate basic principles,

describe the operation of typical examples, point out the similarities between many apparently different snubbers and give design guidance for some typical snubber circuits. To make the text more readable and accessible, I have elected to devote very little space to detailed analytic derivations of the equations describing circuit waveforms and operation. The literature is rich with such expositions and where appropriate I identify relevant references. This should allow the reader to gain a basic understanding of the operation of a particular snubber from the text and then proceed to related literature for more detailed information.

Besides space, there are other reasons for limiting the analytic discussion. As indicated in chapter 2, even for as simple a snubber as the RC-damping network, the analysis quickly becomes very complicated, especially when real circuit details, such as multiple distributed parasitics and the actual behavior of semiconductor devices during switching are included. From the point of view of designing and applying snubbers in the laboratory, often in some haste, it is much faster to use approximate expressions which will get you close to a solution and then adjust component values to optimize performance. I must admit that for years I have railed against this kind of cut-and-try design process in power electronics. In the case of snubbers however, I've had to admit that in the usual pressure-cooker environment where a problem is discovered during development and a quick fix is needed, this approximate approach works very well. More detailed analysis for the final product can (and should!) be done later. The literature is full of such analysis, particularly in papers with academic origins.

But when the pressure is on, even the relatively simple discussions of circuit operation which constitute most of this book, may be too involved. You may only want to know the time of day, not how to design the watch! To meet this need I have included a separate chapter entitled "Bare Bones Snubber Design". In that chapter I give only "do this, use this rule of thumb, etc" instructions with no justification. The idea is to use this information for a quick fix so you can get on with the project at hand. If you want to know more, that's what the rest of the book is for.

Throughout the text I have used SPICE modeling (Ispice by Intusoft) to explain and illustrate snubber operation. Circuit simulation has the advantage that you can idealize or simplify the circuit initially to demonstrate basic principles but then add more realistic components to better approximate the real world as your understanding increases. Fortunately, modern SPICE software does a very good job of simulating switch and snubber behavior. Of course simulation is never perfect, the actual circuit will always be somewhat different. But if you're careful to include reasonable values for parasitic elements, a design which looks good in simulation will usually work in the real circuit but will no doubt require some fine tuning to optimize. Fortunately many different free versions of SPICE are readily available to us. For the most part, even the student editions of these programs is perfectly adequate for snubber design. High priced, full featured versions are very nice when available but are not necessary.

One frustration for me has been what I've had to leave out. In particular I have not addressed the subject of "soft switching" in any detail. This is currently a subject of great interest and new developments but there is enough information on the subject that it deserves a volume of it's own. There is in fact no sharp distinction between snubbers and soft switching. Although they are not usually advertised as such, many "snubbers" are in fact a means to switch a device more "softly" and the transition from snubbers to soft-switching circuits is a gradual one. Many "soft-switching" circuits use principles common in snubbers with additional modification of the overall circuit added.

Chapter 1 gives an overview of snubbers, the variety of names for the same circuit, some terminology and a description of the many different uses for snubbers, along with an historical example dating from 1853.

A major theme of this book is how apparently different snubber circuits have common underlying principles. The differences are often superficial. That theme begins in chapter 2 and is continued throughout the book.

Chapter 2 is intended to show how switches behave and how they are used. There are many good texts[297] which go into the details of

semiconductor device operation, so that subject is treated very lightly. Instead, chapter 2 emphasizes the similarities between different devices and how they are used in switching power conversion, motor controls, etc. It also serves to introduce some additional terminology and operating modes which are to a large extent independent of the particular switching device employed. There is a discussion of parasitic elements (L and C) which are normal parts of any practical circuit and their effect on circuit behavior. This along with the discussion of switching different types of loads illustrates the motivation for using snubbers.

In chapter 3 we finally get down to talking about snubbers with the introduction of RC-damping networks. In chapter 4 diodes are added to the R, L and C components used in chapter 3 to create new families of snubbers with different properties. The snubbers in chapters 3 and 4 are dissipative in nature. While they may reduce dissipation in the switch, that energy is usually dissipated in the resistive part of the snubber instead.

In chapter 5 components are added to recover the energy which was dissipated in the snubbers of chapters 3 and 4 and put that energy to a useful purpose. This can result in a substantial improvement in overall circuit efficiency although there are practical limits which are also pointed out. The necessity of using RC-damping networks with most energy recovery snubbers is explained.

Chapter 6 treats the mundane but very important subjects of component selection, circuit layout and measurements. Chapter 7 is titled "Bare Bones Snubber Design". This chapter is strictly a cookbook with no justification for the instructions given. Justification is given at length in earlier chapters. It is intended for emergency use in the lab.

At the end of this book is a bibliography of books, technical articles and patents related to snubbers. Despite taking up more than 40 pages and over 500 entries, there is no pretence that this is a complete listing but it should be a reasonable sample of the literature over many years and provide an entrée to further research.

Rudy Severns, Cottage Grove, Oregon, April 2008

Acknowledgement

This book has been a lot of fun to write with not too much pain but it would never have been done if Jerry Foutz hadn't nagged and encouraged me to do it. His unfailing support and very considerable efforts both as a reviewer and developing the means to disseminate the book were vital to the project. Without him, no book would have appeared, no matter how long I talked about it!

My special thanks to Pat Hamel for reviewing the book and finding many errors, some very egregious! I corrected these very quickly.

I also have to express my love and appreciation to my wife, Diana for her patience during the hundreds of hours it took to write this book. A whole lot of "honey do's" were seriously delayed which of course are now being carefully attended to.

Chapter 1

An Overview Of Snubbers

Seldom can we clearly identify the originator of circuit ideas in widespread use over a long period of time. The capacitive turn-off snubber would surely seem to fall into that category but that turns out not to be the case. We know exactly where this snubber first appeared, at least in the literature.

One of the key electrical discoveries of the 19th century was Faraday's invention of the induction coil which was immediately adopted by experimenters to investigate electrical phenomena.

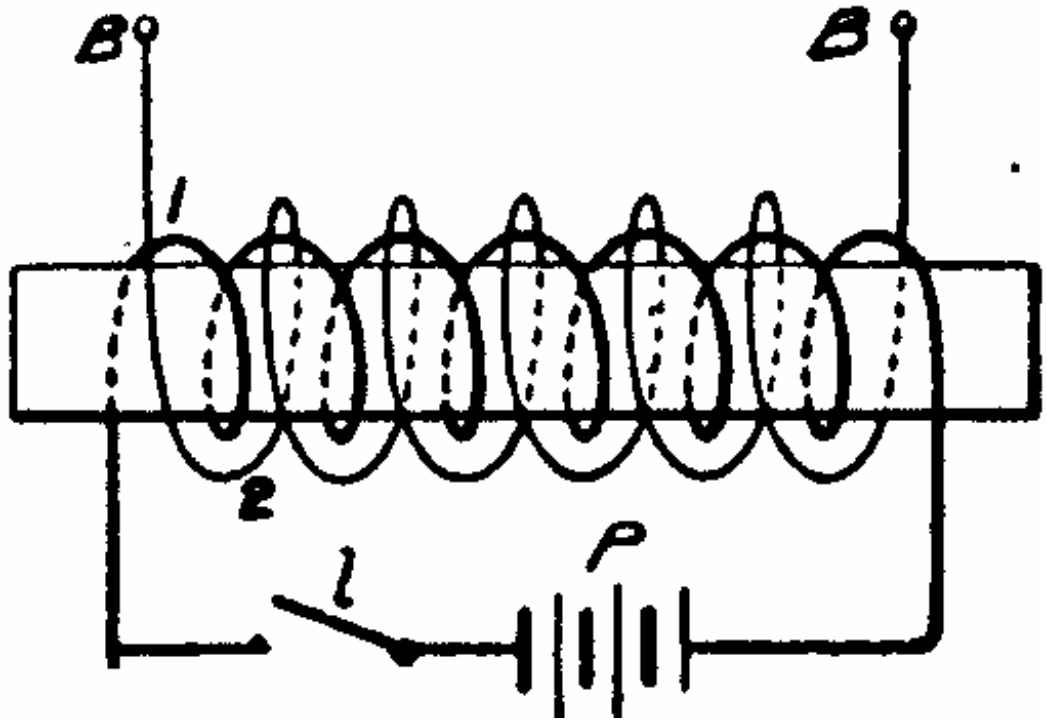


Figure 1-1, equivalent circuit for an induction coil.

Figure 1-1 shows an equivalent circuit diagram. The idea was to create a spark across the secondary terminals when the primary switch was opened. When operating from a DC source it was recognized that nothing interesting happened until the switch in series

with the primary winding was closed for a period of time to store some energy in the inductance and then opened quickly. Early on it was realized that it was very helpful if the primary circuit could be opened and closed repetitively and this operation sustained for long periods of time. Many schemes were advanced to accomplish this. One popular way is shown in figure 1-2. The idea is that the switch contacts were on a leaf spring with an iron disk at one end. The disk was located close to the end of the induction coil core so that as the current built up in the primary winding a

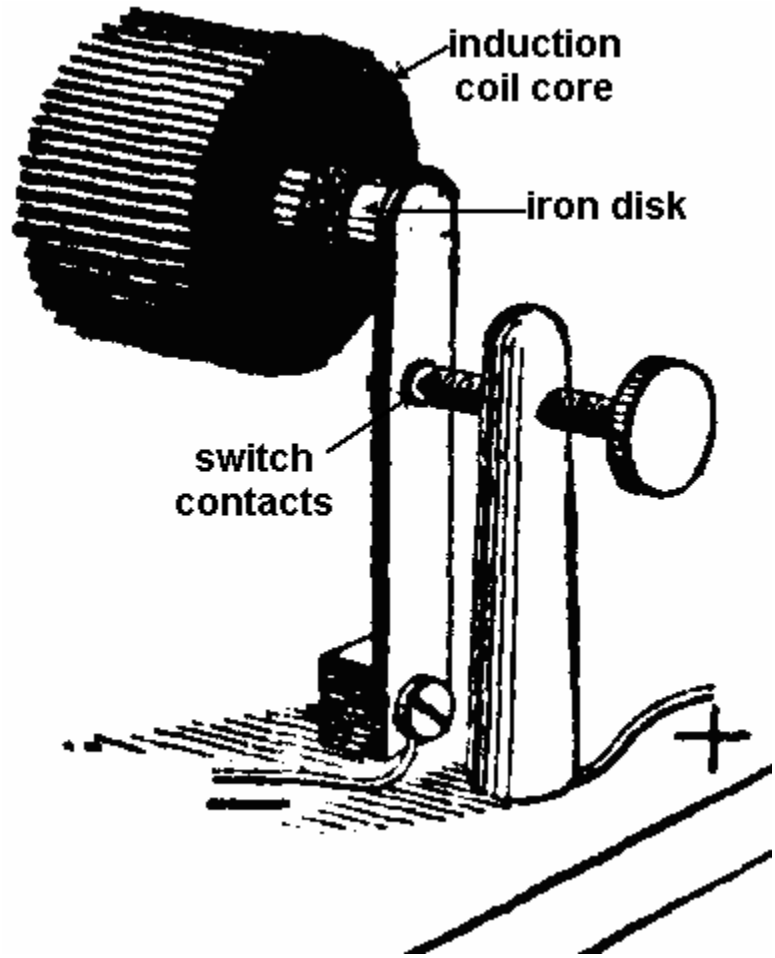


Figure 1-2, induction coil switch arrangement.

point would be reached where the iron disk would be pulled towards the core, opening the contact and the primary circuit. After some period of time the energy stored in the core would dissipate (hopefully, in the secondary arc) reducing the holding force on the iron disk and allowing the spring action to reclose the contacts to

repeat the cycle. The circuit is self oscillating and represents a very early version of a self-oscillating DC-AC inverter operating in the continuous conduction mode (the coil energy did not quite go to zero before the spring closed the primary circuit for the next cycle, so there would be some current in the primary when the switch was re-closed). It is also an example of peak current mode control of the switch because the switch opens when an appropriate peak current is achieved. The leaf spring stiffness and spacing from the core were used to adjust the activation point.

As soon as the early workers had repetitive switching they immediately discovered the intrinsic problem of opening a switch with an inductive load. Early on an arc across the primary switch contacts was noticed when the switch opened. This arc had two effects, first it rapidly eroded the contacts. Second, some or even most of the available energy, intended for the secondary spark, was being consumed in the primary switch, which often heated rapidly. The switching loss was too high! Over 160 years ago the relationship between loss and switch behavior in an inductive circuit was recognized.

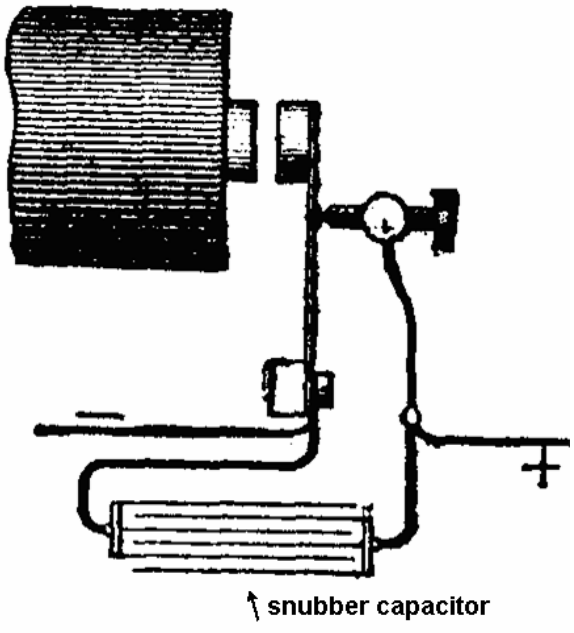


Figure 1-3, the capacitive snubber added across the switch contacts by Fizeau, 1853.

In 1853 Armand Fizeau [118] provided a solution for the problem. As shown in figure 1-3, Fizeau placed a capacitor across the contacts. When the switch turns off, the switch current is commutated to the capacitor but the voltage across the capacitor is very small because the switch has discharged it and only rises slowly as the integral of the current. The result is to allow the switch contacts to open with a very low voltage across them, minimizing the primary arc. This is exactly the same action we see in modern semiconductor capacitive turn-off snubbers. It is clear from Fizeau's paper that he understood exactly what the problem was and invented a solution. Of course the presence of a capacitor across the primary while the secondary was discharging led to the kind of ringing voltage waveform we often see associated with modern snubbers. Snubbers can perform very useful functions but almost always there is a price to pay in the "side effects" introduced by the snubber. We will see this recurrent theme in later chapters.

Because switching of inductive loads is intrinsic to most power conversion a great many schemes have been advanced for "commutation aids" - circuits which reduce the loss or stress on a switch while turning on or off. These range from a wide variety of snubber circuits, soft switching using resonant transitions, zero current switching (ZCS) resonant converters and ZCS and zero voltage switching (ZVS) quasi-resonant circuits. ZVS switching implies that at turn-on and/or turn-off the voltage across the switch is close to zero or at least small. There may however, be current flowing during the transition. ZCS switching implies that at turn-on and/or turn-off the current is very small. Both conditions can lead to significant reduction in switching loss.

ZVS and ZCS switching using resonant transitions is presently an active topic. The latest revival of interest is relatively recent and this technique is widely thought to represent something new. While certainly very useful, it's not new by any means. Resonant transition switching is an idea with a long history in power conversion.

In the early 1920's radio equipment began to be widely used in vehicles. Most of these early vehicles could only provide low voltage DC (6-24 V) power sources. Unfortunately the vacuum tube technology of the day required the use of DC voltages of 100 V or

more. One of the most common means to provide high voltages was to employ a mechanical vibrator to chop the input DC to make AC, pass it through a step-up transformer, then rectify and filter it on the secondary. An example of such a DC-DC converter is given in figure 1-4. This figure was taken from the 1947 Mallory Handbook [276] but represents a technology that matured in the late 1920's and early 1930's.

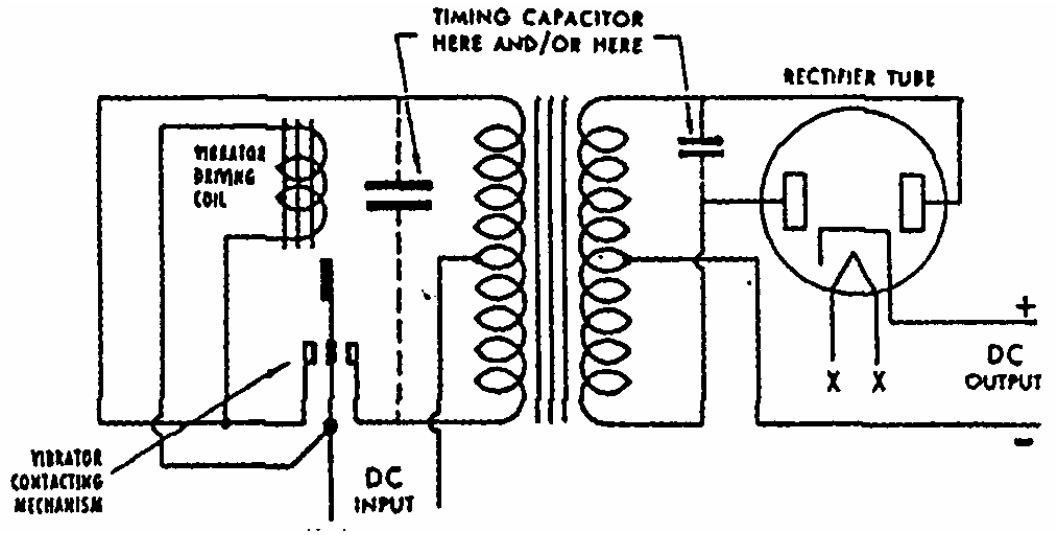


Figure 1-4, example of a vibrator DC-DC converter.

In figure 1-4 there is a capacitor (referred to as the "timing" capacitor) placed across either the primary or the secondary windings of the transformer. This capacitor, along with transformer leakage and magnetizing inductances, provided resonant transition switching that greatly extended the vibrator contact life. That this example exactly reproduces the modern resonant transition switching can be seen in Figure 1-5 which shows typical circuit waveforms [276] associated with figure 1-4. Figure 1-5C shows that the transition is the first part of a resonant ringing waveform. A deadtime (t_2 & t_4) between the opening of one set of contacts and the closure of the other set, was deliberately introduced to allow for resonant transition switching. The discussion in the handbook goes on to point out the effects of too small and too large a deadtime. The length of the deadtime was controlled by the inertia of the reed, which had a small weight on it, and the spacing of the contacts. Obviously the concept of resonant transition switching was clearly understood 80 years ago!

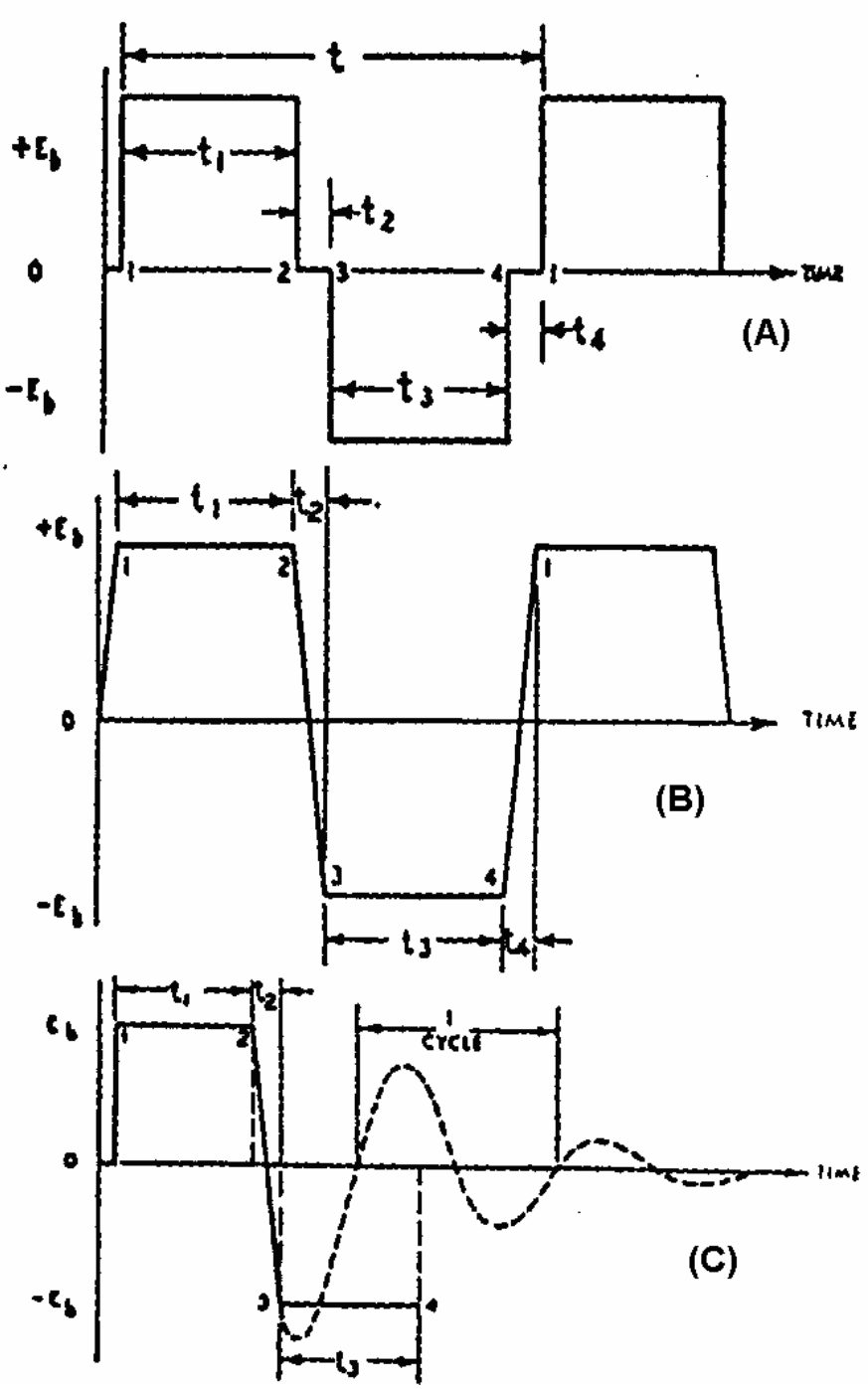


Figure 1-5, switching waveforms associated with figure 1-4.

When power transistors became available in the mid-1950's, vibrators began to be replaced with transistors with anti-parallel diodes as shown in Figure 1-6 (along with representative current and voltage waveforms). Note that the switch current was deliberately made negative at switch turn-on (an inductive load), with the current flowing through the anti-parallel diode to provide zero-voltage turn-on.

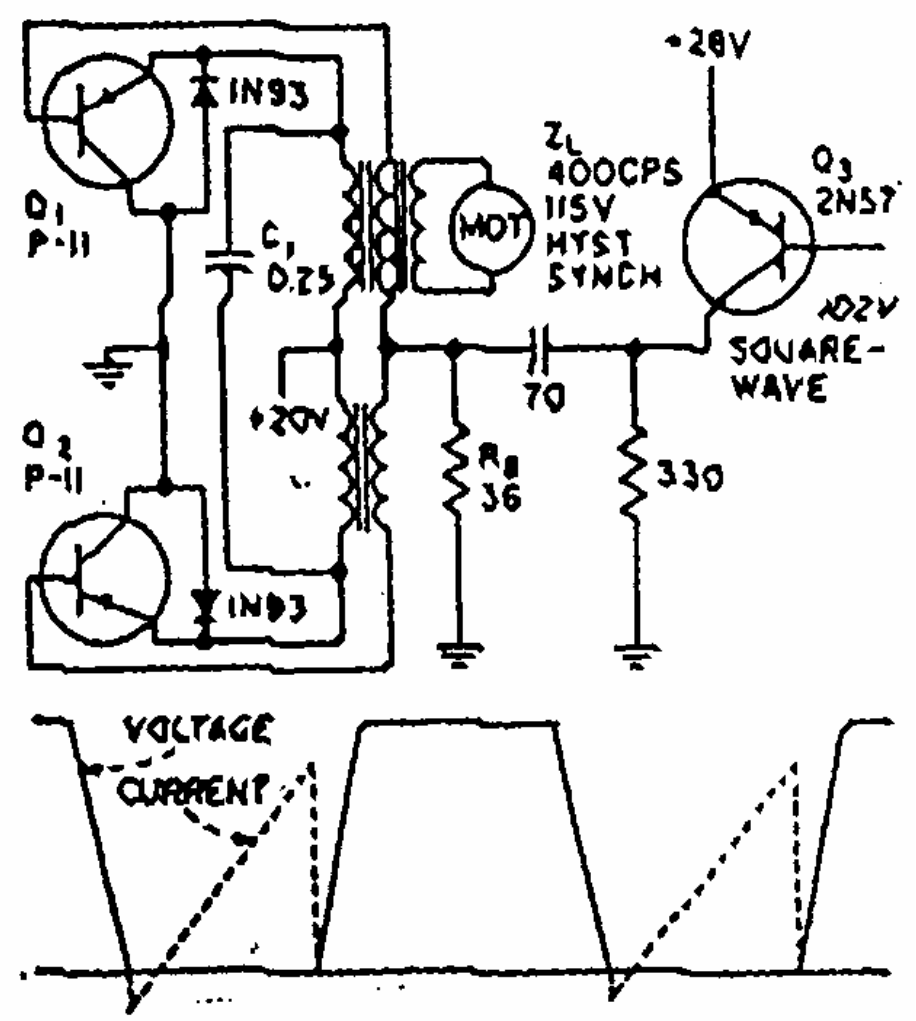


Figure 1-6, DC-AC inverter with soft switching.

A capacitor was used along with the transformer inductances to provide resonant transition switching. These Figures are taken from a 1958 Electronics magazine article[53] that specifically addresses the issue of increasing switching efficiency by using what we now refer to as “soft-switching”.

Vibrator and transistor inverters were not the only applications for soft switching. Beginning the 1930’s inverters using thyratrons, grid controlled mercury arc tubes and ignitrons were in common use and also required switch commutation aids. When thyristors become available in the late 1950’s, the earlier technology from thyratrons, ignitrons and magnetic amplifiers was adapted for the new devices. Over a period of 50 years almost every conceivable commutation circuit was examined. Commutation using an auxiliary switch, of

which much has recently been written, is a very old trick that has been well explored in an amazing variety of variations beginning more than 70 years ago.

We can extend the term “soft switching” to cover a wide variety of snubber circuits which are intended to reduce switching loss. For example the conventional RC-diode snubbers can be designed to provide very soft, low-loss turn-off by selecting an appropriate capacitor value. An analysis of a typical soft switching circuit, such as the phase-shifted bridge circuit with a primary inductor, shows that at turn-off the behavior is exactly the same as a normal RC-diode snubber and the turn-off loss in the switches is described by the same equations.

The need for commutation aids when using switches with inductive loads has been obvious from the beginning. If nothing else the arcing of the contacts or the failure of the switches would bring this to the attention of the experimenter. This requirement drove the invention of most of the techniques we now use.

In some ways a mechanical switch is more difficult to protect than a typical semiconductor switch. A mechanical switch has a voltage breakdown problem not normally seen in electronic switches. The breakdown voltage of the gap between the contacts depends on the spacing between the contacts (among other things). When the switch first starts to open, the spacing is very small and the breakdown voltage low. As the switch contacts open, the breakdown voltage capability increases rapidly but you still have the initial vulnerability because the arc can be sustained as the contacts open. To minimize arcing, it is necessary to have a capacitor large enough that the rate of rise of voltage across the contacts is slower than the rate of rise of the breakdown voltage capability. This subtlety was appreciated 150 years ago.

The point of this history lesson has been to show that the problems arising from switching an inductive load come from the nature of the load and the desire to combine it with a switch. Problems arise because we are "switching" and are not necessarily unique to a particular type of switch. Because of the universality of these problems, snubber techniques have a long history in power

conversion with all types of switches. Of course each switch type has it's own set of limitations which must be taken into account when designing a snubber but the basic principles are relatively independent of the switch type.

What is a snubber?

That sounds like a very simple question but unfortunately there is no simple answer. The reason is that circuits referred to as "snubbers" often perform quite different functions. The term "snubber" appears to have come down to us from a damping element in a mechanical system with masses and springs. The purpose was (and still is for that matter) to damp mechanical oscillations. The common automotive shock absorber is a form of mechanical snubber.

For electrical circuit snubbers one definition might be:

> *A snubber is a network that alters the voltage and/or current waveforms of a switch during turn-on and turn-off.*

While probably true, this definition is so general as to be of very limited use.

Rather than trying to work up some contorted universal definition to cover every case, it's easier to simply list typical applications and extend that list as we think up new ones. Here are some:

- peak voltage limiting
- peak current limiting
- dV/dt limiting
- dI/dt limiting
- load-line shaping to stay within the safe operating are (SOA) boundaries
- improve circuit reliability through reduced electrical and/or thermal stress.

- switching loss reduction
- transfer of switching loss from the switch to a resistor or a useful load
- EMI reduction
- voltage sharing in series devices
- current sharing in parallel devices
- increasing the power obtainable from a given device or devices in a given application
- extension of switch service life

Following comments apply to snubbers:

- A snubber controls or manages energy on a transient basis during and immediately after switching transitions.
- The use of a snubber can greatly increase the power handling capability of a given device or increase it's reliability or both.
- Snubbers are sometimes referred to as "switching" or "commutation" aids.

Classifying snubbers

There have been many attempts to derive universal classification schemes[106] for snubbers. The problem is the many different functions performed by circuits we call "*snubbers*". In general such schemes haven't been particularly useful but for the purposes of this book, we will group snubbers with similar characteristics. None of these distinctions are very rigorous but are convenient to subdivide the discussion:

- Passive.

Snubbers made up of lumped linear network elements, i.e. resistors, capacitors and/or inductors.

- Active-lossy.

These are networks which use non-linear or active devices such as diodes or switches in addition to resistors, inductors and/or capacitors. This class of network dissipates a majority of the switching loss but usually in a resistor rather than in the switching device.

- Active-low loss.

In this type of snubber circuit the energy which would normally be lost in the snubber resistor(s) is delivered either to the input source or to some useful load.

- Non-polarized.

These are networks which have no preferred polarization, i.e. they can be installed in the circuit without regard to polarity. An example would be a simple series R-C damping network.

- Polarized.

Most snubber networks using active devices can be installed in the circuit with only a given polarity. At least in principle, almost any polarized snubber network can be made non-polarized by imbedding it in a diode bridge. This is similar to the 4-quadrant switches shown in figure 2-5 (see chapter 2). But in general most active snubbers have a defined polarity.

- Soft switching

Conceptually, "Soft switching" is enabling the switch to turn on and/or off with either very low voltage across the switch or very low current through the switch. This can result in

very low switching loss and stress. Many snubber circuits do provide varying degrees of soft switching but this term is usually reserved for circuits which use either resonant topologies or some form of resonant transition switching to control switch stress. While these approaches are very popular and useful techniques, they are beyond the scope of this book.

Snubber trade-offs

No matter how useful or interesting snubber circuits may be they still require design compromises between:

- cost
- complexity
- reliability
- loss
- circuit performance

To list just a few. Of course these trade-offs would apply to any electronic circuit. Snubbers are no different in this respect. There is one very important trade-off which is unique to snubbers and which we will see repeatedly in later chapters describing circuit operation:

> *In many, if not most, cases when a snubber is added to the circuit, in addition to alleviating one problem, some additional new stress will be introduced into the switch.*

The benefits of the snubber must be traded against it's disadvantages by selecting component values which achieve the desired results while minimizing the undesired.

Chapter 2

Things You Need To Know About Switches

All switches have limitations such as peak voltage, peak and average current, power dissipation, switching speed, etc. Snubbers are used to improve the performance and reliability of switches imbedded in power circuits but to properly apply snubber techniques it is important to understand how switches themselves behave. This chapter is devoted to a review of switches. We are not going to go into the detailed behavior of each type of switch, but rather look at the general behavior shared by all switches. For specific semiconductor switches see the bibliography. The discussion by Mohan, Undeland and Robbins[296] is a particularly good one for semiconductor switches.

The ideal switch

The simplest form of switch can be represented schematically as shown in figure 2-1.

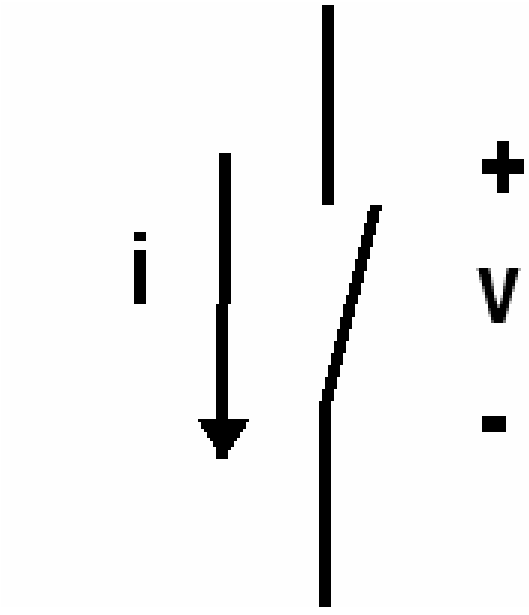


Figure 2-1, representation of an ideal switch including current and voltage polarity conventions.

This is just a two terminal device which blocks current when open and conducts current when closed. An ideal switch, in the open or "off" state, will conduct no current with a voltage of either + or - polarity applied across the terminals. In the closed or "on" state, an ideal switch will conduct current in either direction but have no voltage drop across the terminals. In other words it is a bipolar device which presents an infinite impedance when off and zero impedance when on. This means there is no power dissipation in either state. A further property usually associated with an ideal switch is that the transitions from on-to-off and off-to-on are instantaneous. Ideally switching is accomplished with no power loss.

Power conversion circuits frequently require more than a simple SPST switch. More complex switching functions such as the SPDT switch shown in figure 2-2, can be implemented from combinations of SPST switches.

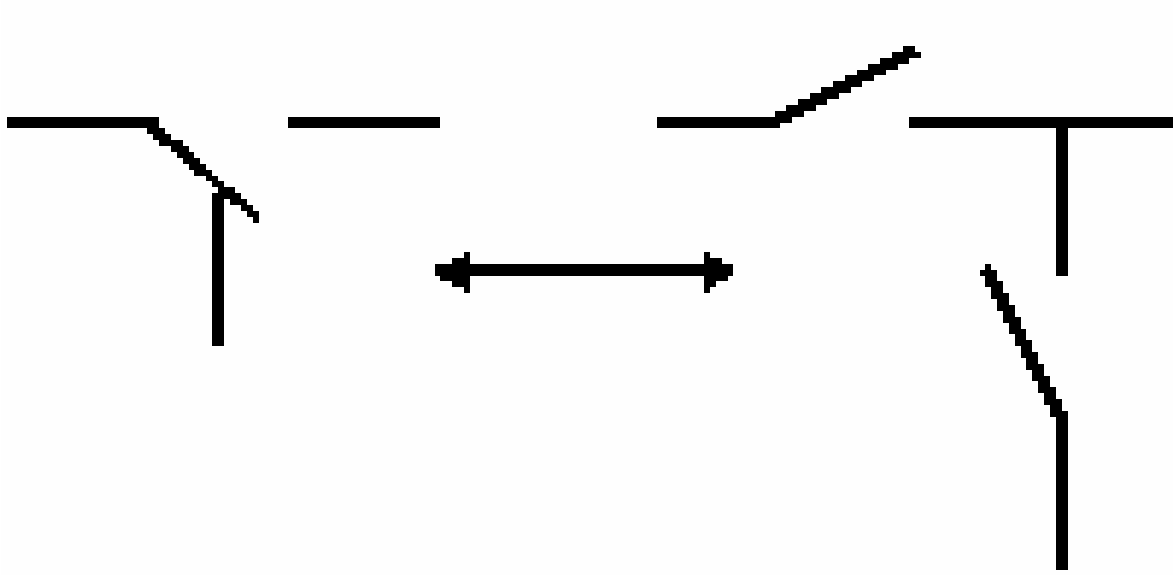


Figure 2-2, more complex switches are made up from combinations of simple switches.

A generalized switch concept

In selecting devices to be used as switches we normally think in terms of some specific type of semiconductor device. A MOSFET or a thyristor for example. However, it is often more productive to think in terms of a more general form of switch: i.e. the device or circuit which performs the switching function may be composed of multiple semiconductors and other components such as capacitors, inductors and resistors, in a network. Examples of this might be a BJT combined with a snubber network as shown in figure 2-3. The result may be a more rugged and/or less expensive and/or more efficient switch. In many cases the most appropriate approach uses multiple devices working together to implement the desired switch function.

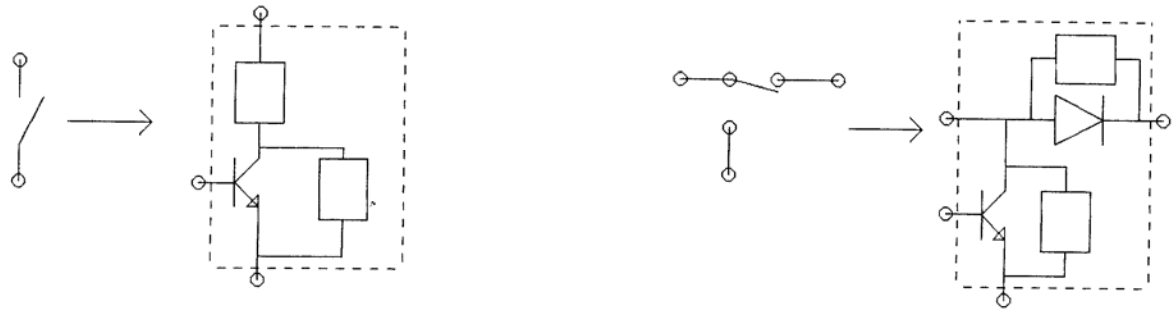


Figure 2-3, example of "switches" being implemented with a combination of a semiconductor devices and auxiliary components.

Switches are sometimes implemented by either the series or parallel combination of the same or different types of devices: a MOSFET in the emitter of a BJT for example. Many different combinations are seen in practice.

Real switches

Real switches take many forms: mechanical, vacuum tube, gas discharge or semiconductor. Although most of the techniques presented in this book can be applied to different kinds of switches we will limit our attention to semiconductor switches because they are

by far the most common type employed today. Semiconductors are of course not ideal devices and have many limitations:

a. There will be a voltage drop across the device during conduction (on-state).

b. There will be some current flow in the off-state.

c. Transition times from on-to-off and off-to-on are finite and therefore lossy.

d. Real switches have four states: on, off, transition from on-to-off and transition from off-to-on. In most cases the transitions will not be symmetrical.

All of these lead to power dissipation in the switch. In addition there are other limitations such as maximum blocking voltage, maximum conduction current, maximum dv/dt and di/dt rates, polarity of the conduction and blocking, instantaneous and average power dissipation, to name just a few. Snubber circuits are used to mitigate the consequences of non-ideal behavior in semiconductor switches.

Fortunately ideal switch behavior is usually not required. Take for example switch transition time or "switching time". In an ideal switch this time is zero (i.e. instantaneous). With power MOSFETs switching times of less than 1 nsec are possible, which is a pretty good approximation of instantaneous in most applications. However, because of interaction with other switches and elements in the circuit, such rapid transitions can lead to a host of problems, such as EMI, increased power loss in other devices, increased peak voltage and current stresses and inappropriate turn-on of other switches in the circuit. In practice what we really want is to be able to control both switching time and the instantaneous voltage and current waveforms during the transitions to suit the application. In many applications it is not necessary to block bipolar voltages or conduct bipolar currents. Unipolar capability is sufficient.

The point here is *don't try to provide performance you don't need for the application*!

Another important switching device characteristic is how the switch is commutated (turned on and off). There are many kinds of semiconductor switches with different commutation requirements. These are summarized in table 2-1.

Table 2-1 Semiconductors and how they are commutated

Device	Turn-on	Turn-off
diodes	circuit	circuit
thyristor family	external	circuit
BJT, MOSFET IGBT, GTO, MCT	external	external

The following examples illustrate the point being made in table 2-1. A diode is a two-terminal device that is in conduction as long as it is forward biased. It turns off only when the terminal voltage reverses and the charge within the device allowed to dissipate. Turn-on and turn-off are controlled by the circuit in which the diode is imbedded.

Some devices, such as the thyristor family, can be commanded to turn on by an external pulse applied to the gate. However, to turn off and be able to block voltage, the current in these devices must first go to zero and remain there for a appreciable length of time, often many μsec. With these devices turn-on is via a gate pulse but turn-off is controlled by the circuit in which they are imbedded. There will frequently be auxiliary switches and associated networks to force turn-off.

Commutation of devices like the BJT, MOSFET or IGBT is in response to an external signal for both turn-on and turn-off. One caution however, some devices, like the IGBT, may be driven into a mode where they will not turn-off on command.

A common problem is the unintended turn-on by circuit waveforms, independent of the desired gating signal. Snubbers can play an important role in avoiding these undesired commutations.

Switch operating quadrant

We can segregate switches by the polarity of the voltages and currents they can conduct or block. The operating quadrant of a switch can be defined using figure 2-4.

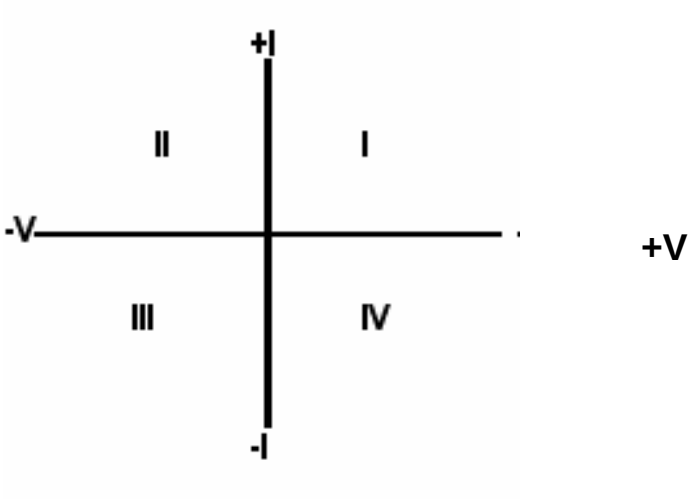


Figure 2-4, operating quadrant.

The circuit application determines the quadrant capabilities required in the switches. Figure 2-5 gives examples of 1, 2 and 4-quadrant switches.

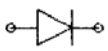
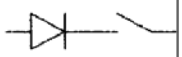
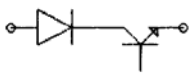
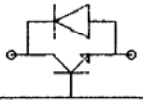
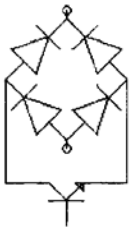
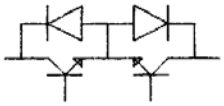
block voltage	conduct current	quads	device	
uni	uni	1		
bi	uni	2		
uni	bi	2		
bi	bi	4		 

Figure 2-5, examples of 1, 2 and 4-quadrant switches.

The load-line concept

A switch will assume several states during an operating cycle, on, transition to off, off, transition to on, which are repeated each cycle. Both the current through the switch (I) and the voltage across the switch (V) will vary during an operating cycle. The instantaneous values of V and I can be visualized by looking at their waveforms on an oscilloscope. But there is another very useful way to visualize switch operation over a switching cycle. Instead of plotting V and I separately against time, we can plot them against each other on a V-I diagram like that shown in figure 2-6 which shows the instantaneous V and I at each point during the switching cycle. This is referred to as a "load-line diagram".

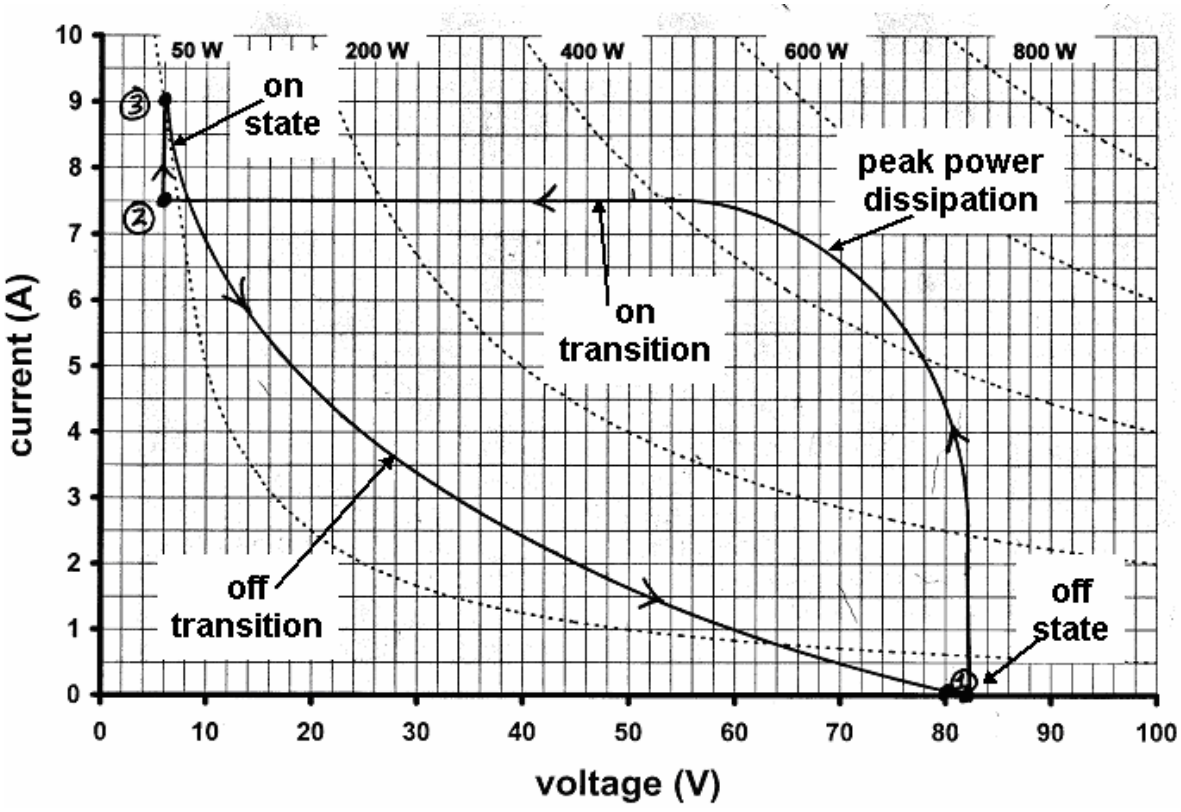


Figure 2-6, an example of a load-line diagram.

The dashed lines represent lines of constant power dissipation, i.e. the product of the instantaneous V and I. This picture allows us to see

at a glance the stresses on the switch due to it's interaction with the circuit and also the effect of a snubber if present. The solid lines on the diagram represent a possible switching scenario. The arrows on the solid line indicate the direction of change as time progresses during the cycle. At point 1 the switch is off. At turn-on the trace proceeds to point 2 which is the completion of the on-transition. The trace between points 2 and 3 represent a possible change in current during the on-state. At turn-off, the trace transitions from point 3 back to point 1, the off-state. The load-line diagram is an important tool for illustrating the behavior of a snubber circuit.

Take special note of the relationship between the constant power lines and the load-line. For example, as we proceed from point 1 to point 2, the instantaneous power increases until it reaches a maximum of about 450 W in this example. Beyond that point the power decreases. The maximum power point, is a point of high stress on the switch, with both high voltage and high current present simultaneously. One of the many uses for snubbers is to modify the load-line to minimize this peak stress. High stress can also occur on the turn-off part of the load line.

SOA concept

All semiconductor devices have V, I and instantaneous V*I product limitations which must not be exceeded if reliable operation is to be achieved. One way to show these limitations for a given device is to plot the limits as boundaries on a V-I diagram and then plot the load-line to see if it lies within these boundaries.

An example of a pair of BJT safe operating area (SOA) graphs is given in figures 2-7 and 2-8. In operation it is important that the load-line lie entirely within the SOA. In BJT's the SOA differs between the off, transition to on and on operation versus the on, transition to off and off operation. This is the difference between "forward biased" and "reversed bias" operation. That's why there are two different SOA graphs for a single device. To use these two graphs you need to plot that portion of the load-line corresponding to turn-on on the graph in figure 2-7 and plot the portion of the load-line corresponding to turn-off on the graph in figure 2-8. An important application for

snubbers is to assure that the load-line remains within the SOA boundaries under all operating conditions that the converter is expected to survive.

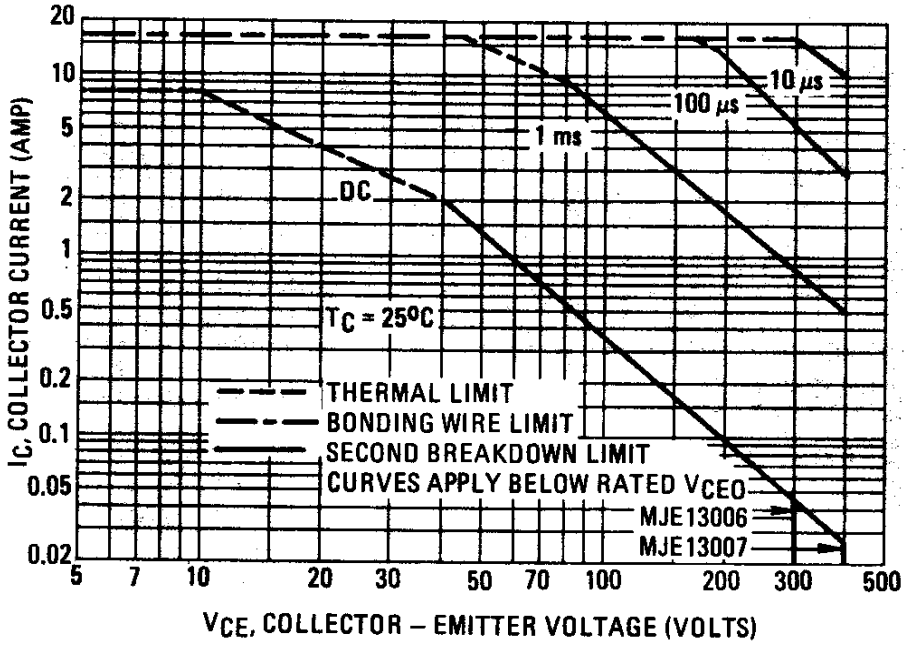


Figure 2-7, Forward biased Safe Operating Area for a MJE13006-7 BJT.

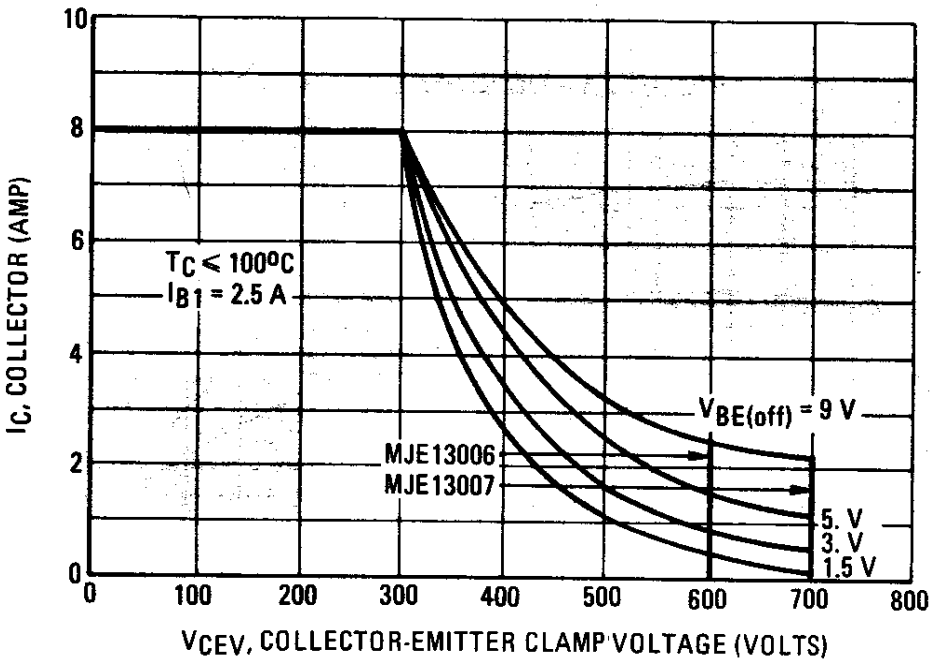


Figure 2-8, Reverse biased Safe Operating Area for a MJE13006-7 BJT.

Derating and SOA

It is normal practice to derate a semiconductor from the manufacturers maximum ratings for voltage, current, V*I product and junction temperature to increase reliability and life expectancy in actual circuit use. We can extend the concept of SOA to include the gain in useful life as illustrated in figure 2-9.

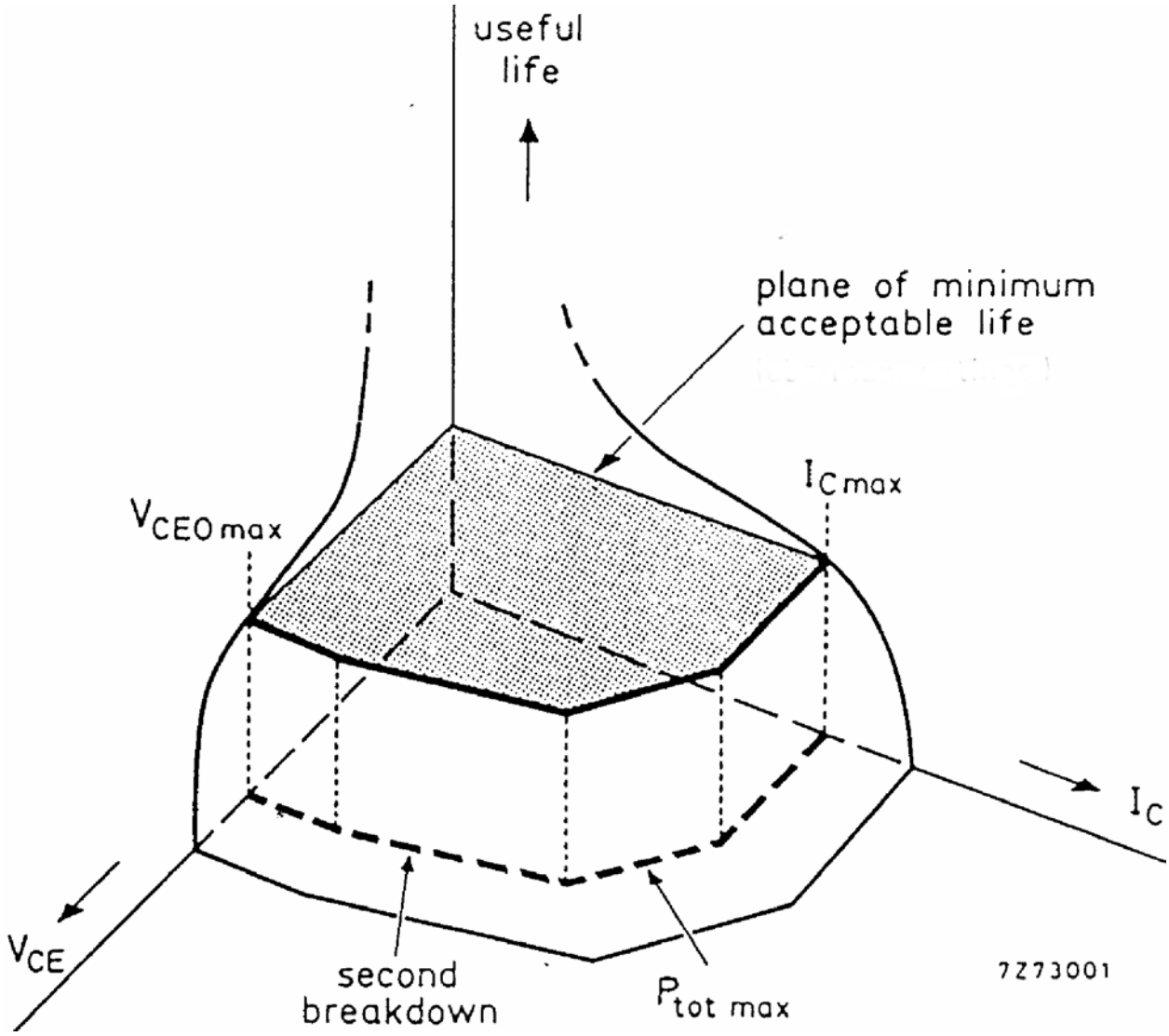


Figure 2-9, the extended SOA graph.

In addition to the limits shown on the SOA graph, some semiconductors also have limitations on dV/dt and dI/dt. This is characteristic of the thyristor family of devices. Excessive dV/dt can

lead to spurious turn-on and excessive dI/dt can lead to current crowding within the device die and lead to failure. These problems can be addressed by limiting the minimum switching time, choice of circuit and by using snubbers.

Switching scenarios

The circuits in which switches are used present different kinds of loads. The load may be resistive, inductive, capacitive or, more likely, some combination of all three. The nature of the load has a profound effect on the load-line and the choice of snubber circuit. For simplicity we will examine each case separately. Later we will combine the loads.

Resistive load switching

A resistive load is one of the simplest. Figure 2-10 shows a switching circuit with a resistive load.

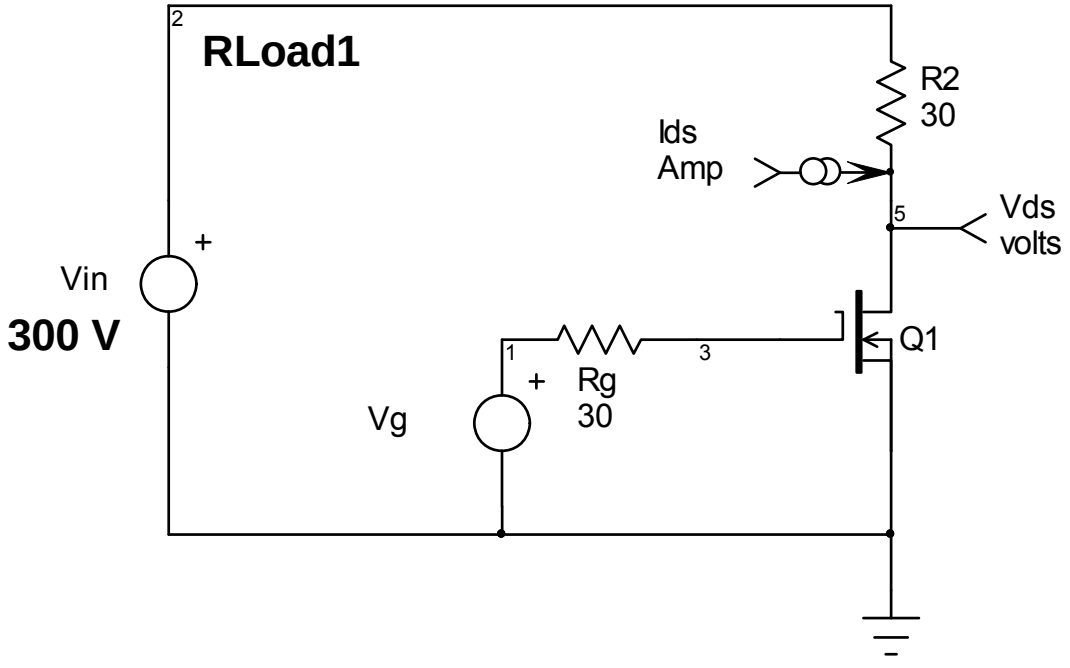


Figure 2-10, Resistive load switching example.

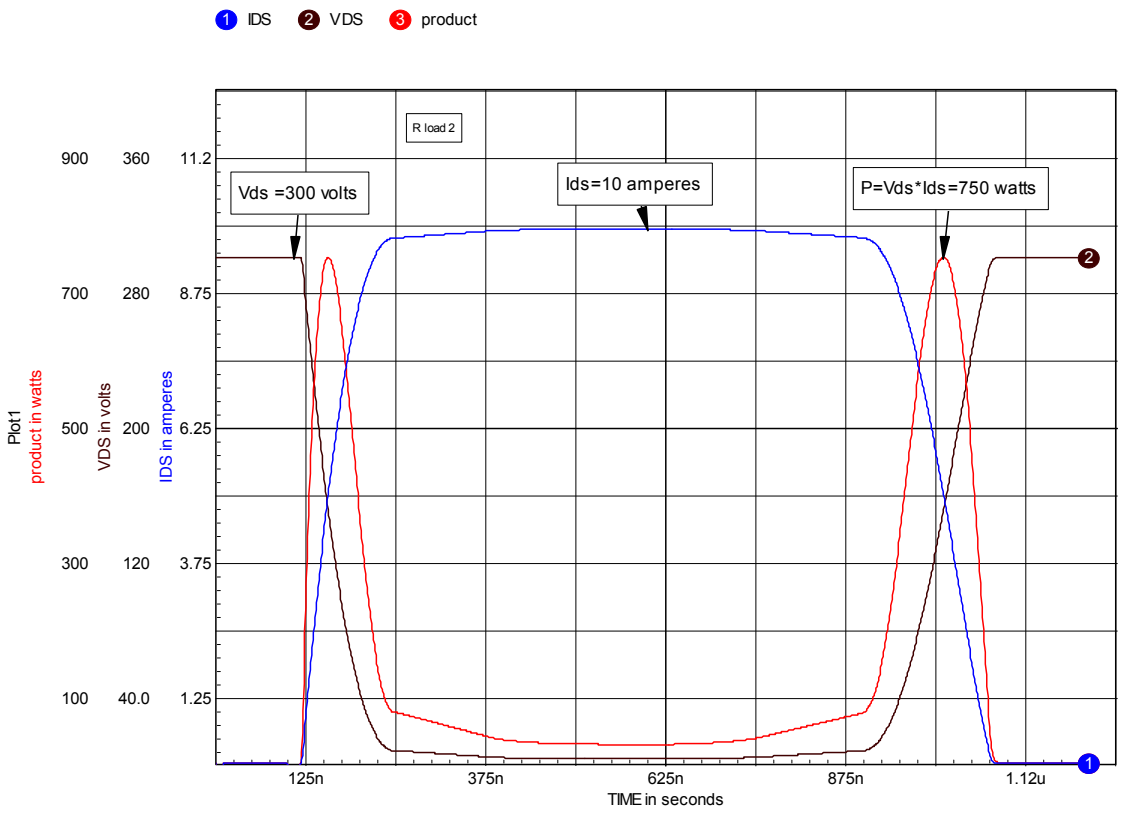


Figure 2-11, typical Vds and Ids switching waveforms with a resistive load.

Figure 2-11 shows the Vds and Ids waveforms associated with this circuit. During the off-state, Vds = Vin and Ids □ 0. As Ids begins to rise at turn-on, the current in the resistor must also increase causing a proportional voltage drop across the resistor (IdsxR$_L$) so that Vds = Vin -IdsR$_L$. Vds begins to fall as the current waveform rises. When Ids = Vin/R$_L$, Vds = 0 and the switch is in the on-state. Resistive load switching is considered to be low stress because the switch is not exposed to the maximum voltage and current simultaneously. This can be seen in figure 2-12 which is the load-line associated with figures 2-10 and 2-11. This is a typical example of a load-line diagram for a resistive load. In this example the traces for the on and off-transitions overlap so you see only a single straight line. The maximum instantaneous power occurs midway through the switch transition, which is 5 A x 150 V = 750 W.

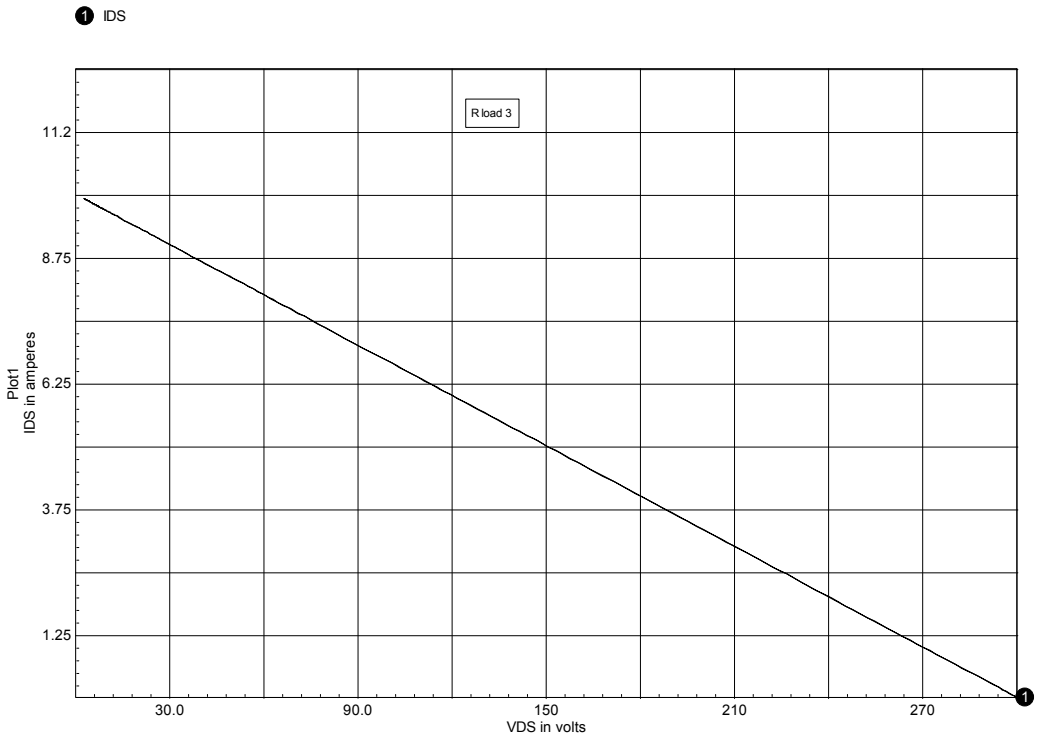


Figure 2-12, Typical resistive load load-line.

The switching loss (P_s) associated with resistive switching can be approximated from:

$$P_s = \frac{V_g^2}{6R_L}\left(t_1 + t_2\right) = \frac{V_g I_o}{6}\left(t_1 + t_2\right)$$

$$I_o = \frac{V_g}{R_L} \qquad (2\text{-}1)$$

Where f_s is the switching frequency.

Clamped inductive switching

Resistive load switching has relatively low loss and peak switch stress. Unfortunately, that type of load is rare in power conversion. More often the load will be inductive.

An example of a typical DC-DC converter is given in figure 2-13.

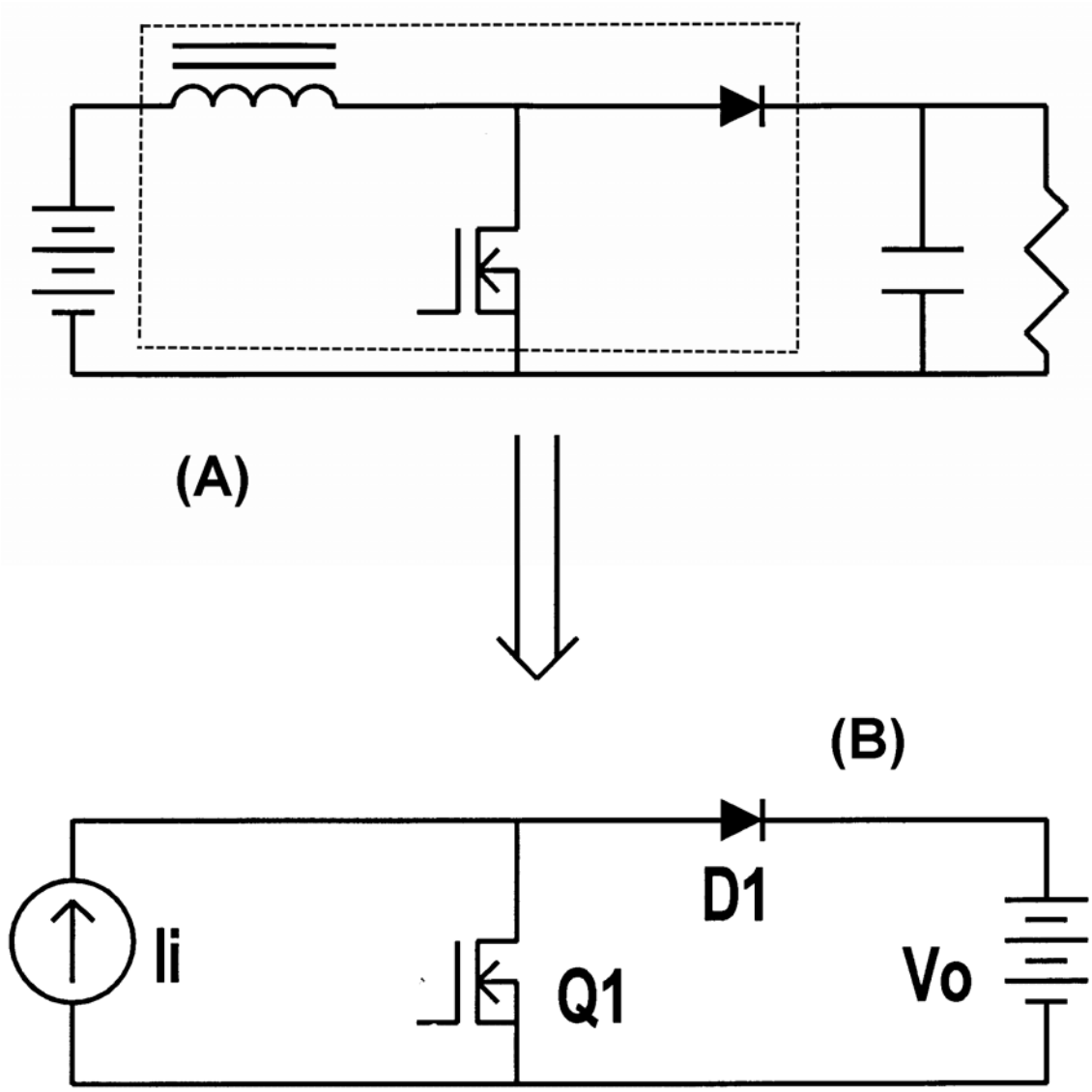


Figure 2-13, Boost DC-DC converter and its modeling approximation.

In the center of this converter (2-13A) there is an outlined network consisting of an inductor, a diode and a switch. This sub-network, and consequently this type of switching, is ubiquitous in power converters. To illustrate this point examples of other topologies where this sub-network appears are given in figure 2-14.

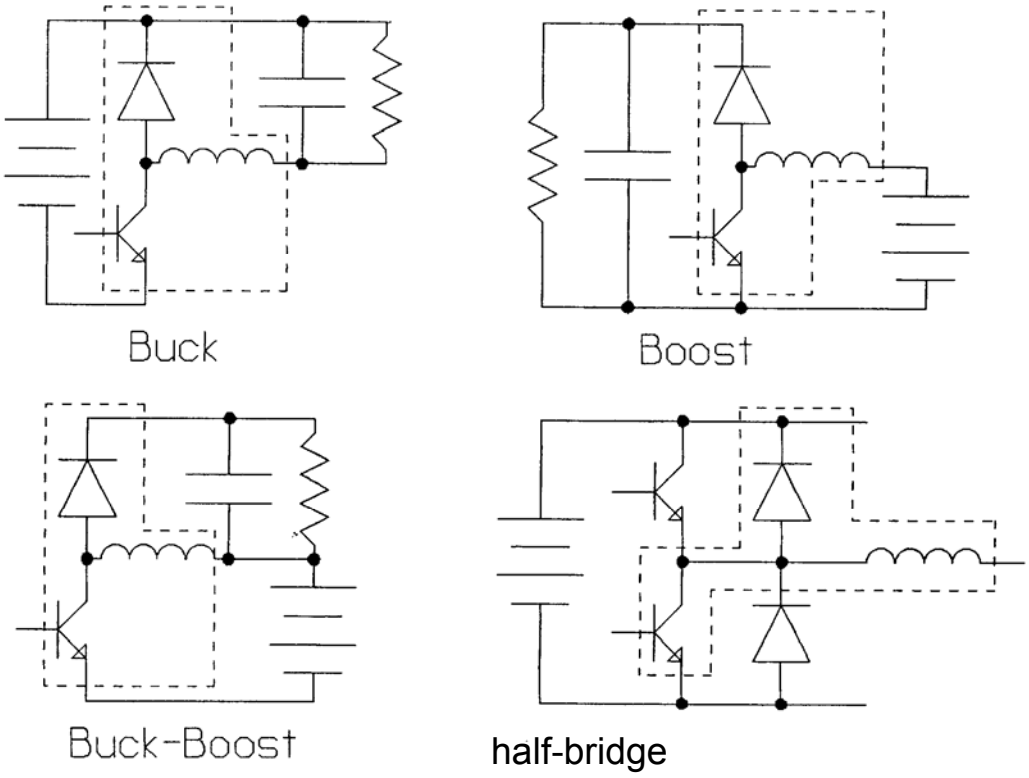


Figure 2-14, Switching topology examples.

For the purposes of this book we are concerned with the circuit behavior during switching transitions. Normally transition times will be very short compared to "on" and "off" time intervals so there is very little change in either the inductor current or the output voltage during transition intervals. To simplify modeling we can use this observation to replace the voltage source and input inductor with a constant current source and we can replace the output load and filter capacitor with a constant voltage source, as shown in figure 2-13B. For our purposes this simplification doesn't greatly change the waveforms we are concerned about and we will use this simplification extensively.

In the discussion which follows, and indeed throughout the remainder of this book, we will use the boost converter, operating in the continuous inductor current mode, as an example of "clamped inductive switching" as we discuss various snubber circuits. This type of switching is almost universal in power conversion so the discussion, even though limited to a specific converter topology, applies in general.

To model this type of load we can use the SPICE model shown in figure 2-15. Initially we'll use an ideal diode for D1 but later we will change to a real diode and see the effect on circuit operation. Resistor R2 is there as a means for metering Ids and has little effect on circuit operation.

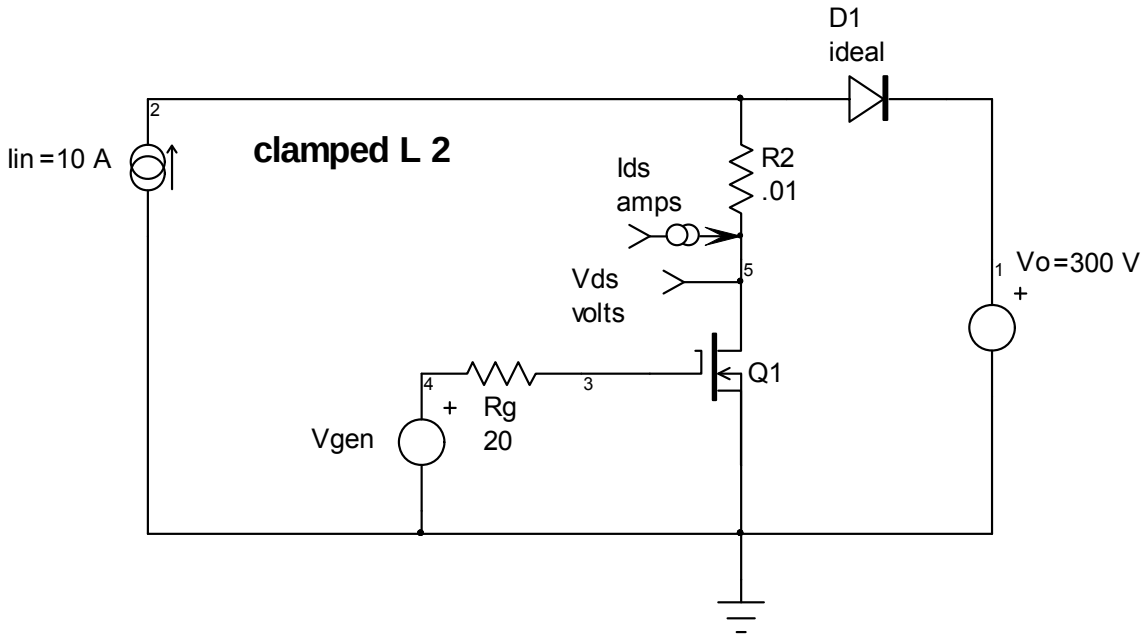


Figure 2-15, Clamped inductive switching circuit.

To make comparisons between switching scenarios easier, the nominal switch voltage has been set at 300 V and the switch current at 10 A as was done for the resistive switching example (figure 2-10). To provide continuity to the switching and snubber discussion to follow we will use these parameters consistently for most examples except where a change in value is needed to illustrate some point.

The waveforms associated with the circuit in figure 2-15 are shown in figure 2-16. Notice that at turn-on, Ids must rise to it's full value before Vds begins to fall. At turn-off Vds rises to it's full value before Ids can begin to fall. This means that the switch is exposed to both the maximum current and maximum voltage simultaneously. This is in contrast to the resistive switching case where Vds starts to fall as Ids begins to rise.

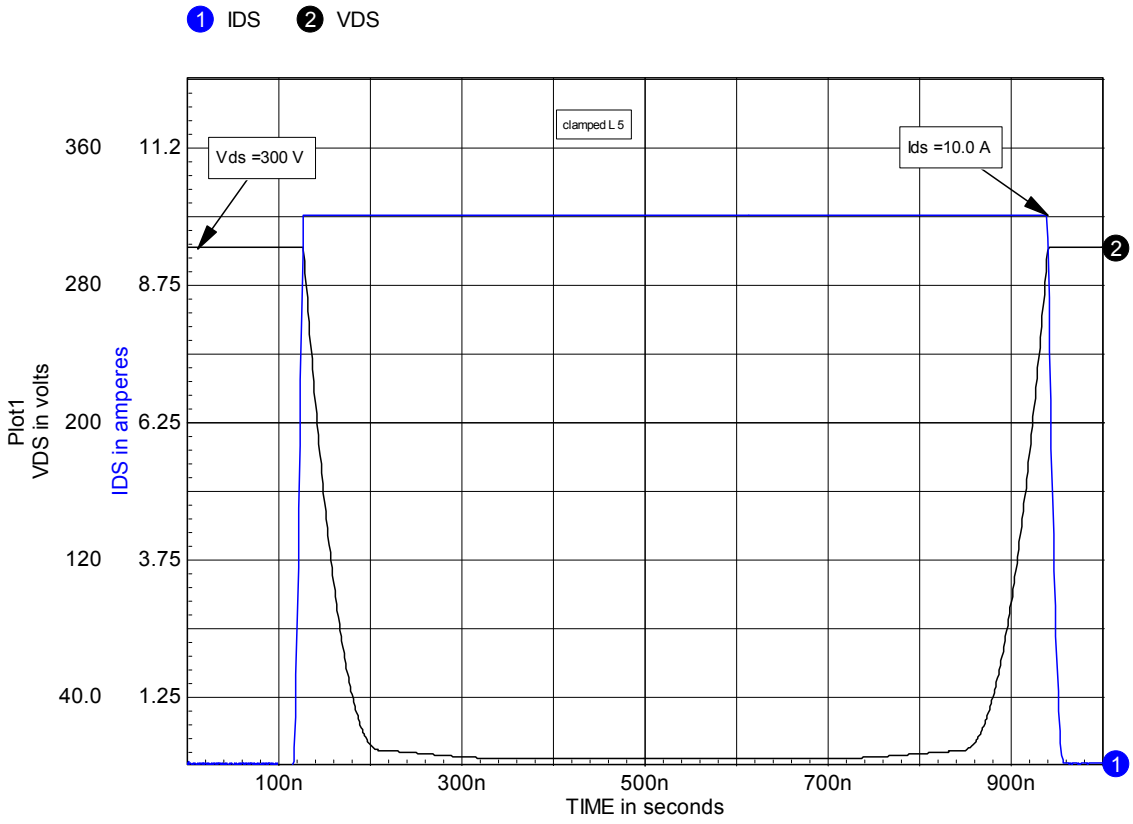


Figure 2-16, Idealized clamped inductive switching waveforms.

We can understand this behavior by examining the model. The connection point for Iin, D_1 and R_2 forms a node at which Kirchhoff's current law must be satisfied: i.e. the sum of the currents into and out of the node must be zero at all times.

When Q_1 is off, Iin must flow through D1 into the output (Vo). This means that in the off-state Vds = Vo. As Q1 turns on and Ids begins to rise, the current in D1 will start to fall (being the difference between Iin and Ids). However, as long as there is any forward current in D1, the diode will in effect be a short circuit and Vds = Vo. When Ids = Iin, the current in the diode is zero and it stops conducting. This allows Vds to fall. For the moment we will ignore the reverse recovery current inherent in real as apposed to ideal diodes.

As Q1 turns off, no current can flow in D1 until Vds reaches Vo, forward biasing D1, so Ids (in Q1) remains constant. When Vds reaches Vo, D_1 conducts and Ids can begin to fall.

The instantaneous power dissipation in Q1 is shown in figure 2-17.

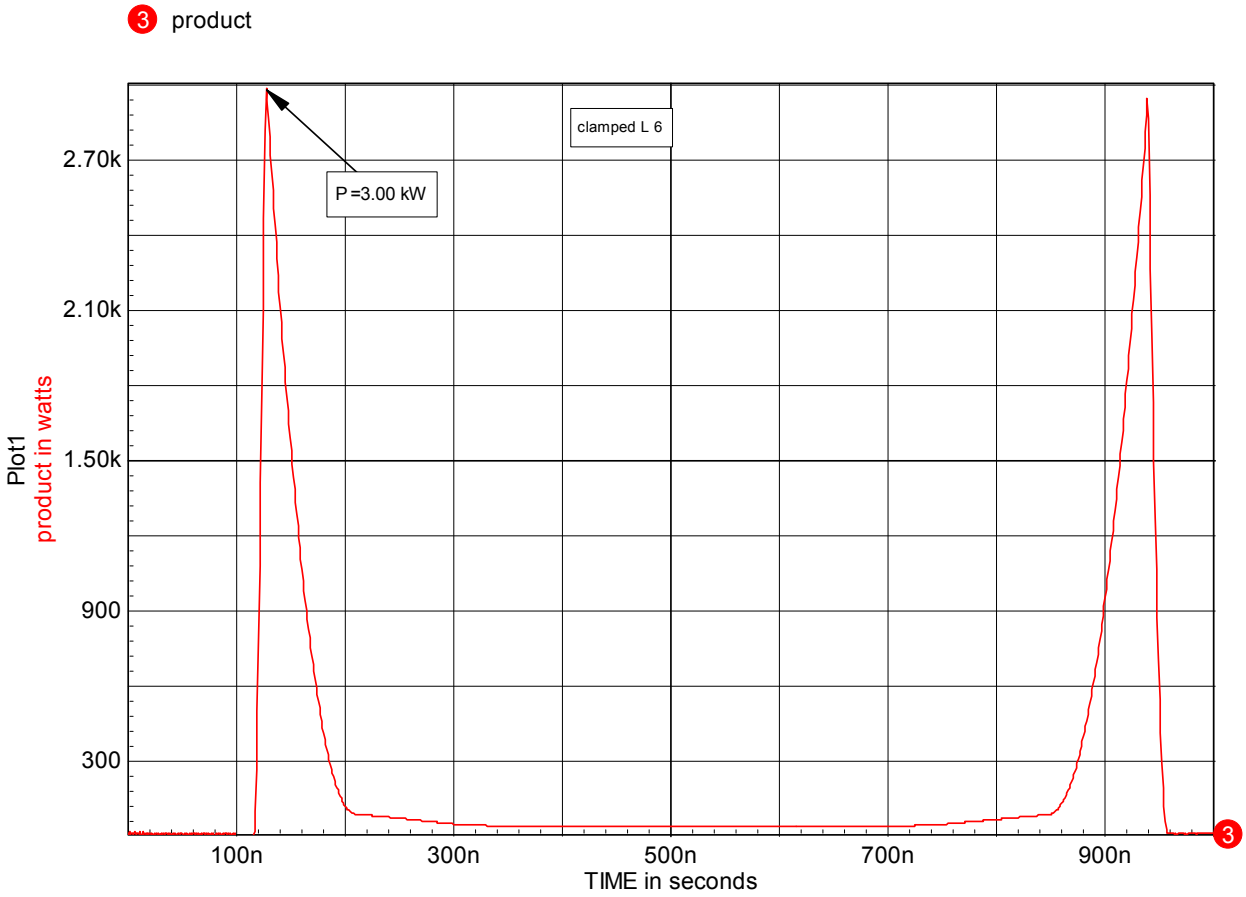


Figure 2-17, Power dissipation during the switching interval for the circuit in figure 2-15.

The peak power is now 3,000 W, which is four times the 750 W for the resistive switching example (figure 2-11) with the same switch peak voltage and current.

The load-line in figure 2-18 illustrates why the power is so high. This load-line is essentially rectangular with the maximum Vds and Ids occurring simultaneously on both turn-on and turn-off. The turn-on and turn-off traces overlap. This is often referred to as "hard switching" and is obviously much more stressful than resistive load switching.

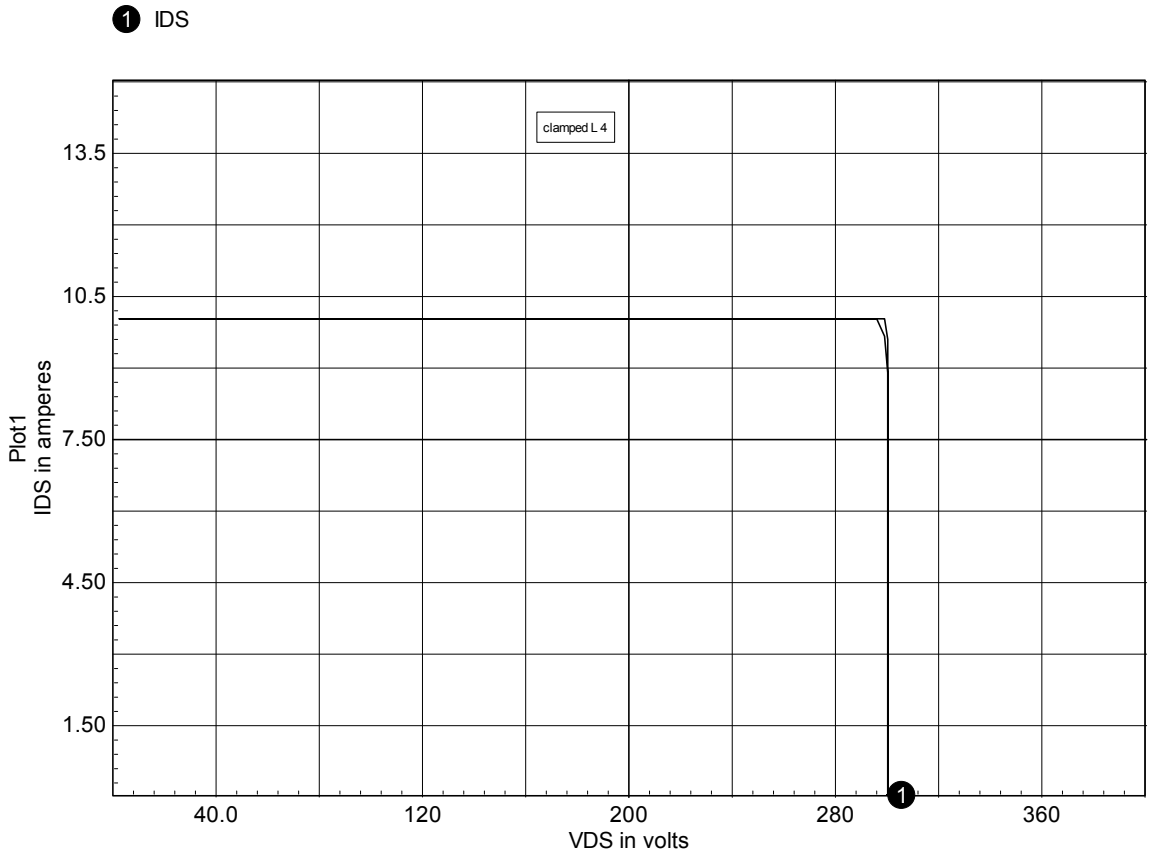


Figure 2-18, Switching load-line for the circuit in figure 2-15.

The power loss due to switch transitions with a clamped inductive load can be approximated from:

$$P_s = \frac{V_o I_{in}}{2}\left(t_1 + t_2\right) \qquad (2\text{-}2)$$

For the same values of maximum voltage and current, the loss for clamped inductive switching is three times that for resistive load switching and the peak power dissipation is four times.

If we change D1 in figure 2-15 from an ideal diode to a real diode, which will display reverse recovery current, the situation gets even worse as shown in figure 2-19.

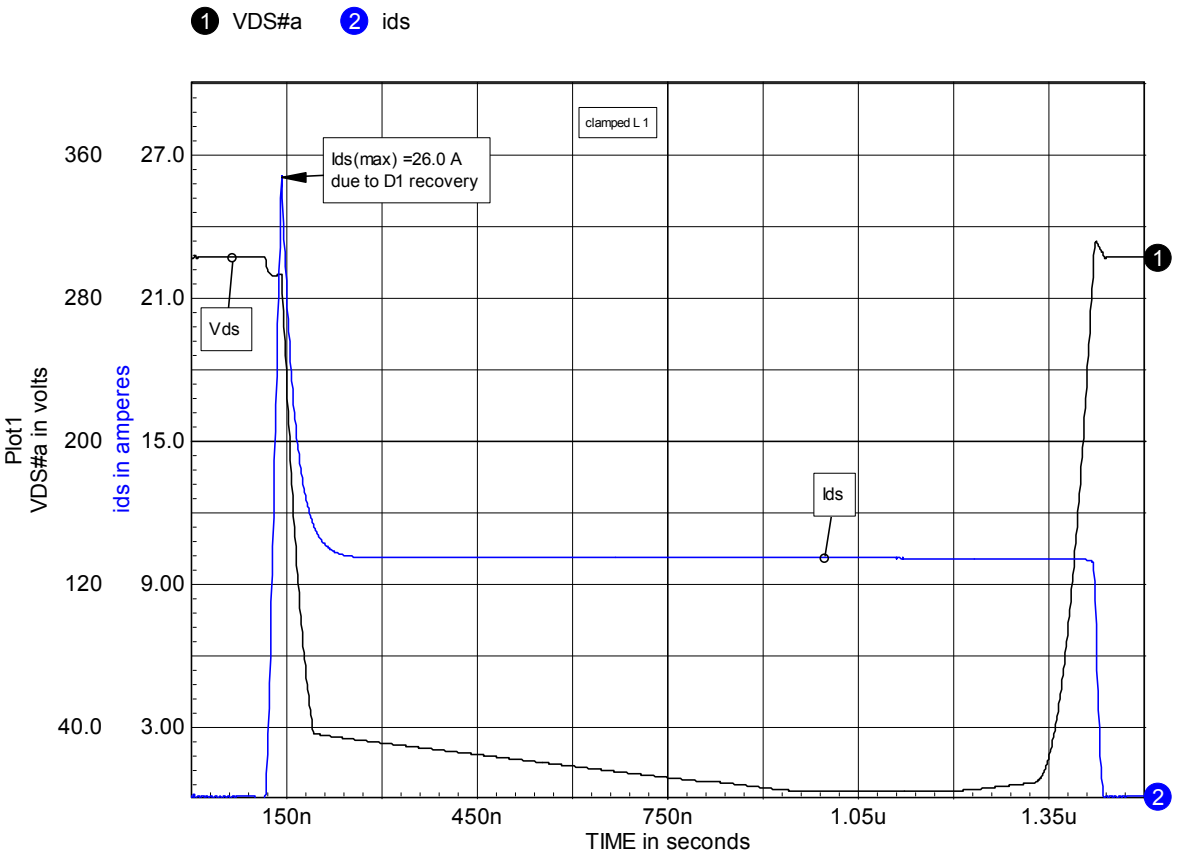


Figure 2-19, Switch waveforms with a real diode.

At turn-on there is a 26 A current spike due to the combination of input current and diode reverse recovery current. The peak power at turn-on is now about 7.8 kW. The use of a real diode leads to a drastically different load-line graph as shown in figure 2-20.

The turn-on current spike is large because of the rapid transition of the switch (high di/dt). If we slow down the switch, then this spike will decrease and the total switching loss may actually decrease. However, if we want to keep the switching time small then we will have to use some form of snubber to limit the diode reverse recovery di/dt.

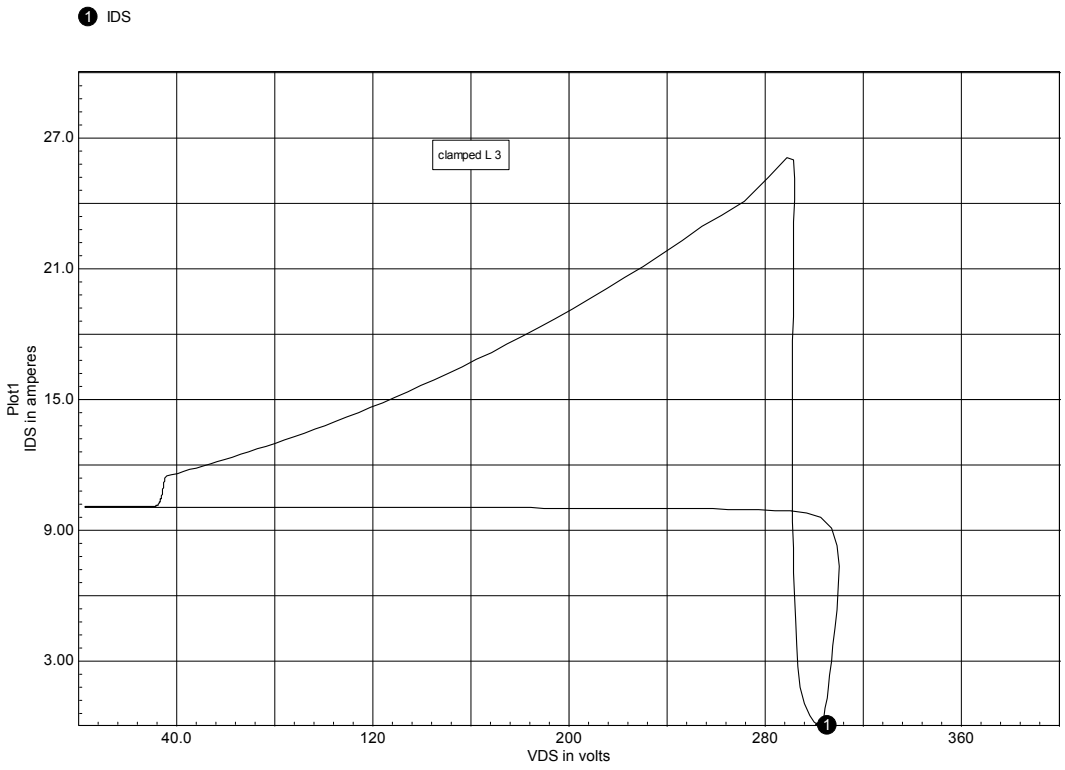


Figure 2-20, Clamped inductive switching load line with a real diode.

Unclamped inductive switching

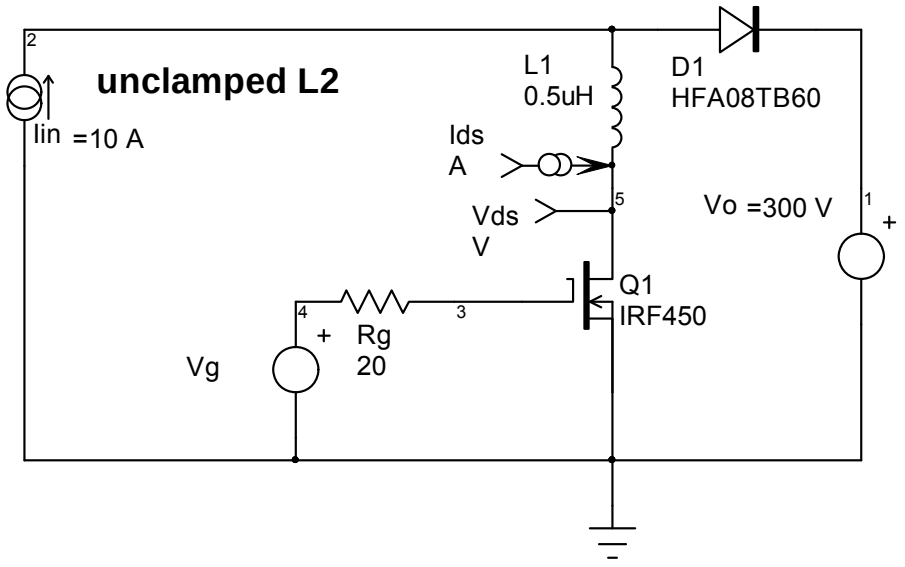


Figure 2-21, switch with unclamped inductance.

Any practical circuit will have some inductance in series with the switch. This can be due to both layout parasitic inductance and semiconductor package inductance. We can use the model in figure 2-21 to explore the consequences of adding this parasitic inductance.

A 500 nH parasitic inductance (L1) has been added in the switch drain. From this model we get the waveforms shown in figure 2-22.

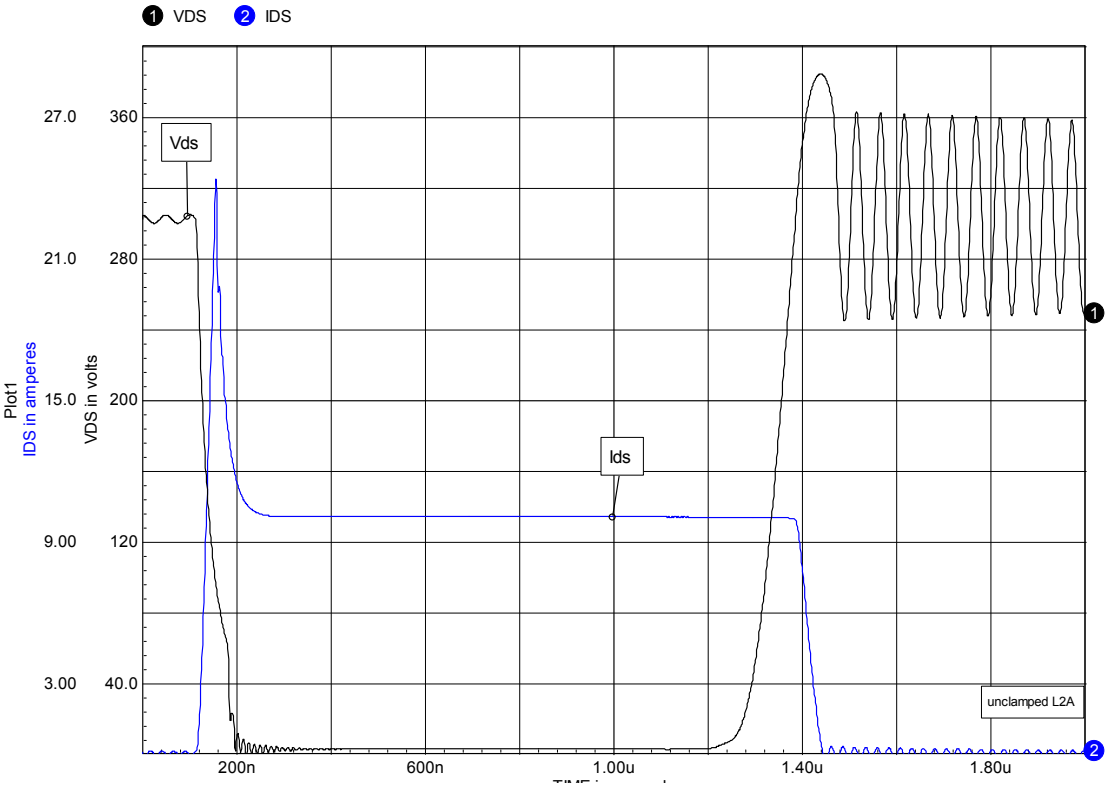


Figure 2-22, Vds and Ids waveforms with unclamped drain inductance.

Obviously the waveforms have changed. In some ways for the better but in others for the worse. Let's start by expanding the time scale during turn-on (figure 2-23) to take a closer look at this interval.

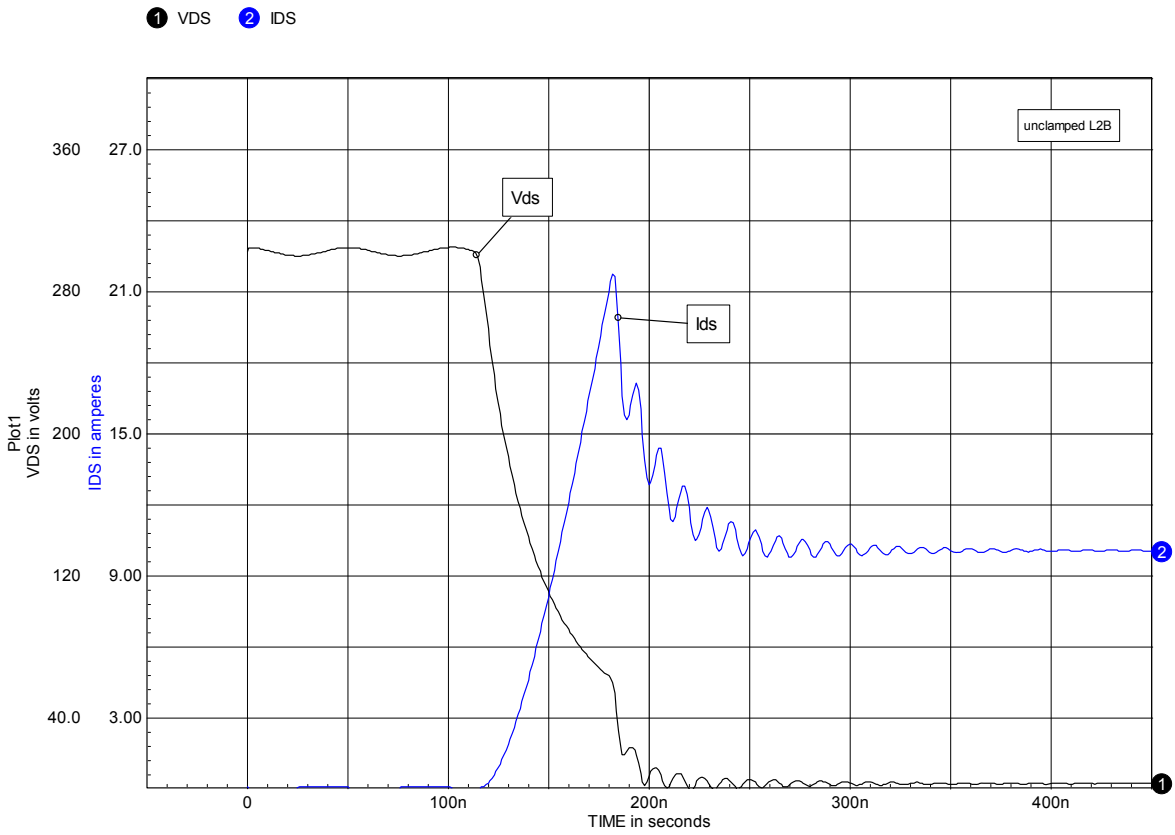


Figure 2-23, Ids and Vds at turn-on, expanded time scale.

Notice that Vds now begins to fall before Ids has reached it's maximum. The effect of L1 is to reduce the turn-on stress. The decrease in Vds is due to a voltage drop across L1 as Ids rises [V=L x d(Ids)/dt]. This is the basic principle of the turn-on inductive snubber. In this example L1 is also large enough to reduce the diode reverse recovery current spike, which is another feature of an inductive turn-on snubber.

While L1 helps at turn-on, at turn-off, a large ringing voltage spike is now present at turn-off. The ringing comes from the combination of the L1 and the output capacitance of the switch. If we want the benefits of L1 at turn-on we will have to add some network to the circuit to suppress the turn-off voltage spike. This will be dealt with in chapter 2.

The load-line graph associated with these waveforms is shown in figure 2-24.

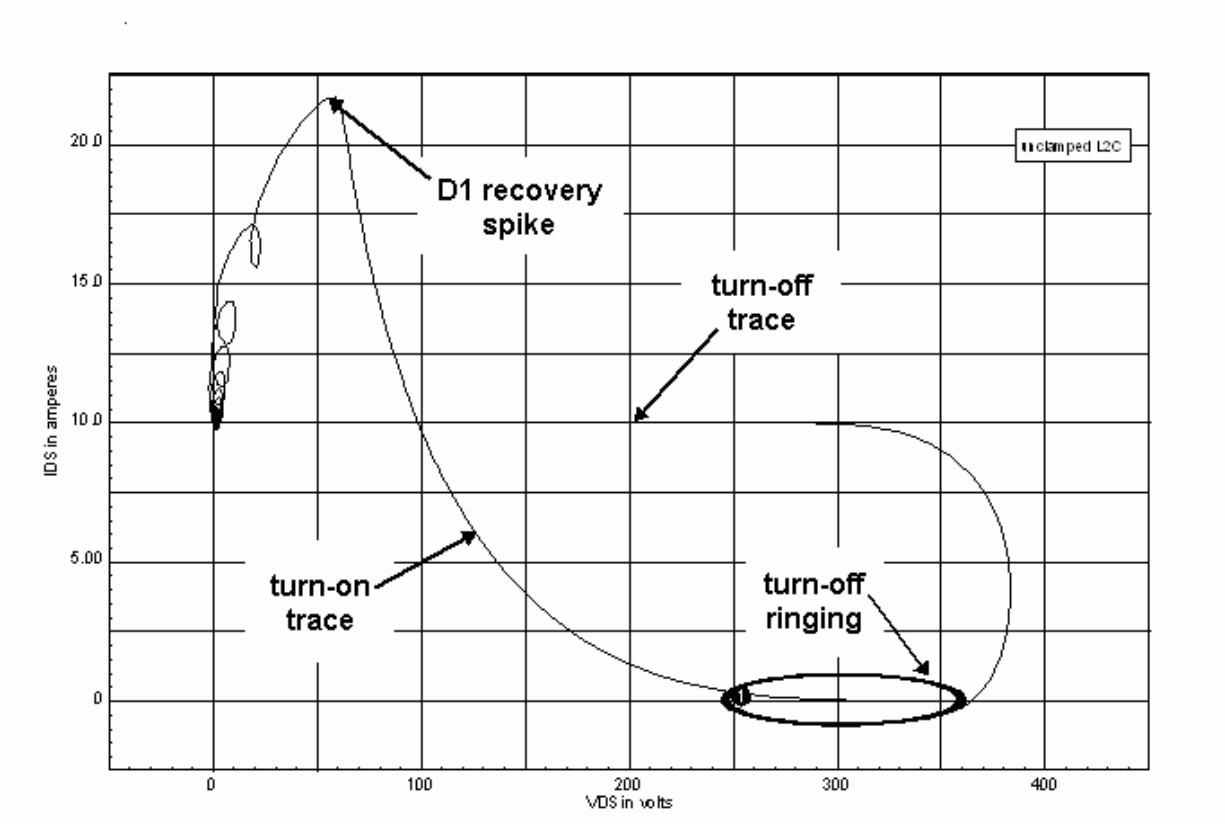


Figure 2-24, load-line graph with unclamped drain inductance.

During turn-on this load-line has greatly reduced stress, including a reduced diode recovery current spike. However, at turn-off we have a voltage spike and severe ringing. There is also ringing at turn-on after the point where D1 reverse recovery current has peaked and is falling. This is the point where D1 can support reverse voltage.

Capacitive switching

Capacitance is another common parasitic element. There will be the junction capacitance of the switches and diodes plus stray capacitance from the circuit layout, semiconductor package mounting, etc. We can examine the effect of shunt capacitance by adding C1 to figure 2-15, keeping the ideal diode, as shown in figure 2-25.

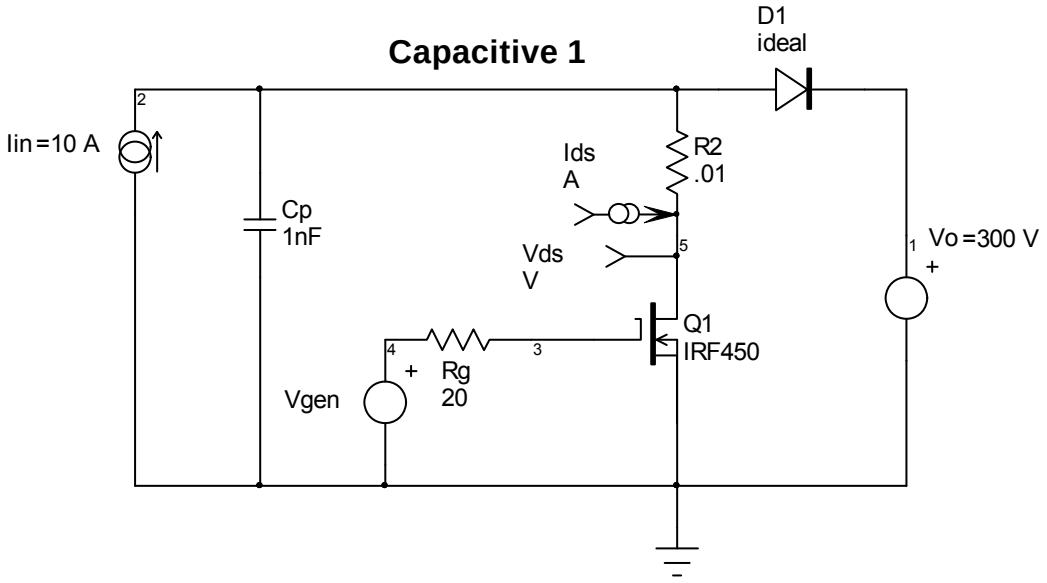


Figure 2-25, adding parasitic capacitance to the circuit.

The waveforms associated with this model are shown in figure 2-26.

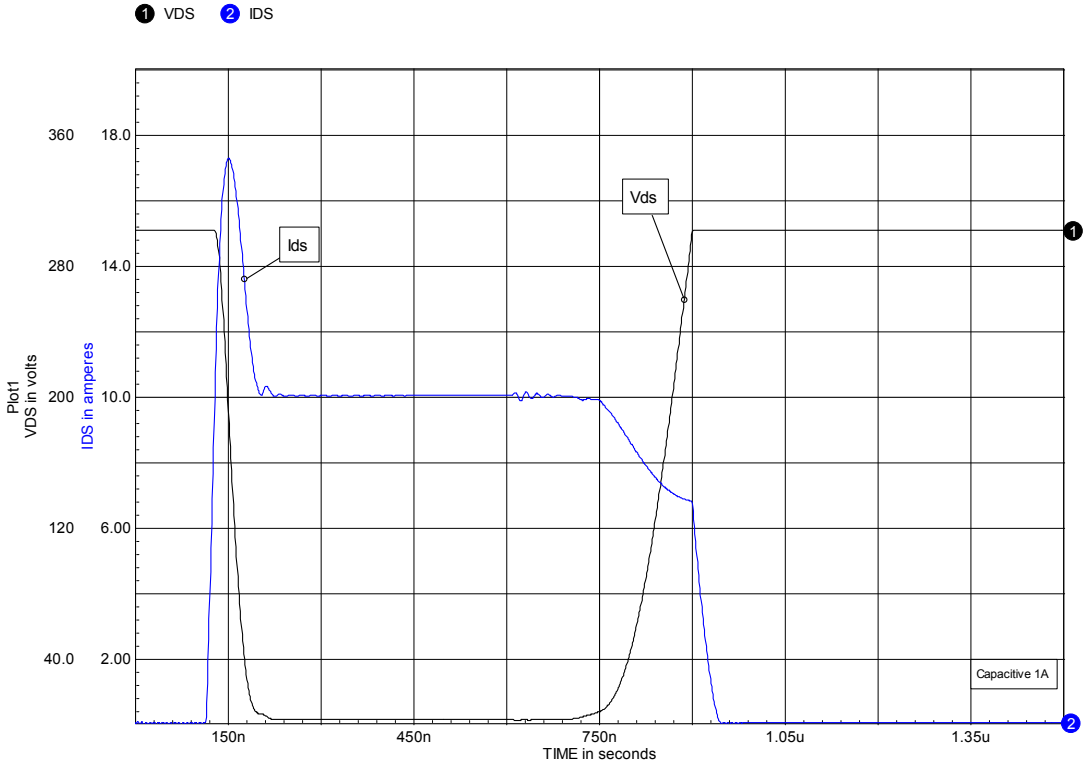


Figure 2-26, waveforms for capacitive load switching.

At turn-on there is a current spike due to the discharge of C1. Since the diode is ideal in this example, there is no reverse recovery current spike. In a circuit using a real diode then both current spikes would add together. The presence of parasitic capacitance creates additional stress at turn-on but it significantly reduces the stress at turn-off. Because the capacitance provides another path for current flow as the switch turns off, the switch current can now begin to fall immediately as V_{ds} begins to rise. For a sufficiently large value of capacitance, the turn-off stress can be reduced to near zero. Unfortunately this is achieved at the cost of higher turn-on stress and the loss of the energy stored in the capacitor. The effect of shunt capacitance is the basis for turn-off snubbers. In the case of a snubber however, some arrangement has to be made to control the turn-on current spike.

The load-line for this kind of switching is shown in figure 2-27.

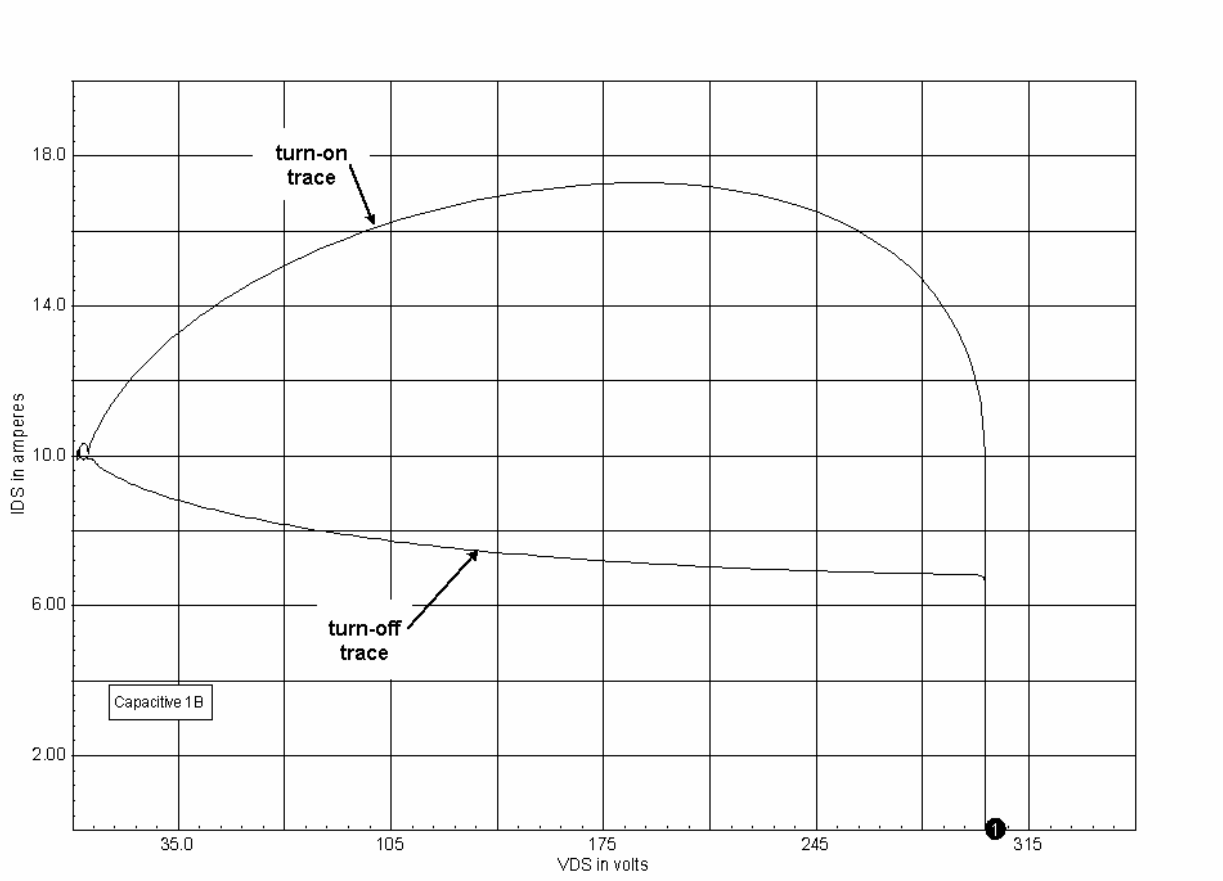


Figure 2-27, Load-line for capacitive load switching

Switching with real loads

In addition to the desired components, any practical circuit will have parasitic elements due the non-ideal character of desired components and the physical layout. Parasitics are generally unintentional but some are unavoidable. The use of good layout practices is a vital part of reducing parasitic elements.

> *The best practice is to minimize the parasitic inductances and capacitances due to the physical layout before employing snubbers. Clean up the circuit first, then add a snubber.*

The use of a snubber to remedy the effects of poor layout is a very bad practice.

Figure 2-28 extends the idealized circuit introduced in figure 2-15 to include typical parasitic elements.

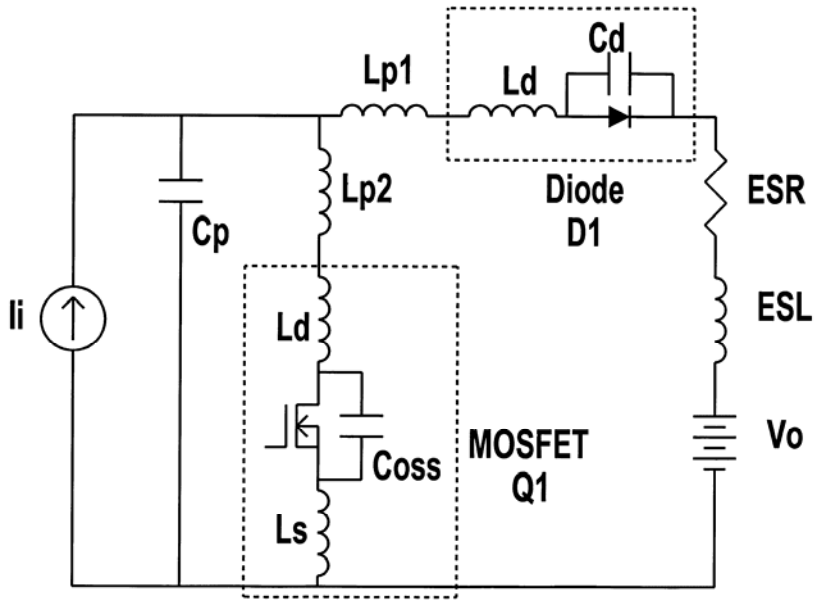


Figure 2-28, Typical parasitic elements in a converter circuit.

Let's take a moment and look at each of the parasitic elements:

- Cp represents the shunt capacitance of the input inductor and also stray capacitance of the interconnecting conductors between the input inductor,Q1 and D1.

- Lp2 is the wiring inductance associated with Q1.

- In Q1, Ld and Ls are the lead and bonding wire inductances within the device package. Coss is the output capacitance and may also include capacitance from a heat sink.

- Lp1 is the wiring inductance associated with the diode.

- In D1,Cd is the capacitance associated with the diode junction and Ld is the internal package inductance.

- The output filter capacitor will have both ESR (equivalent series resistance) and ESL (equivalent series inductance).

- In addition there will be stray capacitance associated with device heat sinks and transformer windings.

- Transformers usually introduce leakage inductance, which can be substantial.

Figure 2-28 is just a simple example. More complex circuits will have even more parasitic elements and these parasitics will play an active role in circuit behavior.

Effect of parasitics on circuit waveforms

To investigate their effect, we can add parasitic elements to a SPICE model as shown in figure 2-29. Note, D1 is now a real diode (an IR, HFA08TB60). Parasitic junction capacitances are not shown in figure 2-29 but are built into the device sub-circuits. Device models may also contain typical lead inductances internal to the package. The values chosen for the parasitics are reasonable approximations for a circuit of this power level but you should keep in mind that the values can be much larger in some circumstances. Particularly when transformers with leakage inductance are employed.

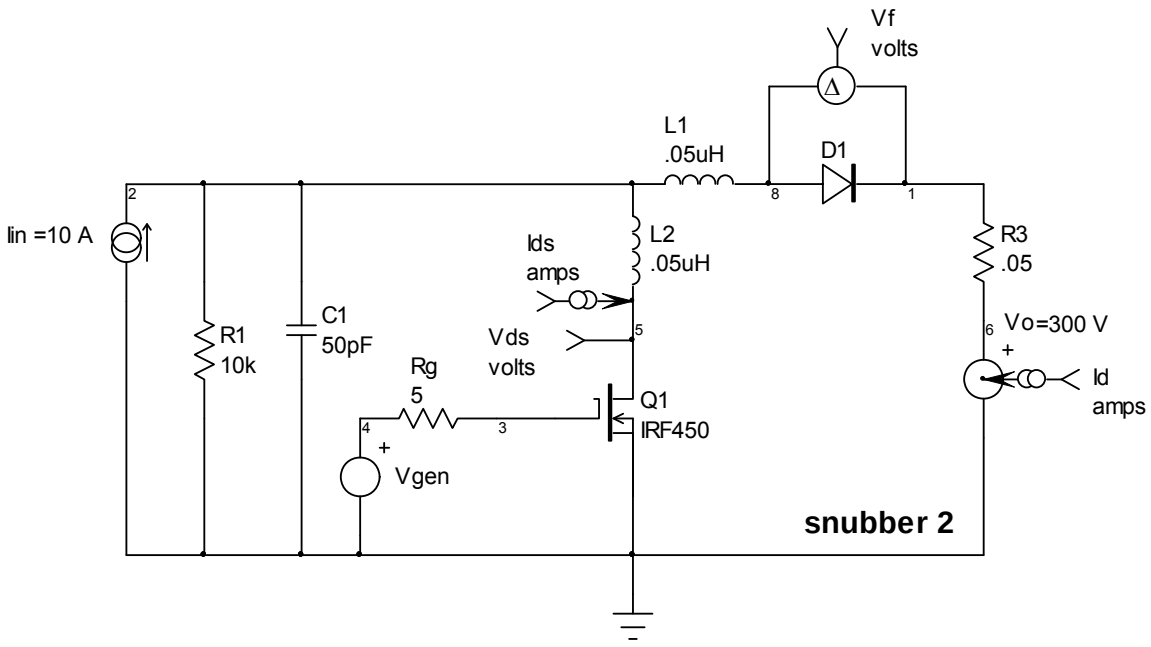


Figure 2-29, SPICE model with parasitic elements added.

A number of metering (V and I) points have been included in the model. This clutters up the schematic a bit but is very handy for deciphering circuit behavior. When modeling complex circuits extensive metering is often used.

Running the simulation, we get the waveforms shown in figure 2-30. The first thing we notice is the ringing in the turn-on current and turn-off voltage waveforms by the combination of the parasitic inductances (Lp) and capacitances (Cp). Looking a bit closer we can see the initial dip in Vds at turn-on and the Vds voltage spike at turn-off, are both caused by Lp. At turn-on the diode reverse recovery spike on Ids is present and at turn-off we can see the effect of Cp on Ids.

The Q1 waveforms don't look all that bad but when we look at the voltage waveform across D1 shown in figure 2-31, things don't look good at all.

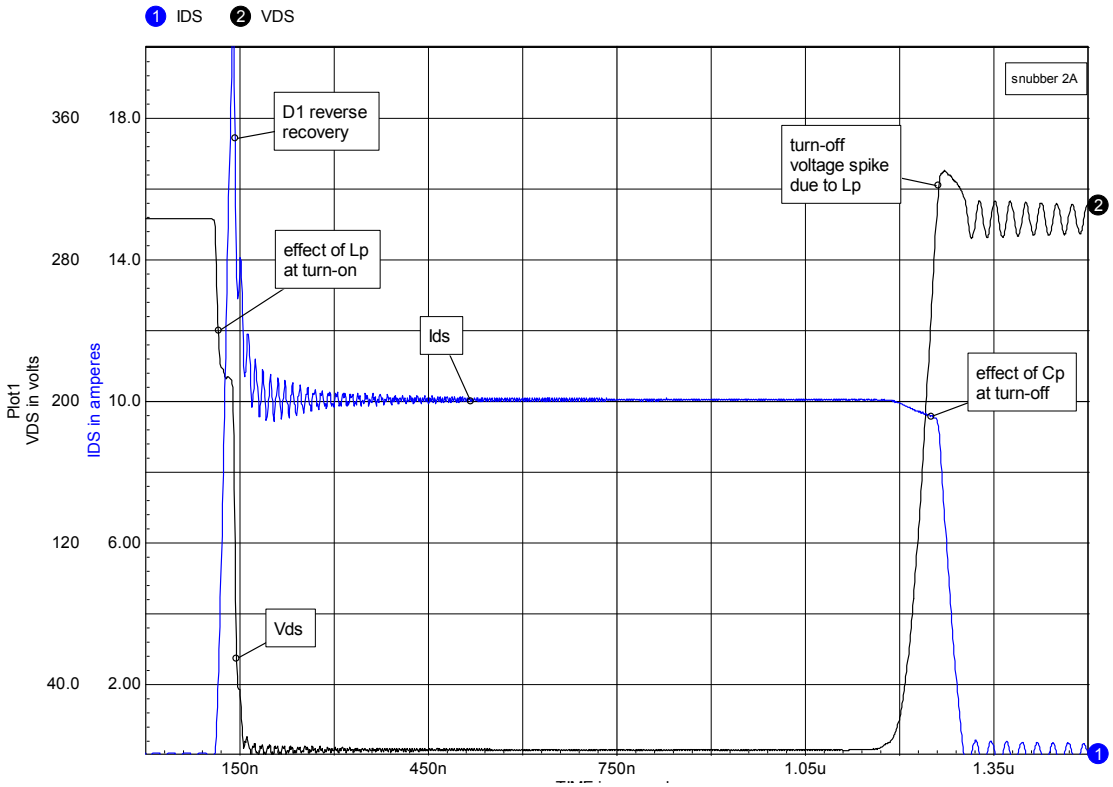


Figure 2-30, Q1 Vds and Ids waveforms.

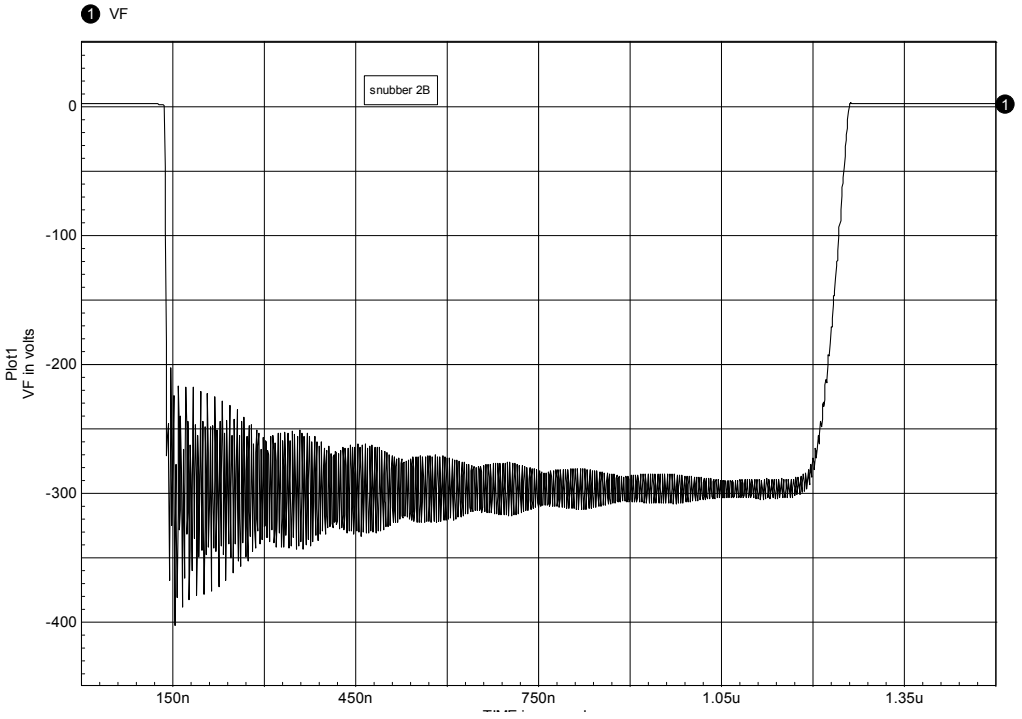


Figure 2-31, D1 voltage waveform.

The amplitude of the voltage ringing is large and has simultaneous ringing at two frequencies. This is not too surprising since the overall circuit has multiple inductances and capacitances: i.e. it is a multipole network. In an ideal circuit the diode reverse voltage would be 300 V but the overshoot here is about 100 V above that. This waveform needs be damped to reduce diode stress and EMI.

What would happen if L2 were even larger, say 500 nH? This would be possible in a circuit with transformer leakage inductance in series with the switch or even excessively long leads to Q1 and D1.

Figures 2-32 and 2-33 show the impact of increasing L2 from 50 to 500 nH. The voltage and current ringing are now very large and continue during the entire switching cycle. D1 reverse voltage risen to almost 1 kV and there is a 120 V turn-off spike on Vds. Clearly parasitic inductance is something we want to minimize!

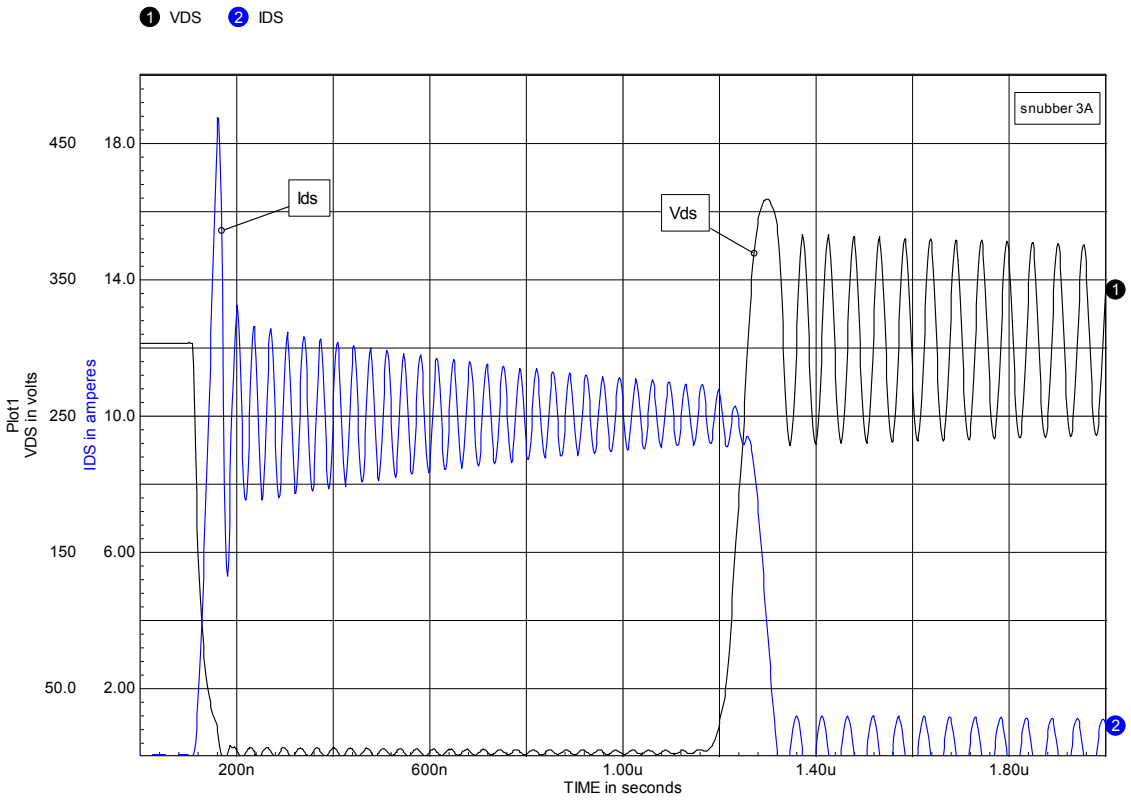


Figure 2-32, Q1 Vds and Ids waveforms with L2=500 nH.

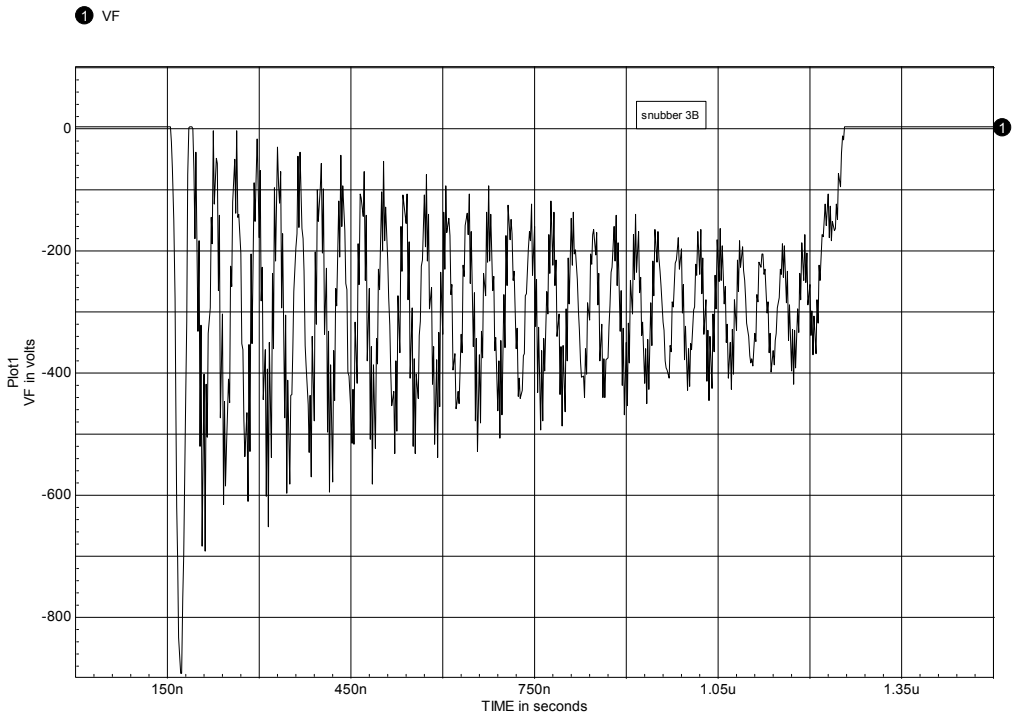


Figure 2-33, D1 voltage waveform with L2=500 nH.

Unintentional overlapping conduction in switches

A very common problem in circuits containing more than one switch is simultaneous conduction of two or more switches at a time when this is not desired. Switches have four operating states: on, off, transition from off-to-on and transition from on-to-off. Generally the problem falls into one of two categories. The first case is where some other switch in the circuit is triggered on inadvertently while one switch is in full conduction. This is frequently a problem in thyristor circuits due to undesired dV/dt induced turn-on and it can lead to catastrophic failure of the switches. The second and more common case is where a second switch begins to turn-on while a first switch is still in transition from on-to-off. How serious this is depends on where in the individual turn-on/turn-off transitions the two switches are. The consequences can range from a modest increase in loss to device destruction. Usually we try to design the circuit so that these two cases cannot occur in any normal operating mode but we are not

always successful. Snubber circuits can be used to mitigate the effects of these kinds of events.

A very common example of overlapping conduction is the reverse recovery current spike through a diode. The diode is a switch which may very well be conducting when another switch is turned on. The result as we have already seen, can be a large current spike in both switches.

The same problem can occur when two active switches are used. This can be illustrated using the model in figure 2-34.

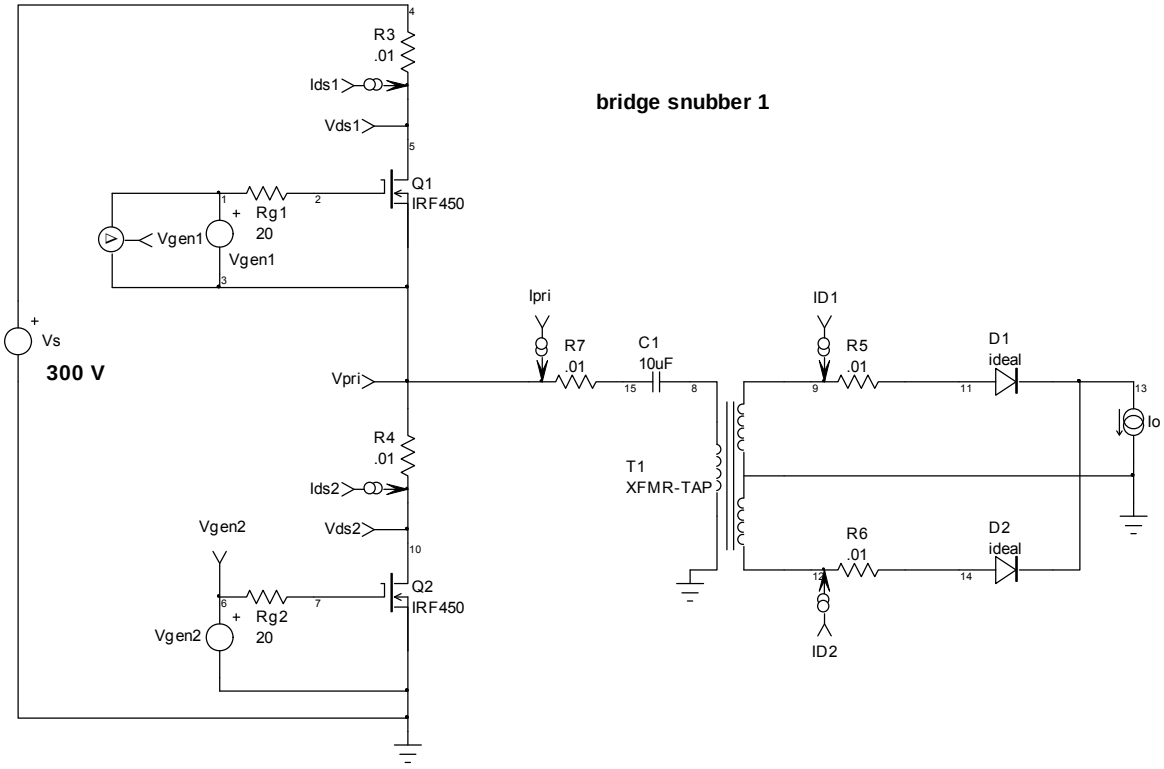


Figure 2-34, idealized half-bridge converter circuit.

In this circuit Q1 and Q2 conduct alternately. A dead-time is usually built into the drive waveforms to assure that both switches are not on simultaneously. Typical Ids waveforms for Q1 and Q2 are shown in figure 2-35, where the dead-time is very evident.

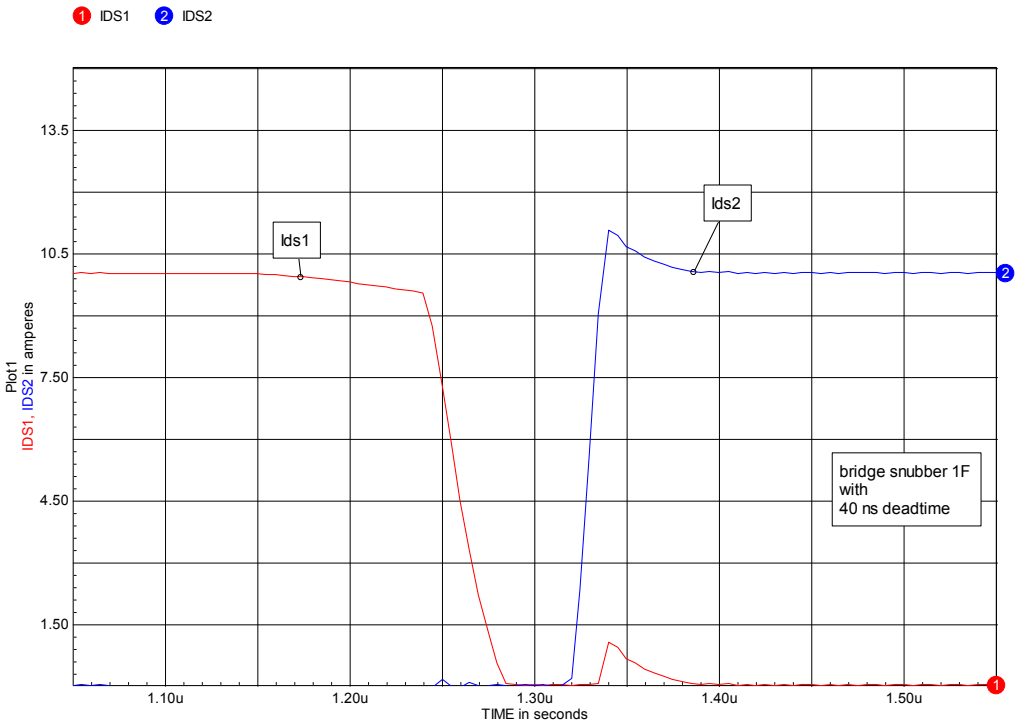


Figure 2-35, normal Ids waveforms for Q1 and Q2.

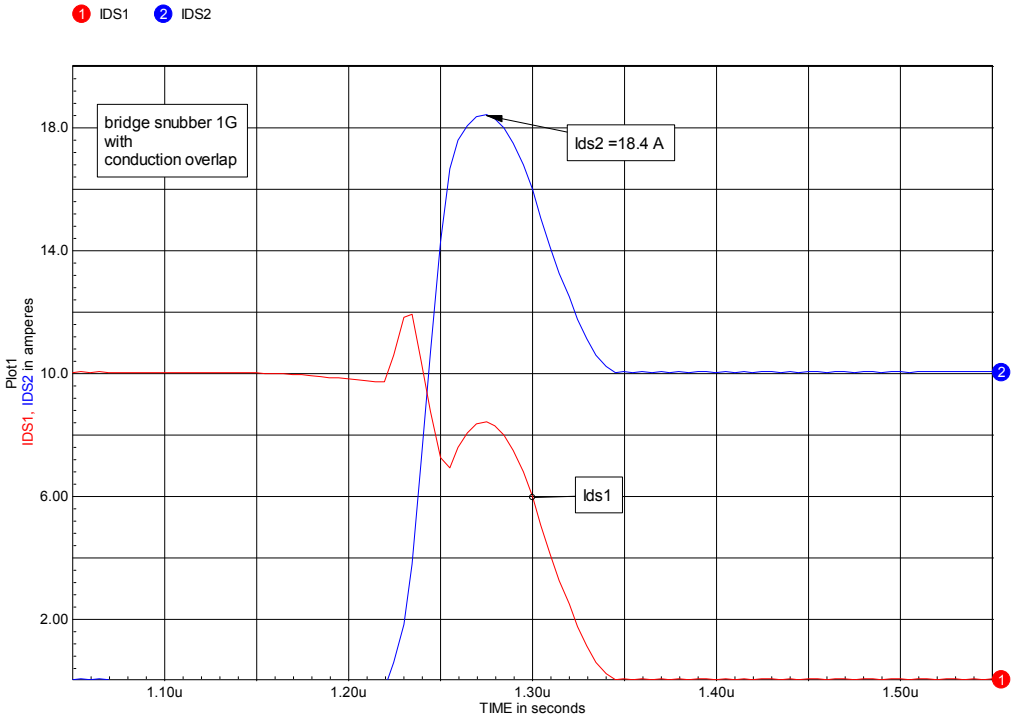


Figure 2-36, an example of Ids1 and Ids2 waveforms during conduction overlap.

Suppose however, that the dead-time is not sufficient and there is conduction overlap. An example of this is given in figure 2-36.

When overlapping conduction is present, the power dissipation in each switch may be quite high, as shown in figure 2-37.

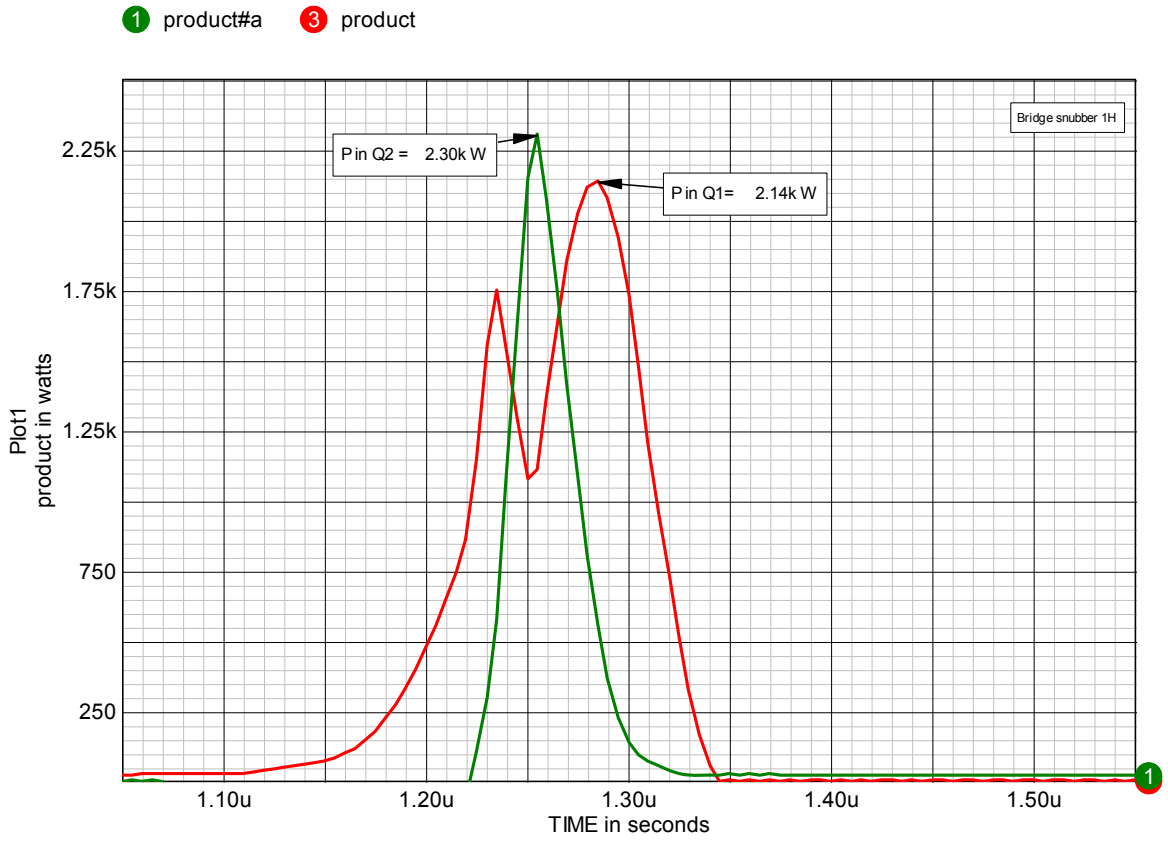


Figure 2-37, power dissipation in Q1 and Q2 during Q1 turn-off.

While this kind of overlapping conduction is usually attacked by providing ample dead-time, due to component variations that is not always successful. One reason is the need to maximize the switch duty cycle to improve overall circuit efficiency. This can lead to making the dead-time too short for worst case component and temperature variations. While the first line of defense is adequate dead-time, an inductive turn-on snubber can provide additional protection.

Lack of desired overlapping conduction

The converter circuits in which we typically worry about overlapping conduction are for the most part derived from the buck topology. However, there is another entire class of converter topologies[387] which are derived from the boost topology. Multi-switch versions of these circuits usually require that at least two switches be in simultaneous or overlapping conduction. The problem which arises when the switch conduction fails to overlap is the dual[387] to the overlapping conduction problem in buck derived converters. You get a voltage spike during switch transitions rather than a current spike. This problem is just as undesirable as the current spike and is usually controlled by careful attention to the switch drive waveforms. For abnormal operating conditions and from reliability considerations, some form of snubber or voltage clamp is usually employed to protect the switches in these topologies.

Chapter 3

RC -snubbers

An RC-snubber, or damping network as it is sometimes called, consisting of a series R and C is by far the most commonly used snubber. One would think that designing such a snubber would be easy but to do it analytically turns out to be not so simple. The problem is that the snubber is usually imbedded in a complex multi-element network with several inductances and capacitances, most of them parasitic, some varying with voltage. This makes closed analytic solutions intractable for the purposes of day-to-day design work. In addition, it is necessary to use some judgment in choosing what peak voltages and/or currents are acceptable and also acceptable losses.

The approach adopted here is a combination of simple analytic models, approximations which lead to a good "first guess" and some final adjustment in the actual circuit. This is not a very elegant method but it usually converges quickly to an acceptable solution. Those interested in a more analytic approach, are referred to the classic paper by McMurray[287] and in this section we will use some of the results of Dr. McMurray's paper. The McMurray paper is a good example of the analysis complexity for even simple cases.

Examples of RC-snubber use

To illustrate the use of an RC-snubber we'll take a look at damping the ringing voltage waveform across D1 which was shown in chapter 2 (figure 2-31). We will modify the model in figure 2-29 by adding an RC-snubber (Rs & Cs) across D1 as shown in figure 3-1. For the moment we will use some typical values for Rs and Cs without explanation because I just want to demonstrate the general behavior of an RC snubber. A bit later we'll see how the values for Rs and Cs are determined in a particular application.

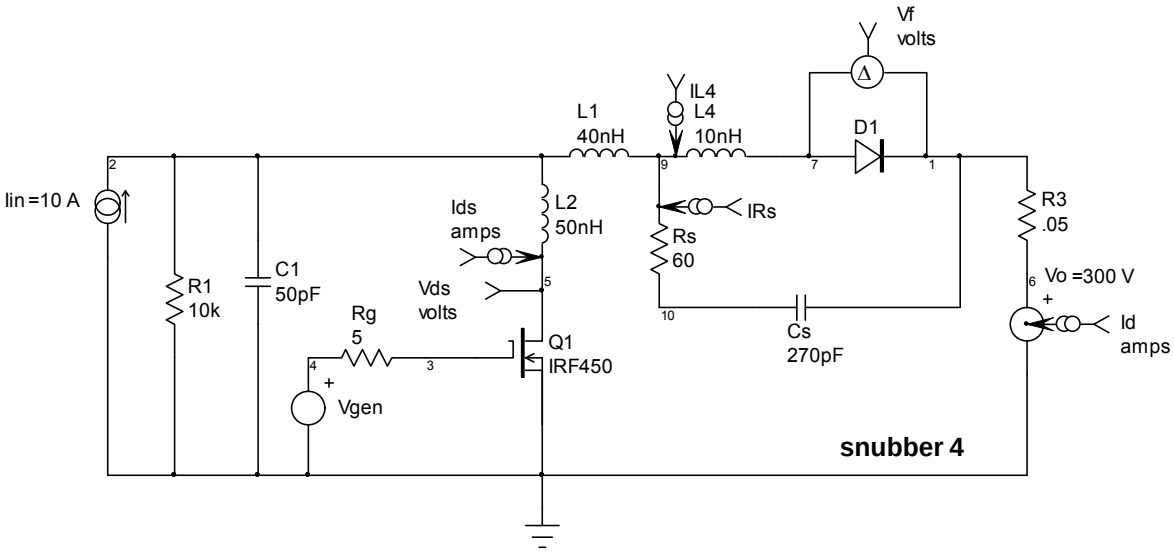


Figure 3-1. RC-snubber across D1.

Note that L1, in figure 2-29, has been divided into L1 and L4 in figure 3-1 to simulate the effect of package inductance: i.e. the snubber is across the outside of the package and not directly across the diode junction. The associated Vds and Ids waveforms are shown in figures 3-2 and 3-3.

Comparing figures 2-31 and 3-2 (figure 2-31 is repeated here for convenience), it is clear that the voltage waveform across D1 has been dramatically improved. This is a very good example of just how useful simple snubbers can be and why they're so popular.

Comparing figures 2-30 and 3-3, the improvement is not so dramatic. The Q1 turn-on current and voltage ringing are gone but the effect at turn-off is hardly detectable. But there is an important difference in the Ids current spike at Q1 turn-on, it is somewhat wider. This is addition current in Q1 at turn-on is due to the charging of Cs, through Rs and Q1, at Q1 turn-on. This increase in turn-on current is one of the undesired "side-effects" which appear when a snubber is added to the circuit.

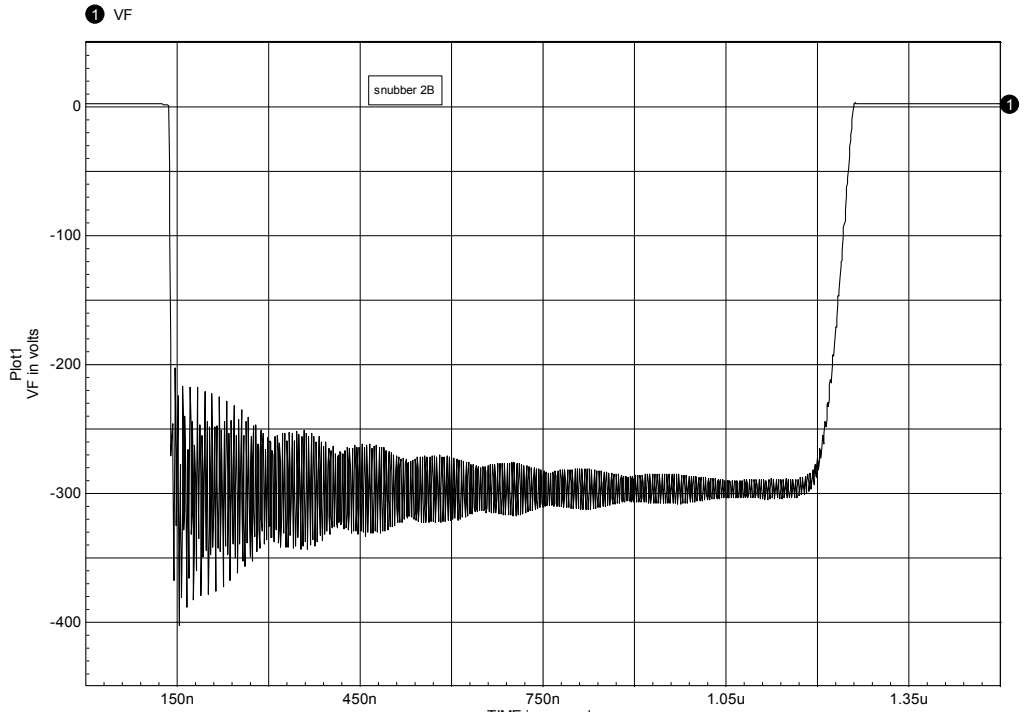


Figure 2-31, D1 voltage waveform.

Figure 3-2, D1 voltage waveform with snubber across D1.

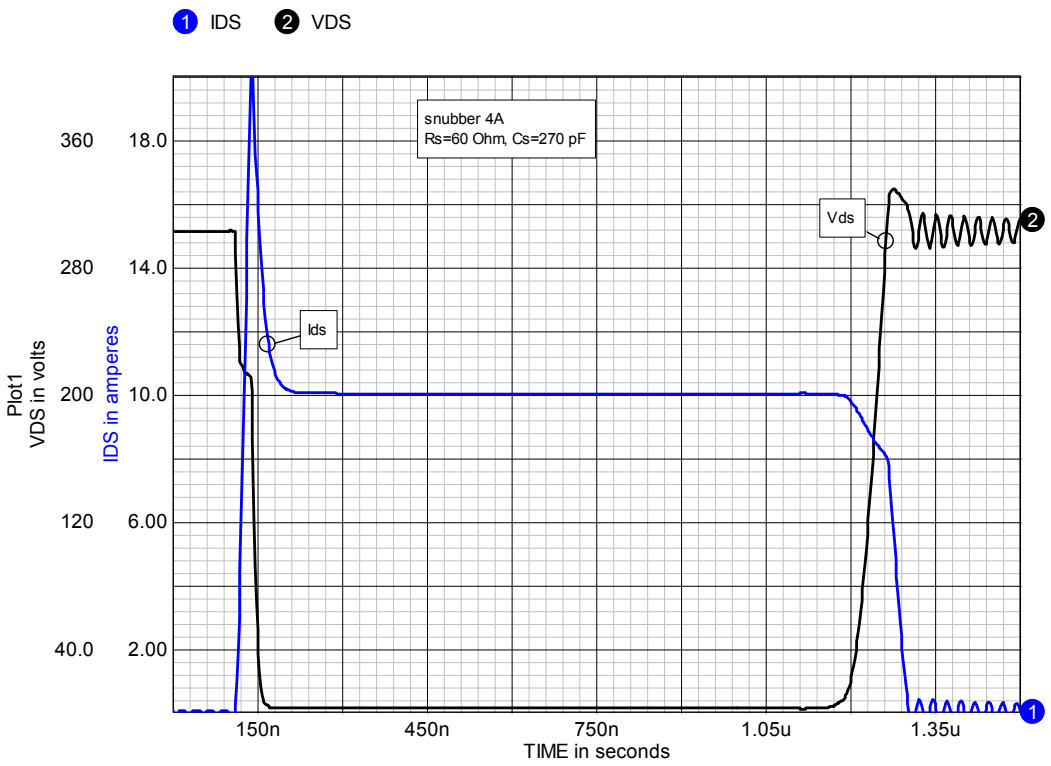


Figure 3-3, Q1 Ids and Vds waveforms with a snubber across D1.

In steady state, when Q1 is off and D1 is conducting, Cs will be discharged essentially to zero. While Q1 is on, Cs is charged to Vo=300 V through Q1 and when Q1 turns off and D1 turns on, Cs is discharged back to zero through D1. Figure 3-4 shows the current waveform in Rs and Cs as Q1 turns on and off.

The current in Cs consists of short, high amplitude pulses, with a substantial RMS value, which can stress the snubber capacitor. Pulsed current waveforms with high peak and RMS values are typical of many snubber circuits. This is why snubber capacitors must be carefully chosen. Choices for snubber capacitors are discussed in chapter 6.

The current pulse associated with Q1 turn-on flows in Q1 and adds to the D1 reverse recovery current spike. This can be seen more clearly in figure 3-5 which gives the current waveforms in L4 and Rs and their sum, which is the current spike in Q1 at turn-on.

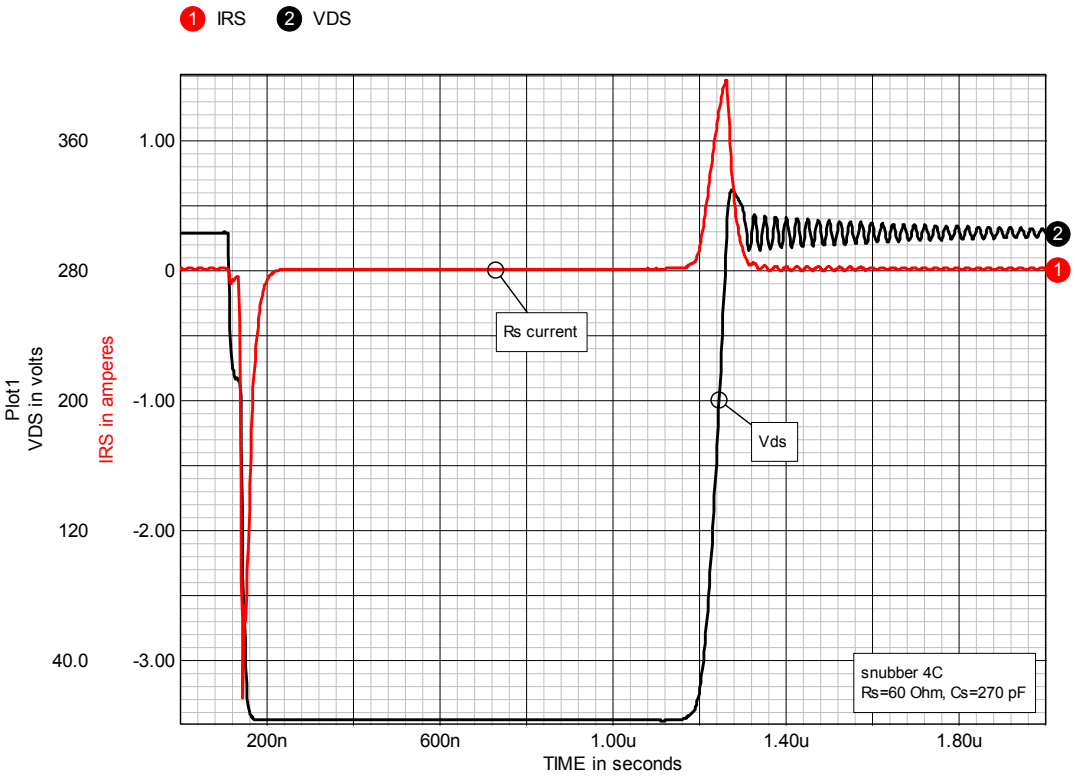


Figure 3-4, snubber current waveform.

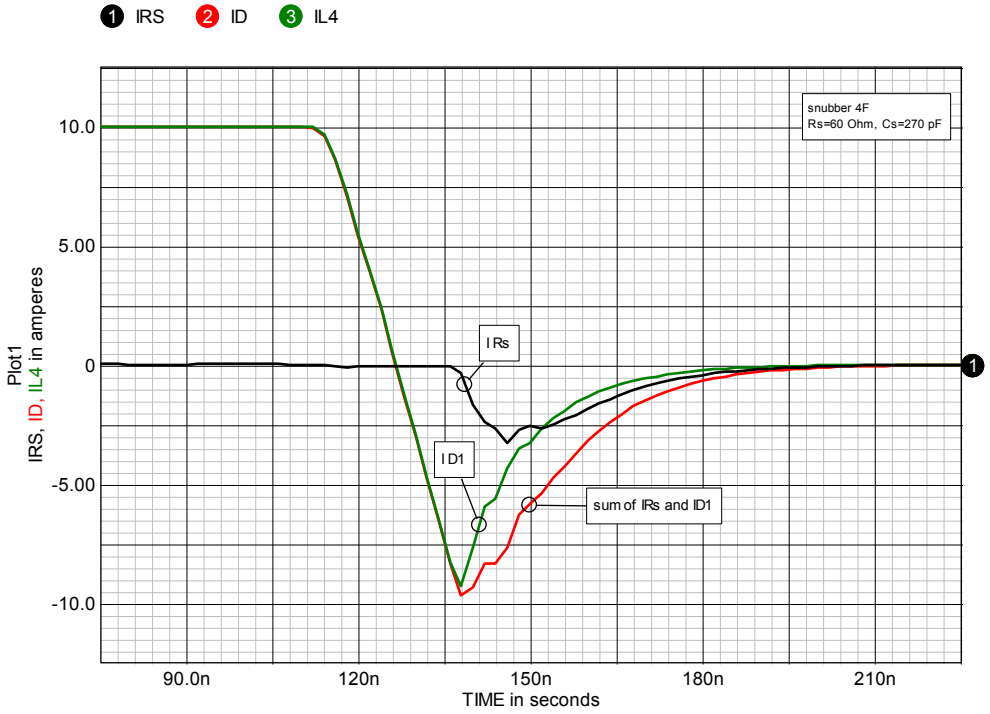


Figure 3-5, components of Q1 Ids turn-on current spike.

The wider turn-on current spike in Q1 is due to the addition of the Cs charge current to the D1 reverse recovery current.

The peak amplitude of Ids is directly related to the value for Rs, the larger we make Rs the smaller the spike will be. But, as we will see shortly, there will be an optimum value for Rs which gives the most effective damping and/or the smallest peak voltage. Sometimes we may have to select a compromise value for Rs which trades lower peak current for somewhat higher peak voltage.

The important lesson here is that while the snubber suppresses the ringing across D1, and reduces some ringing elsewhere in the circuit, it introduces additional current stress on Q1. The introduction of new current or voltage stresses is a typical consequence of adding a snubber to a circuit. This has to be taken into account when designing snubbers. There is no free lunch! It is possible however, to design snubbers with auxiliary switches which add little or stress to the power switches[27,45,116,123,150,157,185,190,254,278,438].

Another effect of adding a snubber, is the power dissipation in Rs. When Cs is discharged through D1 essentially all the energy (U_1) stored in Cs will be dissipated in Rs. When Q1 turns on and Cs is recharged, energy will again be dissipated in Rs. As a result, the energy loss per switching cycle will be:

$$2U_1 = CsV^2 \qquad (3\text{-}1)$$

The power dissipation in Rs (P_{Rs}) will depend on the switching frequency (f_s):

$$P_{Rs} = CsV^2 f_s \qquad (3\text{-}2)$$

Adding the snubber introduces loss. It may be that some other losses will be reduced but this loss is still a matter of concern. The larger we make Cs the greater will be the beneficial effect of the snubber but also the greater will be the loss introduced by the snubber. Typically we try to choose a value for Cs which is the minimum that gets the job done, although as shown in chapter 7 (see figure 7-11 and associated text), sometimes it is desirable to reduce the switch loss at the price of increased loss in Rs.

As we've just seen, adding an RC-snubber across D1 only partially reduces the ringing waveforms associated with Q1. Let's shift the snubber from D1 to Q1 as shown in figure 3-6 and examine the effect on the circuit waveforms. In this example we have made Cs larger (1 nF) and reduced Rs to 30 Ohm.

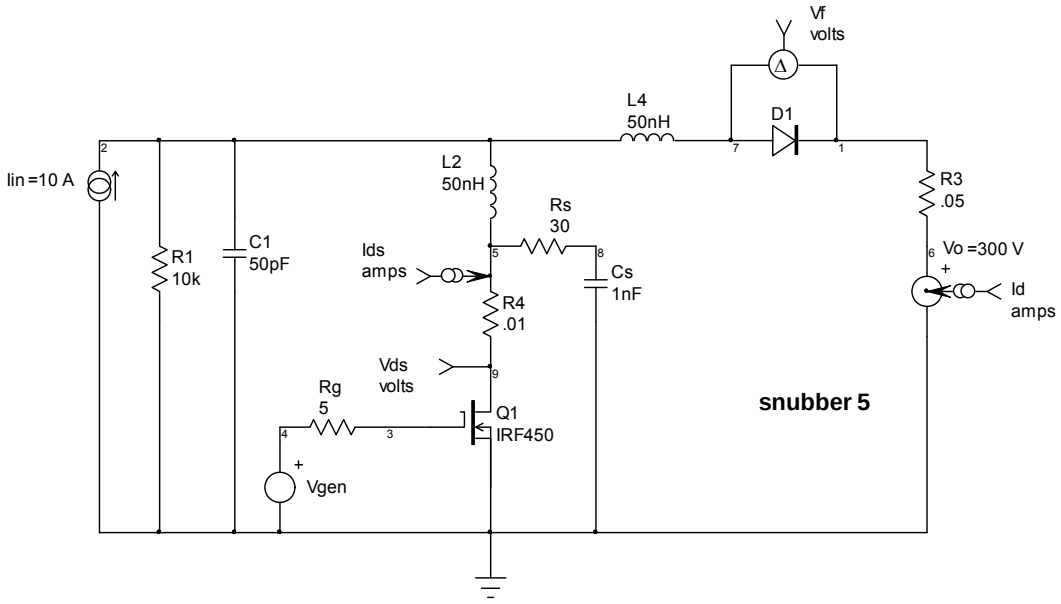


Figure 3-6, RC-snubber across Q1.

The waveforms associated with Q1 are shown in figure 3-7. Comparing the waveforms in figures 2-30 (repeated here for convenience) and 3-7, we see that the primary effect of placing the snubber across Q1 is to damp the voltage ringing at turn-off but there is not much effect on the turn-on current ringing. Note also that at Q1 turn-off Ids now begins to fall before Vds reaches Vo. This reduces Q1 loss.

The voltage waveform across D1 is shown in figure 3-8. Comparing figures 2-31 and 3-8, we see that the D1 voltage ringing is reduced with the snubber across Q1 but not by nearly as much as when the snubber was across D1. Typically there are multiple inductances and capacitances in the circuit and you will very likely have to use more than one RC-snubber. Because there will be some interaction between snubbers, you may have to juggle the component values to get the desired effect with minimum power loss.

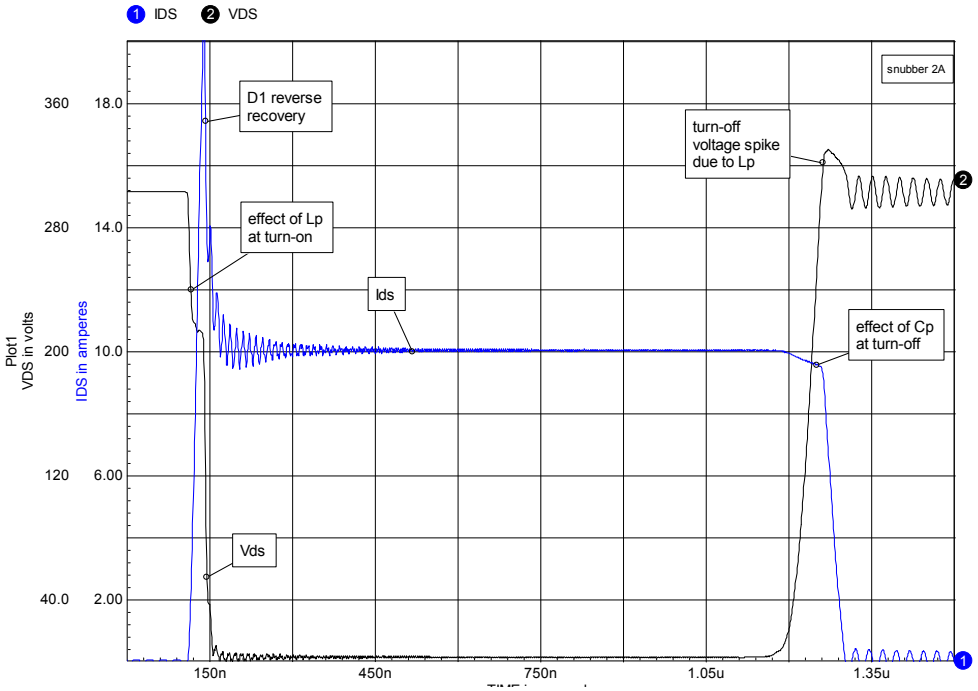


Figure 2-30, Q1 Vds and Ids waveforms.

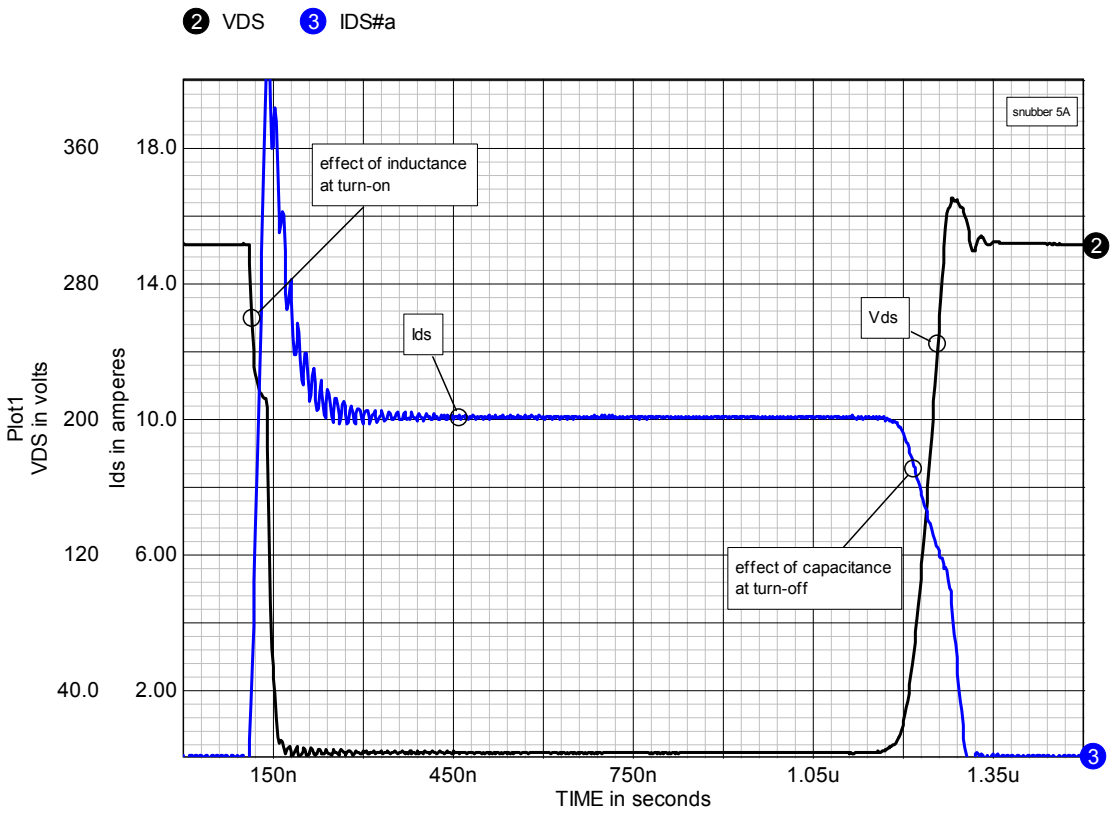


Figure 3-7, Q1 waveforms.

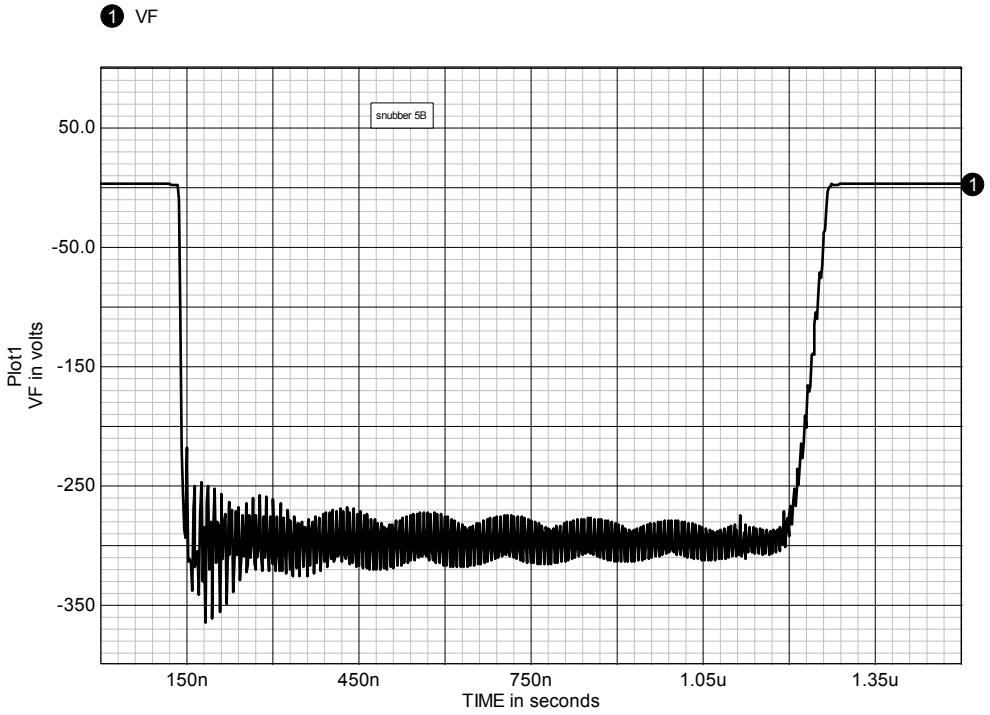


Figure 3-8, voltage waveform across D1.

We've just seen an overview of how the RC-snubber works and how it might be applied in a given circuit. Now we need to look in much greater detail to see how to design such a snubber for a given application.

A closer look at RC-snubber behavior

An RC-snubber is usually used to limit the peak voltage (V_p) across a device and/or to damp an oscillatory waveform. In most cases limiting V_p will result in adequate damping so in the following discussion we will make limiting V_p our primary goal but keep an eye on waveform damping as we go along.

The discussion will begin with simple, idealized models which illustrate circuit behavior. Then components will be added making the model more realistic to show the effect of additional parasitic elements and the finite switching times of real devices. We'll end up with the circuit in figure 3-6 except that L2=500 nH, a reasonable value if there is some transformer leakage inductance present.

We will start with the simple R-L-C circuit shown in figure 3-9. The network represents the circuit state (of figure 3-6) just after the Q1 has turned off, with L2 representing parasitic drain inductance, Vo represents the output voltage to which the end of L2 (at node 4) is clamped through D1, Io is the current in L2 at t=0 and Rs-Cs represent the snubber. What we're interested in is the waveform for Vds as we vary Rs and Cs.

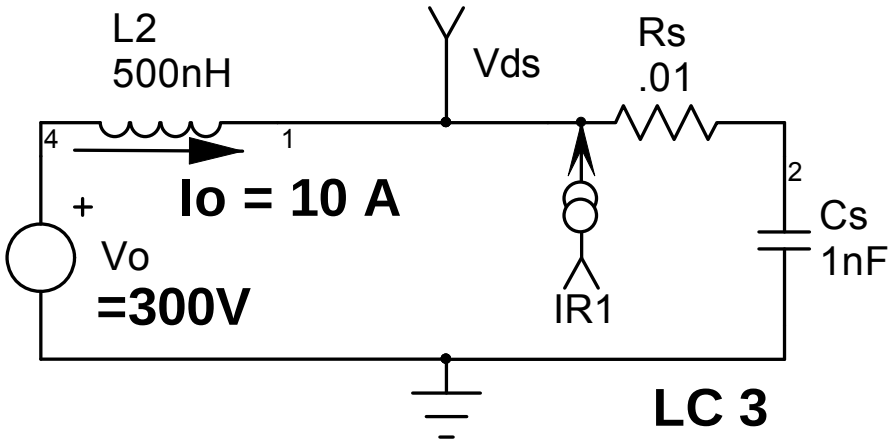


Figure 3-9 Equivalent circuit just after Q1 turn-off

If Rs=0, then we can predict the peak value for Vds from[287] from the following expression:

$$\frac{V_{ds}}{V_o} = 1 + \sqrt{1 + \left(\frac{I_o}{V_o}\right)^2 \left(\frac{L2}{Cs}\right)} = 1 + \sqrt{1 + \left(\frac{I_o}{V_o}\right)^2 Z_o^2} \qquad (3\text{-}3)$$

For the values given in figure 3-9, V_p = 674 V (from equation 3-3).

That's for Rs very small. What if we let Rs=67.4 Ohms? The waveforms for these two values of Rs are shown in figure 3-10.

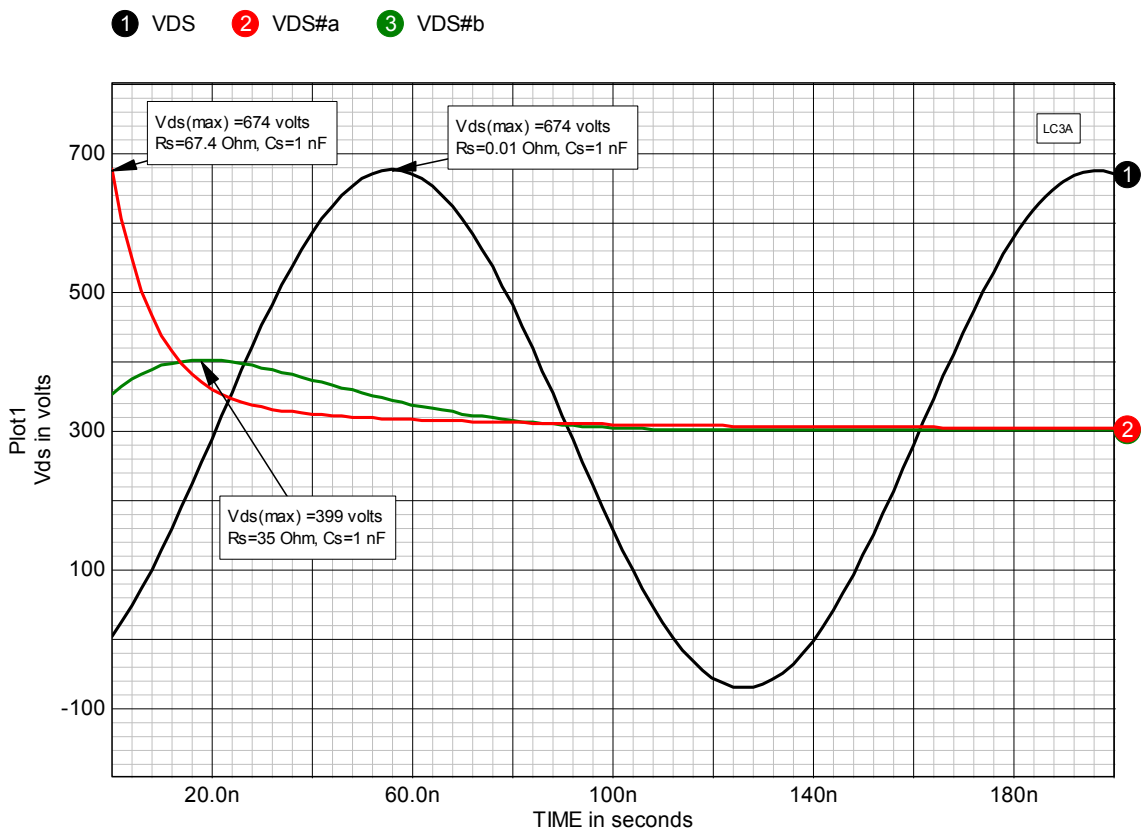


Figure 3-10, Vds waveform for different values of Rs.

For Rs=0, V_p=674 V as predicted from equation (3-3) and the waveform is undamped. On the other hand, for Rs=67.4 Ohm, V_p =Io*64.7 = 674 V, which is no improvement in V_p but the waveform is now very well damped. If we make Rs larger, V_p will only increase which is not what's wanted. We want to decrease V_p. Suppose we make Rs=35 Ohm. The effect of this on V_p is shown by the third waveform in figure 3-10. Now V_p=399 V which is a reduction of 275 V.

The point of this exercise is to show that there will be some optimum value for Rs, between zero and 67 Ohms, which gives the minimum value for V_p. Given that the maximum voltage rating for an IRF450 is 500 V and normal practice would be to derate by 20% (to 400 V), V_p=399 V is a safe value. If we adjust the value of Rs a bit we will find that the Vds minimum is quite broad and 35 Ohm is pretty close to the best choice we can make for that particular value of Cs. If we want to reduce V_p further we'll have to use a larger value for Cs.

We'll examine the choice of Cs shortly but first we need to generalize how we find the optimum Rs for a given choice of Cs and parasitic values.

Finding the optimum value for Rs

Besides cut-and-try in SPICE, how do we find the optimum value for Rs? At the very least we need a way to make a good initial guess.

The ringing frequency (f_o) for the network in figure 3-9 is:

$$\omega_o = 2\pi f_o = \frac{1}{\sqrt{L2Cs}} \quad (3\text{-}4)$$

The characteristic impedance (Z_o) of the network is defined by:

$$Z_o = \sqrt{\frac{L2}{Cs}} \quad (3\text{-}5)$$

For the values of Vp/V_0 normally acceptable ($Vp/V_0<2$), the optimum value for Rs will be in the following range:

$$Z_o \leq Rs \leq 2Z_o \quad (3\text{-}6)$$

A detailed exposition can be found in McMurray[287]. For V_p/V_o values close to 2, Rs optimum will be close to Z_o. However, it is more common to have Vp/Vo < 1.4 which moves the optimum value for Rs above 1.5 Z_o. Choosing Rs = 1.5 Z_o is usually a good starting point.

Using the values in figure 3-15, Z_o = 22.4 Ohm. Experimentally we found the optimum value for Rs = 35 Ohm, so Rs = 1.6 Z_o. In this case Vp/Vo =1.3.

The effect of different values for Rs on Vp is shown in figure 3-11.

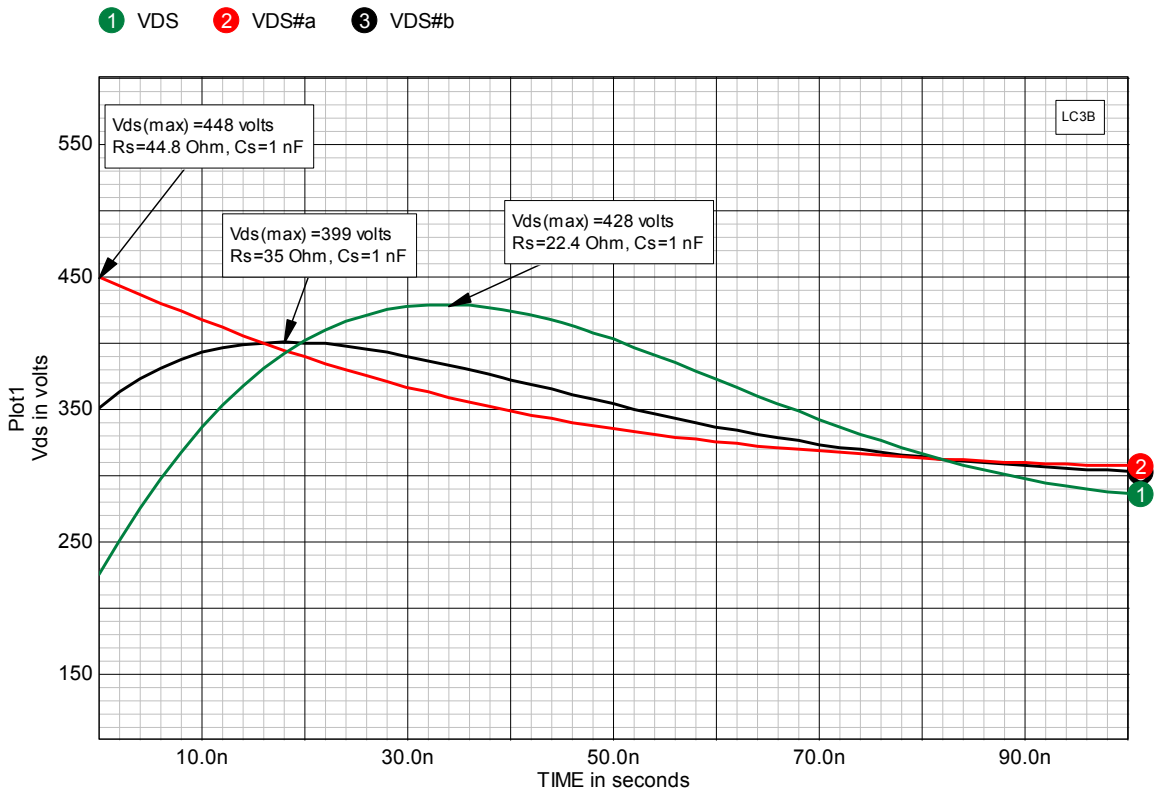


Figure 3-11, effect of small changes in Rs on Vp.

As the waveforms show, the initial choice of value for Rs is not critical. Choosing Rs in the range of Z_o to $2Z_o$ will give a well damped waveform but the optimum value, from the point of view of minimum V_p, will usually be somewhere in-between.

It may be disturbing to only guess at the optimum value of Rs when it is possible to compute an exact value[287] in an idealized situation. The reason we don't bother becomes clear when we move to a more realistic circuit where the output capacitance of the switch (Coss) is added as shown in figure 3-12.

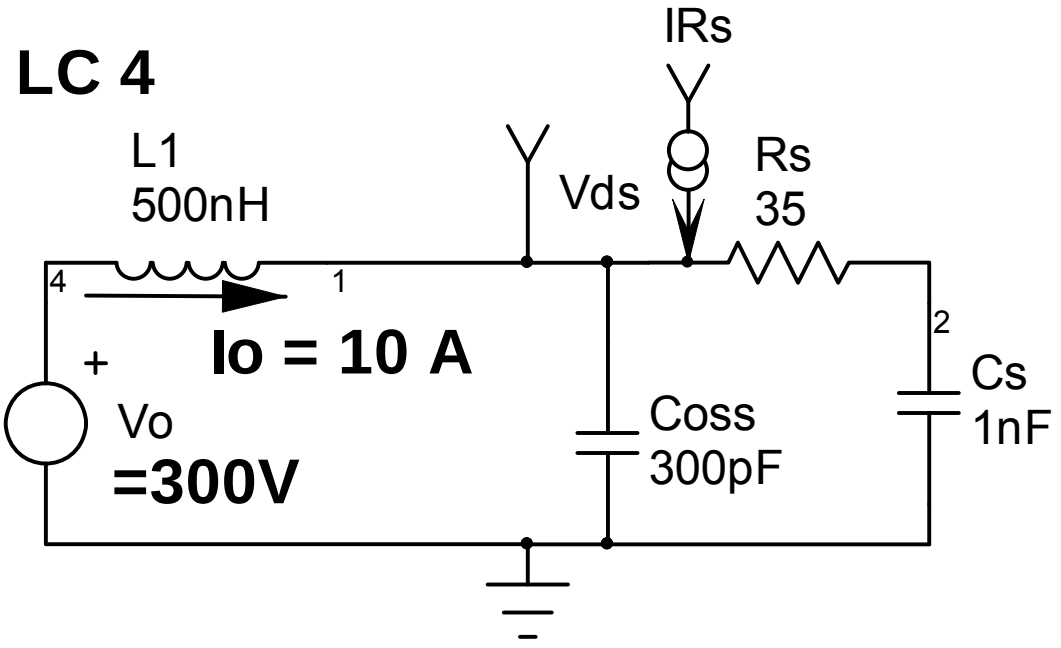


Figure 3-12, circuit with Coss added.

The effect of Coss on the Vds waveforms is shown in figure 3-13. With Rs= 35 Ohm, Cs = 1 nF and Coss = 0, Vp = 399 V. However, with the current values for Rs and Cs, Vp is now 489 V, an increase of 90 V! Coss has a profound effect on Vp because it reduces the effective damping in the circuit. We can vary Rs and will find the optimum value is about 29 Ohm. But Vp is still 482 V. If we want to reduce Vp further we will have to increase the value of Cs. In this example Cs ≈ 3 x Coss. The typical range for Cs is 3 to 10 x Coss. This is discussed further in chapter 7 (figure 7-11).

As shown earlier, Cs is discharged through Rs at switch turn-on. The lower the value for Rs, the higher the peak pulse current will be. Because varying the value of Rs away from the optimum value changes Vp only slowly, it is normal practice to make Rs somewhat larger than optimum to limit the peak current.

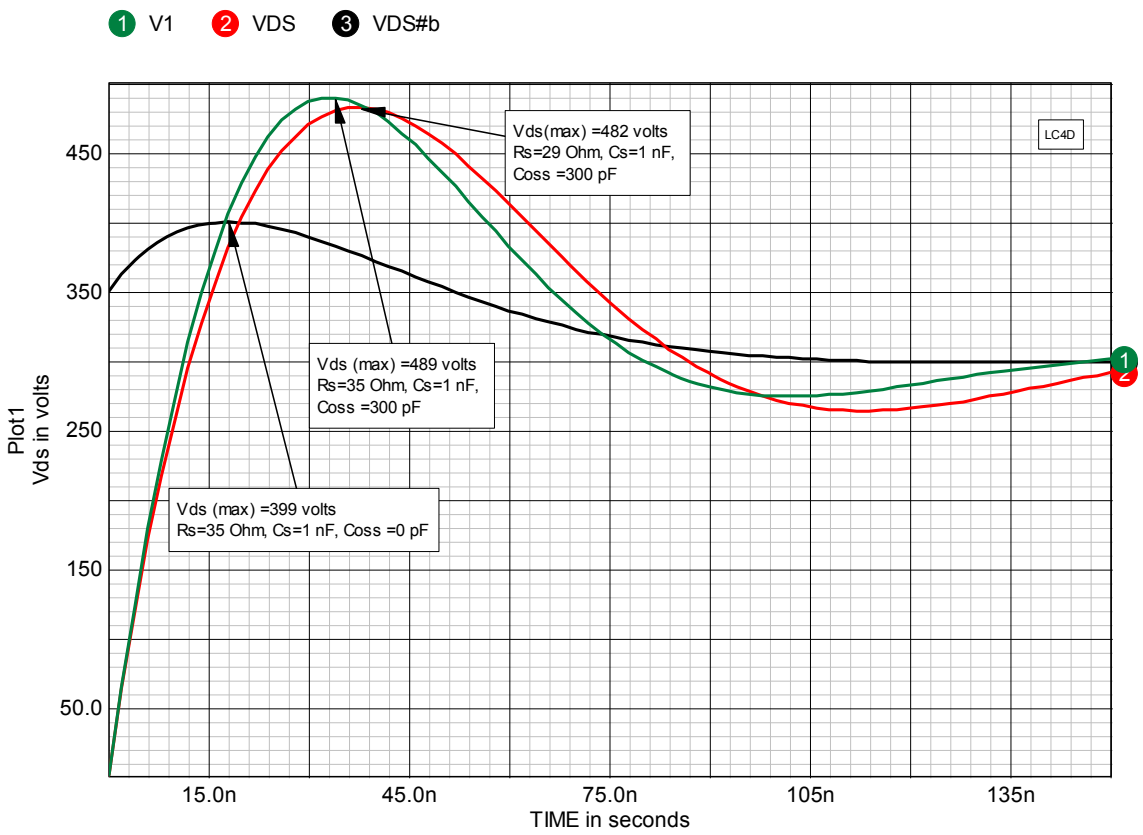


Figure 3-13, Vds waveforms with Coss added to the circuit.

However, there is another consideration which sometimes forces us to make Rs smaller than optimum. For the snubber to perform properly, we assume that the voltage across Cs is reduced to nearly zero during the on-time of the switch. That limits the minimum switch on-time to about five RC time constants. Where:

$$\tau = \frac{1}{RsCs} \qquad (3\text{-}7)$$

Or, conversely, we may have to reduce Rs below the optimum value to properly charge Cs in the time available. Similarly, to properly discharge Cs there may be a minimum conduction time for D1. These minimum time restrictions may force us to use a smaller value for Cs and/or a non-optimum value fro Rs and accept higher V_p.

Choosing Cs

Typical initial values for Cs are in the range of 3 to 10X the shunt capacitance being damped (Coss for example). Smaller values for Cs result in lower dissipation in Rs but also less damping. Higher values for Cs give better damping but also reduce the loss in the switch at the expense of higher loss in Rs. The total circuit loss however, tends to stay almost the same over a wide range for Cs (see figure 7-11).

Usually we can get the values for device capacitance from the manufacturers data sheet. Typically there will be a tabulated value for the capacitance but there may also be a graph like that shown in figure 3-14.

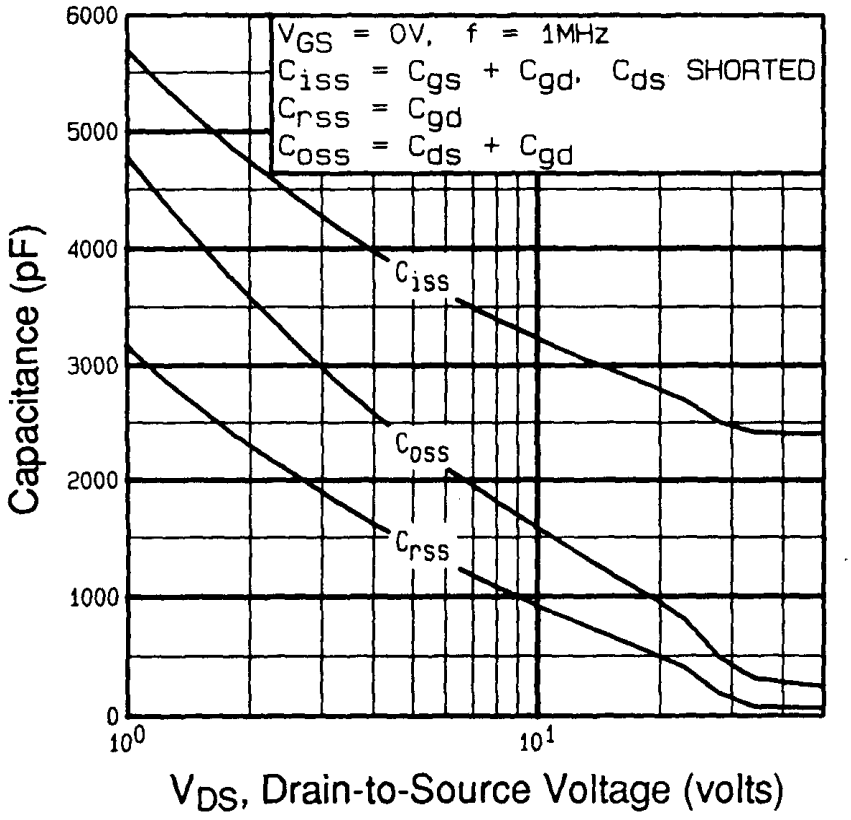


Figure 3-14, junction capacitances for an IRFP450, 500 V MOSFET.

Now we have to be a bit careful. The tabulated value for Coss in the data sheet for this device is 720 pF but this is for Vds=25 V. During

the time interval we are interested in, Vds will be in the neighborhood of 300 V. Looking at figure 3-14, for Vds=50 V the value for Coss is about 250 pF and sloping downward slowly. Extending the graph gives a estimated value of about 150 pF at 300 V. If you are not given a graph like this then an approximate value can be found by dividing the tabular value by 4 if the tabulated value is for a low Vds, which it usually is.

When designing the RC snubber for a diode you will need to know the junction capacitance at the reverse voltage at which the ringing occurs. An example of the variation of diode capacitance with reverse voltage is shown in figure 3-15.

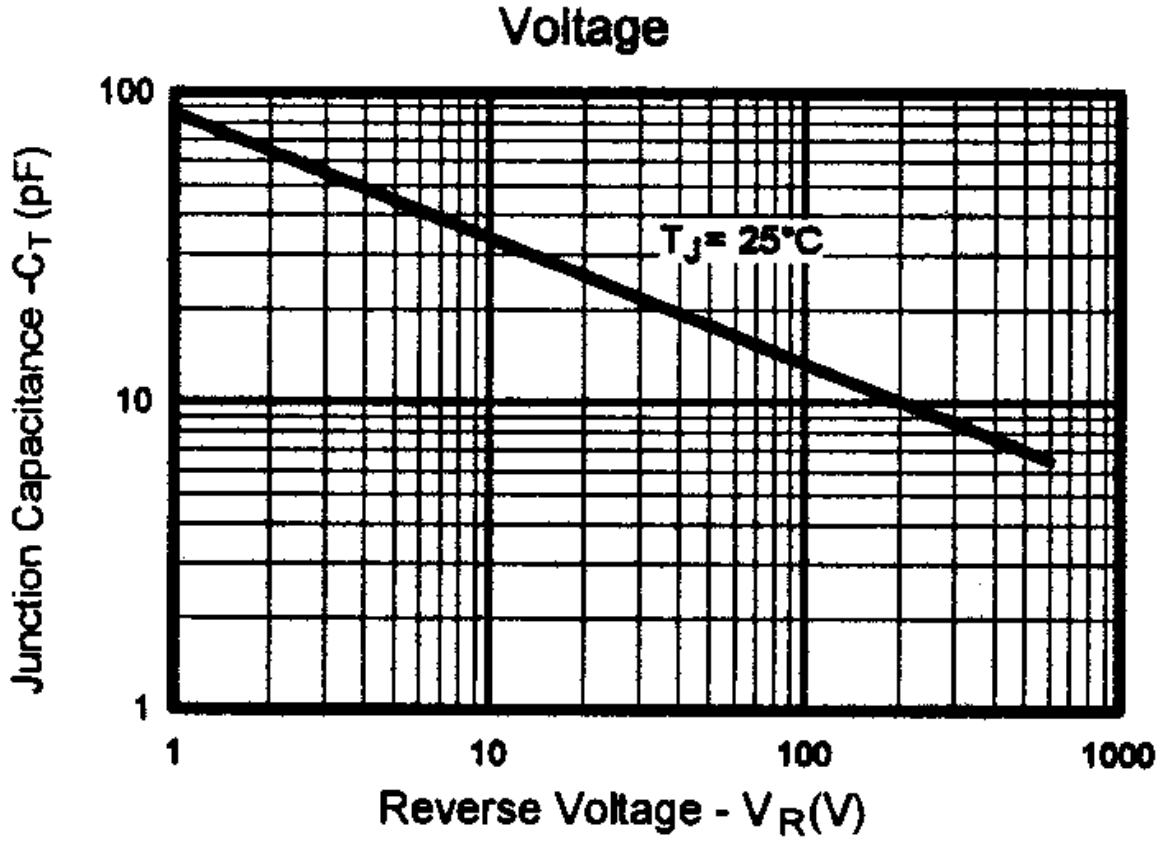


Figure 3-21, junction capacitance for an HFA08TB60, 600 V ultra-fast diode.

The diode capacitance (C_T) is much smaller than the typical accompanying switch, in this case being only about 8 pF at 300 V. However, the tabular part of the data sheet indicates that C_T can be larger, up to 25 pF. When you add in the effect of mounting

capacitance it is better to be conservative and assume the higher value for C_T.

It is possible to perform a test on the actual circuit to get an approximation of the values for the parasitic elements. First we determine the ringing frequency from the Vds waveform. Then we add a known capacitance (C_{test}) across Q1 as shown in figure 3-16,

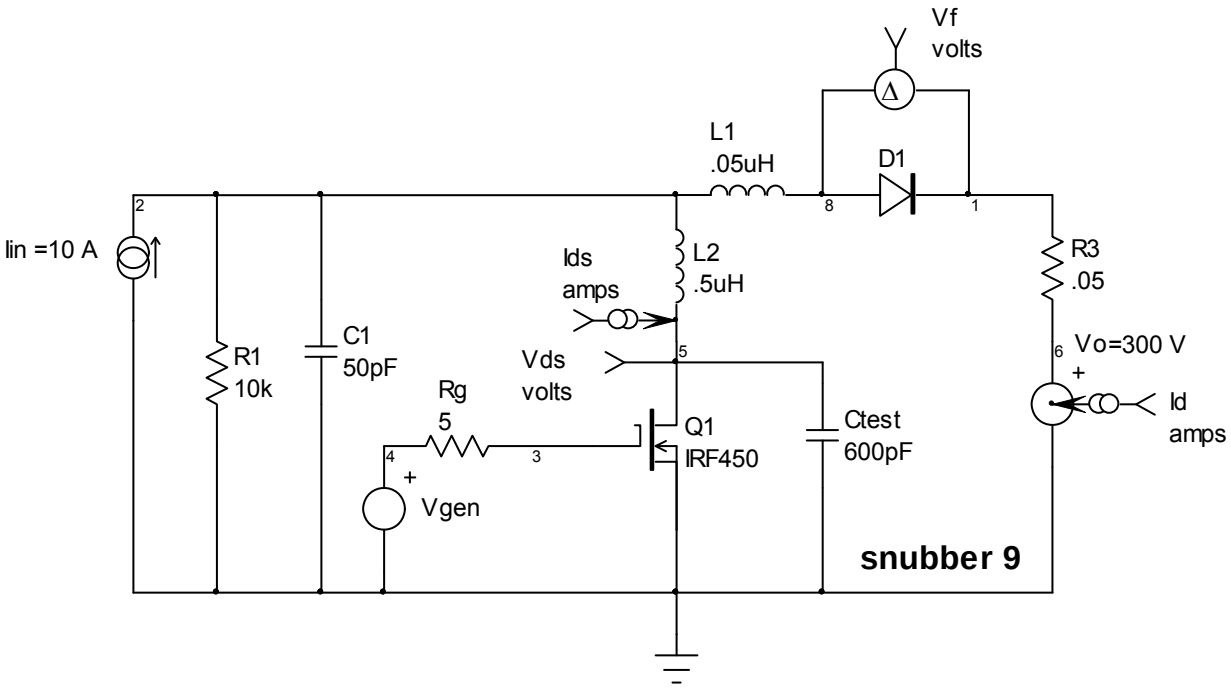


Figure 3-16, adding a test capacitor to the circuit.

and measure the new ringing frequency. The two waveforms are shown in figure 3-17. In this case f_1 = 18.86 MHz (without C_{test}) and f_2 = 7.6 MHz (with C_{test}).

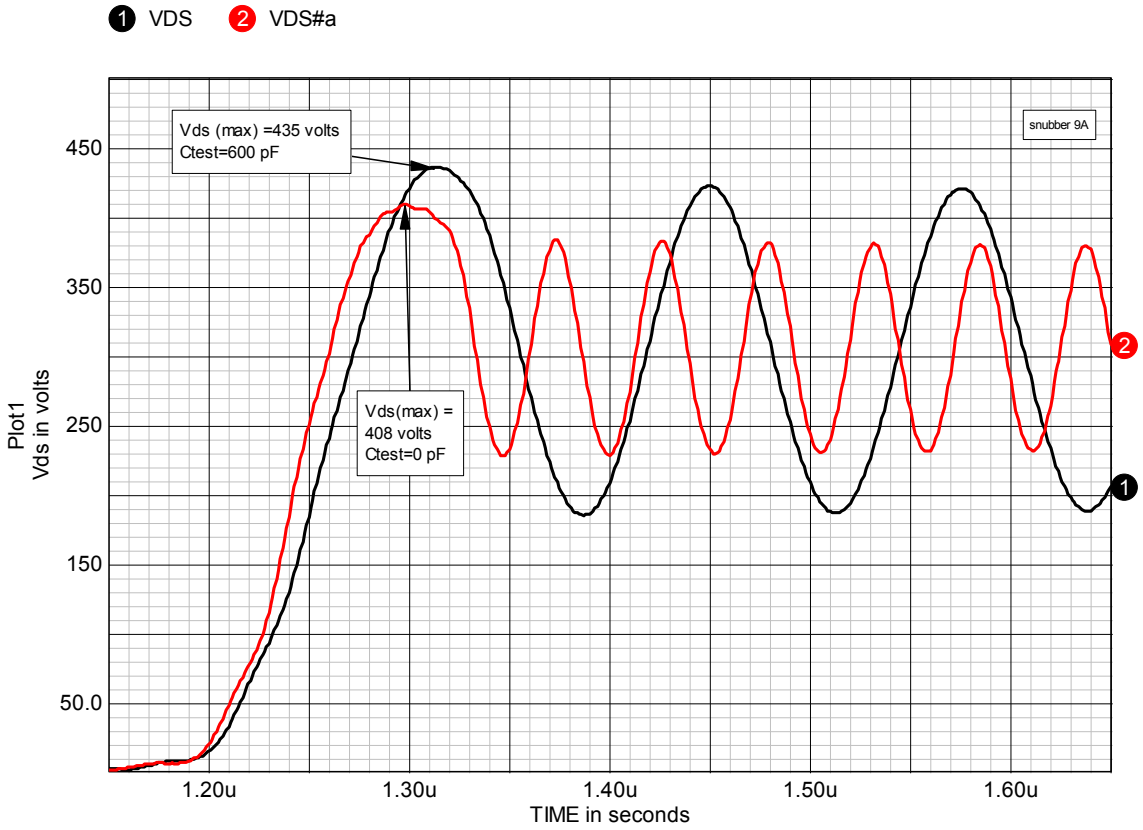


Figure 3-17, Vds ringing with and without C_{test}.

Knowing the value for C_{test}, f_1 and f_2, we can use the following equations to estimate both L2 and Coss:

$$L2 = \frac{1}{C_{test}}\left[\frac{1}{\omega_2^2} - \frac{1}{\omega_1^2}\right]$$

$$Coss = \frac{1}{L2\omega_1^2}$$

$$\omega_1 = 2\pi f_1, \quad \omega_2 = 2\pi f_2 \qquad (3\text{-}8)$$

Equation (3-8) strictly speaking is only for the simple case of a single L and C so when we apply it to a practical circuit like that in figure 3-

22, we only get an approximation since the other elements in the circuit will have some effect. For example, using f_1 = 18.9 MHz, f_2 = 7.6 MHz and C_{test} = 600 pF, we get L2= 582 nH and Coss = 122 pF. Because we're using a SPICE model, we know that L2 is actually 500 nH. But, during turn-on and turn-off, L1 and L2 are effectively in series, i.e. L=550 nH. A value of 582 nH is close. Obviously C1 has some effect which changes the apparent value of L but usually it's not worth fussing about.

This technique gives an approximation of the actual circuit values which is adequate to begin the snubber design. But we have to be careful. When there are multiple different parasitic inductances and capacitances in the circuit, depending on the relative values, the approximation may off by a factor of 2. Also multiple ringing frequencies may be present which complicates things.

In some cases it is possible to adjust the SPICE model values until you have approximated the waveforms in the actual circuit.

A design example

The following is an example of designing an RC-snubber for the circuit shown in figure 3-16 (without C_{test}) using the approximations given earlier and some final adjustment of values. Keep in mind that when Q1 is turning on and D1 off, L1 and L2 will be in series. The same thing happens when Q1 turns off and D1 on. That means the effective value for L is the sum of L1 and L2, ignoring the effect of C1.

For Q1:

L2+L1 = 550 nH, Coss = 125 pF. Since Q1 is a 500 V device, we would like Vds(max) < 400 V:

- set Cs1 = 10 x Coss ≈ 1250 pF

- Zo1 = 19.1 Ohm, let Rs1 = 1.5 Zo = 28 Ohms
- Power dissipation in Rs1 for fs = 100 kHz, P=Cs1 x V_o^2 = 11 W

For D1:

C_T = 25 pF, L1+L2= 550 nH. Since D1 is a 600 V diode, we would like Vrev < 480 V:

- set Cs2 = 250 pF
- Zo1 = 47 Ohms, Set Rs2 = 60 Ohm
- Power in Rs2 for fs = 100 kHz, P=470 pF x 300^2 x 10E5 = 4.2 W

The circuit with two RC-snubbers is shown in figure 3-18.

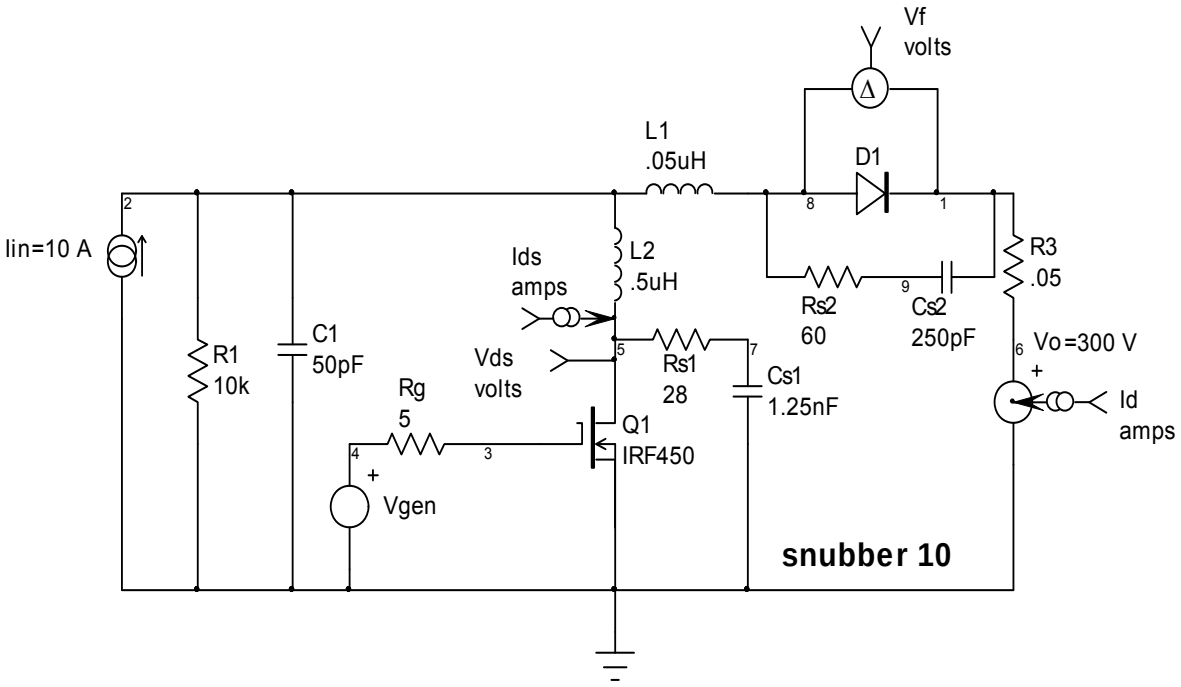


Figure 3-18, RC-snubber design example.

The Vds waveform for Q1 is shown in figure 3-19. In this case the first trial value for Rs1 (28 Ohm) was very close to the optimum (30 Ohm).

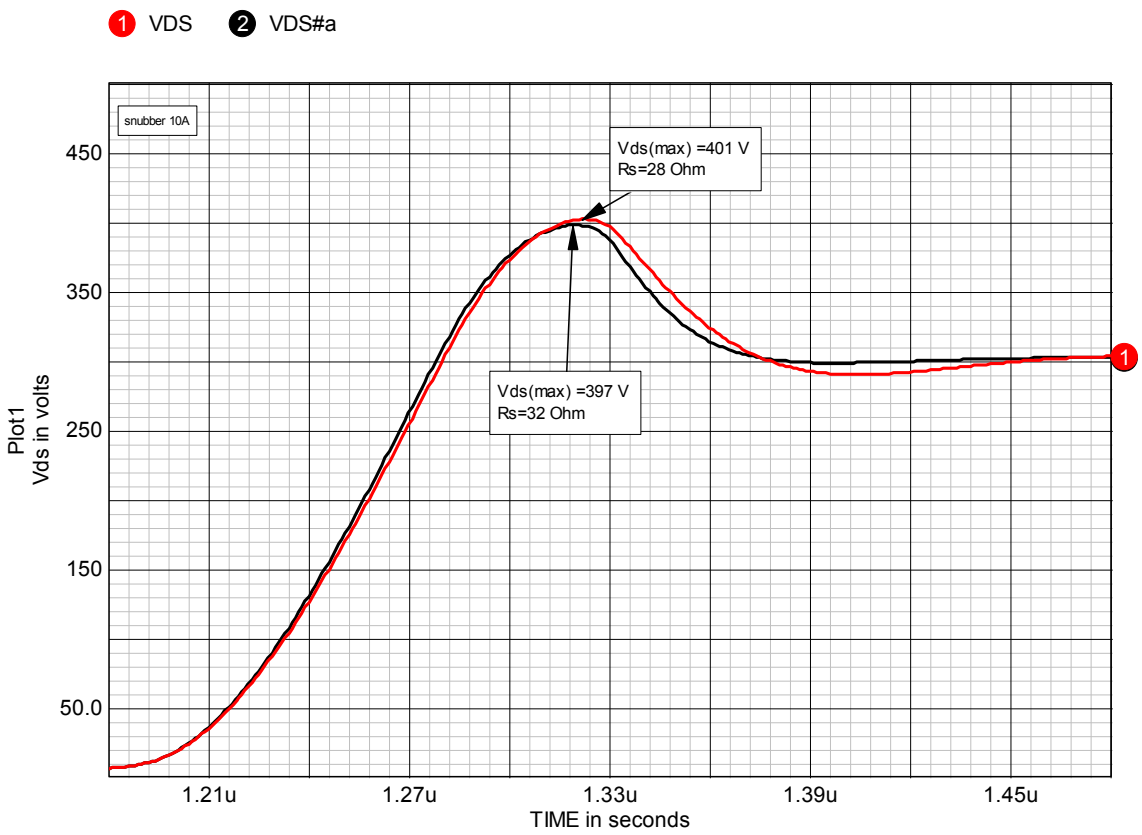


Figure 3-19, comparison of two values for Rs.

The voltage waveform across D1 is shown in figure 3-20. Again the initial guess for Rs2 (60 Ohm) is close to optimum. However, we have not met our goal of Vrev < 480 V. To meet that requirement it will be necessary to increase Cs2 to 470 pF and use a smaller value for Rs2 (55 Ohm). The peak reverse voltage is now down to 477 V which meets the requirement.

Because the two snubbers will interact to some extent we can recheck the value of Vds peak on Q1. In this example, Vds peak has dropped slightly to 391 V due to the increased capacitance of Cs2.

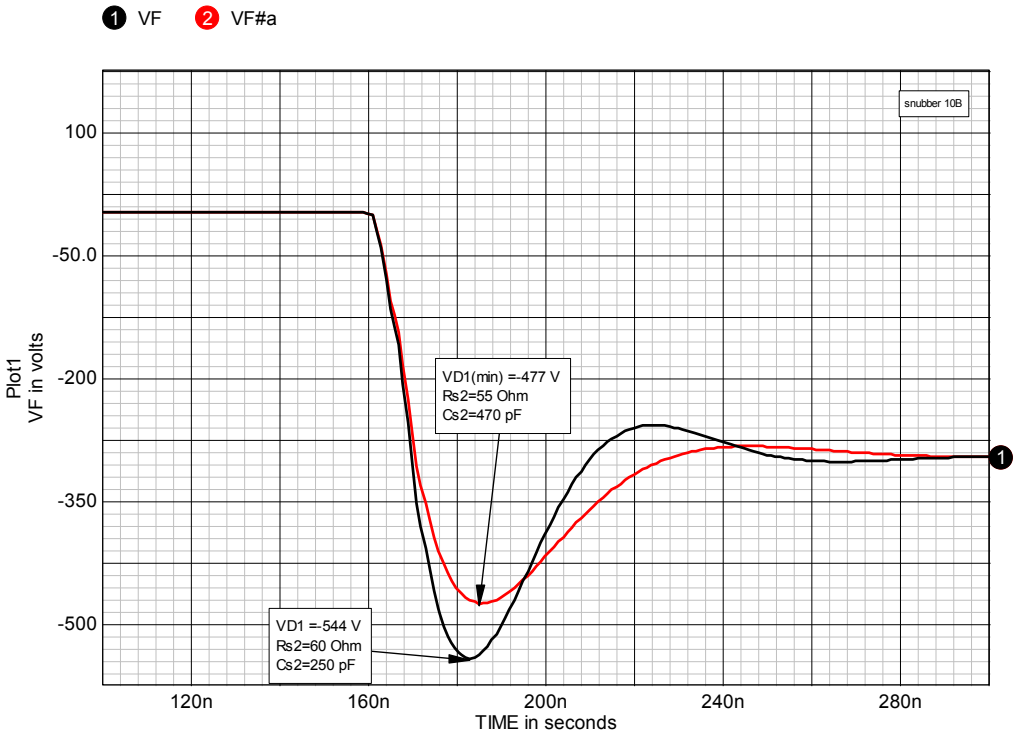


Figure 3-20, reverse voltage across D1at Q1 turn-on.

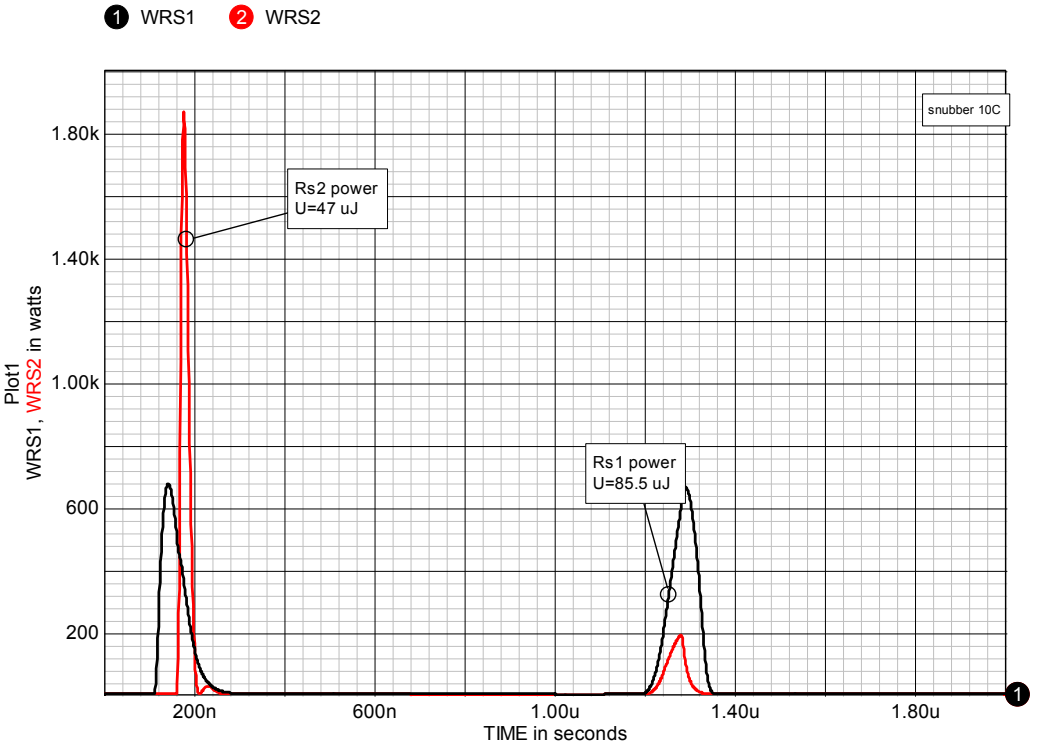


Figure 3-21, power dissipation in Rs1 and Rs2: one switching cycle.

The final step is to check the power dissipation in Rs1 and Rs2. The instantaneous power dissipation and total energy losses per

switching cycle for each resistor are shown in figure 3-21. For a 100 kHz switching frequency the dissipation in Rs1 = 9 W and Rs2 = 5 W. These values, taken from the SPICE model, are close to the values we initially estimated. A detailed discussion on the selection of the actual resistors for snubber applications is given in chapter 6.

As a final check we can examine the load-line for Q1 as shown in figure 3-22. The graph provides a comparison between load-lines with and without the RC-snubbers.

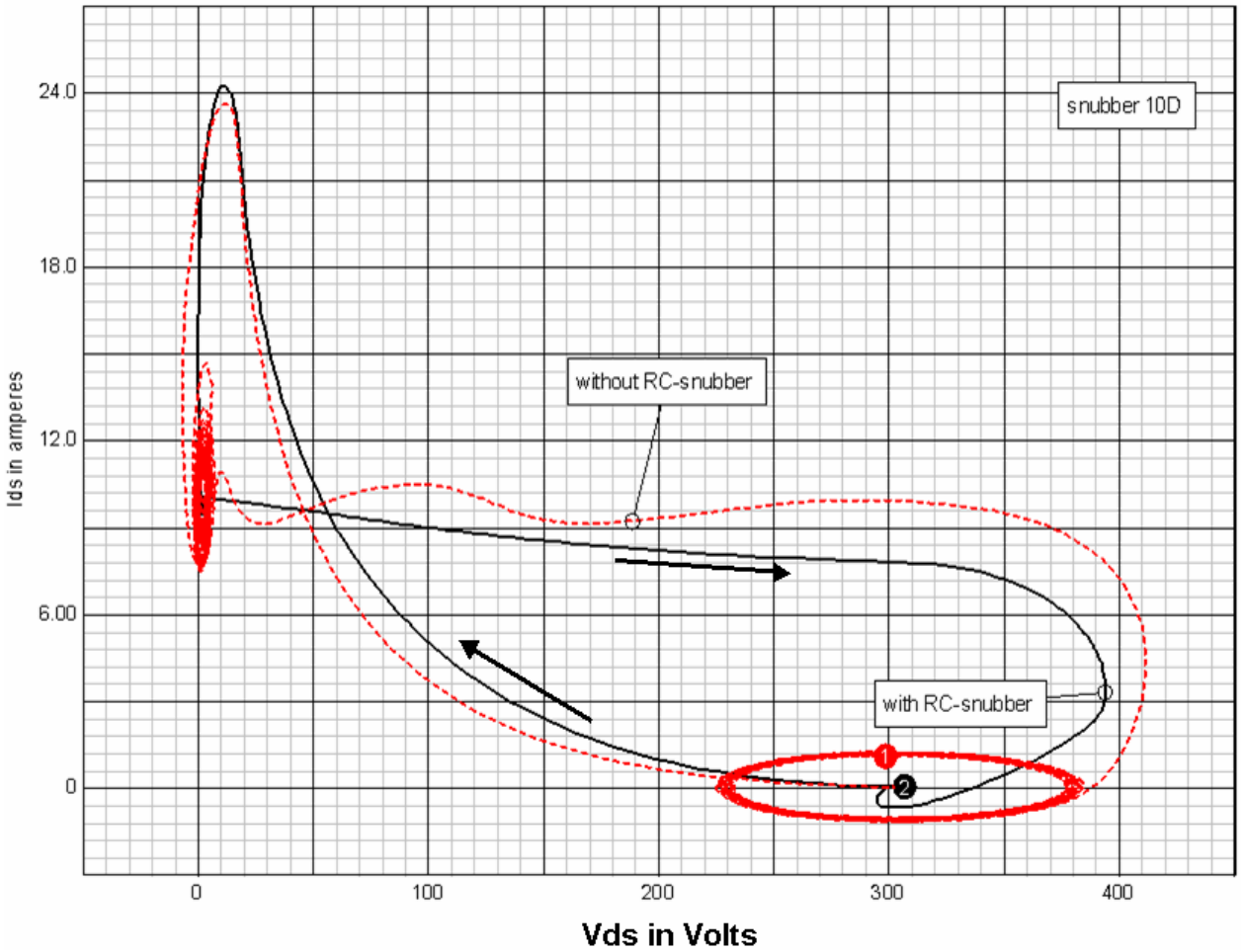


Figure 3-22, comparison of load-lines with and without the RC-snubbers.

With the snubbers, the ringing is very well damped and the peak value for Vds is now below 400 V, as desired for derating. In addition the turn-off portion of the trace has lower instantaneous power (Vds x Ids). However, the turn-on portion of the trace (with the snubber) has higher values for of instantaneous power and a higher peak value for

Ids. This is due to the need for charging and discharging the energy in the snubber capacitors at Q1 turn-on.

This is also a good time to check on the power dissipation in Q1 as shown in figure 3-23.

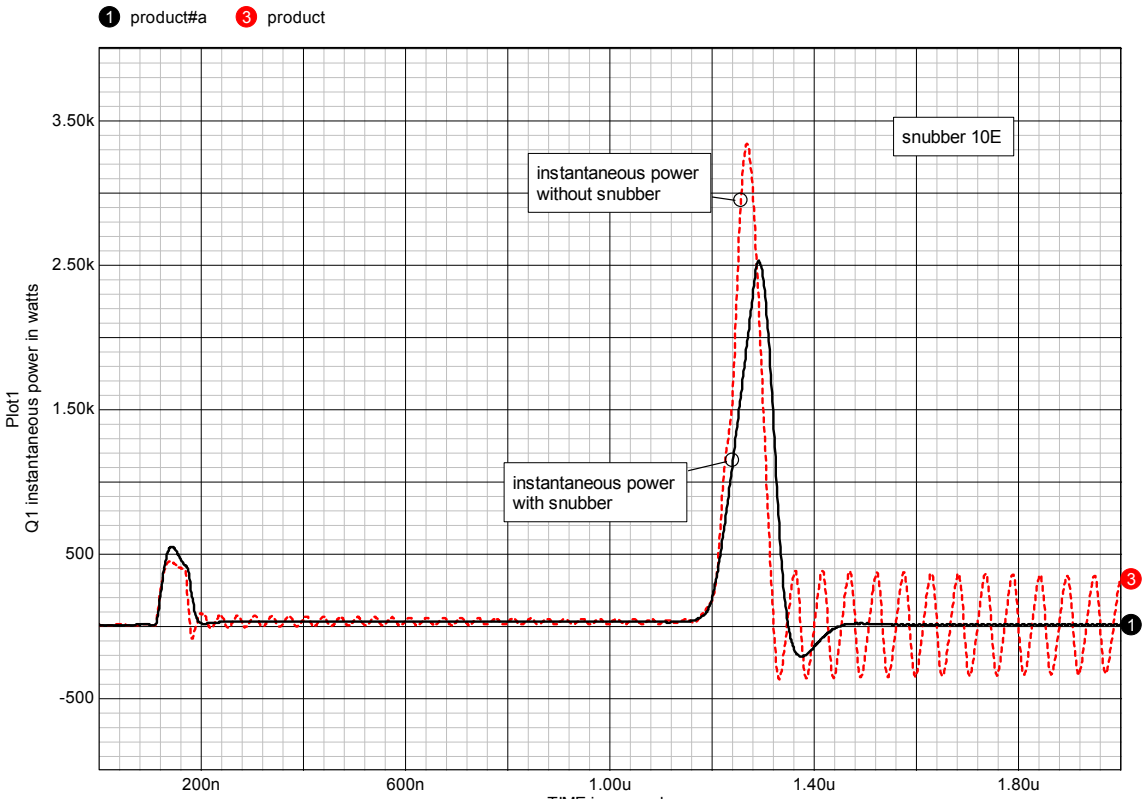


Figure 3-23, instantaneous power dissipation in Q1 with and without the RC-snubbers.

At turn-off the peak power is substantially lower and at turn-on it is only marginally greater. It seems that this design meets our basic requirements.

Chapter 4

Dissipative RLC-diode snubbers

Passive RC-snubbers can be very effective in reducing peak voltages and damping ringing waveforms. Sometimes however, more is needed. For example, we may wish to reduce power dissipation in a switch due to switching transitions or alter the load-line to reduce peak stresses and to stay within SOA boundaries. In thyristor and IGBT circuits it is often necessary to limit dv/dt and/or di/dt.

The snubber circuits shown in figure 4-1 and variations of them can be used for these purposes.

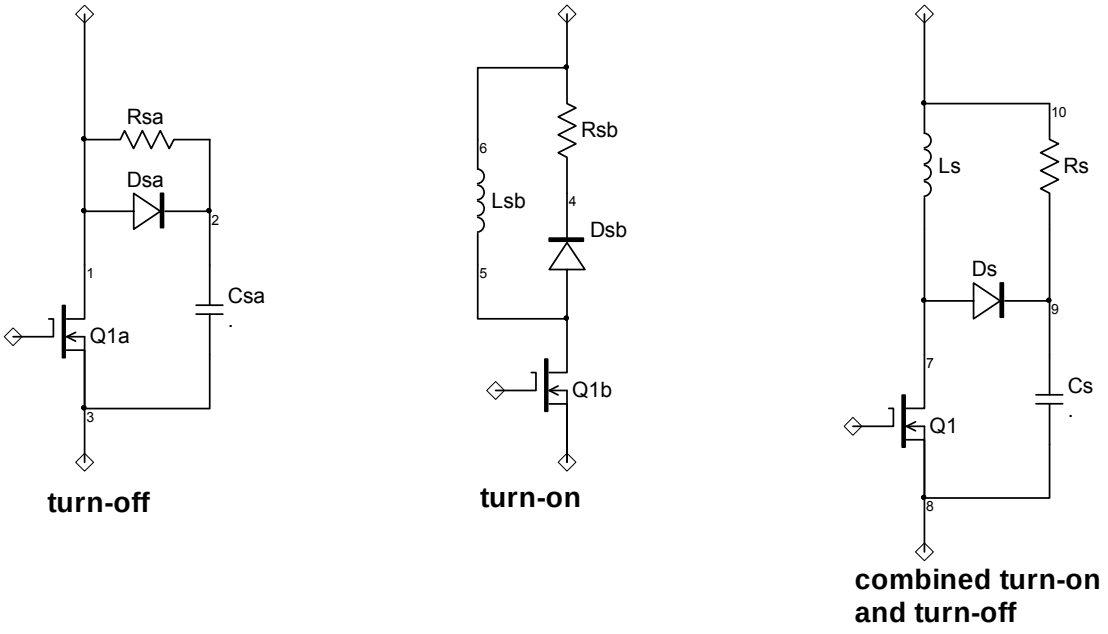


Figure 4-1, Typical RLC-diode snubbers.

After the RC-snubber, RLC-diode family of snubbers are the most commonly used.

We will begin with an idealized boost converter without any snubber. Using this as our reference, we examine several different snubbers (turn-off, turn-on and combination snubbers), how they modify and improve the circuit waveforms, the disadvantages of the circuits and how to determine appropriate component values. Finally we'll discuss variations of the basic snubbers, including non-linear capacitors and saturable inductors, which have advantages in some applications. Initially we will be using component values for the snubber examples which work very well but appear to be picked out of thin air with no explanation. The rational for the choice of component values will be explained after the snubber behavior is described, in the section on choosing component values.

This family of snubbers is referred to as "dissipative" because the energy diverted from the switch, reducing switch dissipation, will be dissipated in a snubber resistor (Rs). However, this does not mean that all the energy saved from the switch transitions is necessarily lost. In some cases overall circuit efficiency can be improved somewhat by careful selection of snubber component values. It is also possible to decrease overall efficiency, so care must be taken in selecting values.

Basic circuit

An idealized boost converter is shown in figure 4-2.

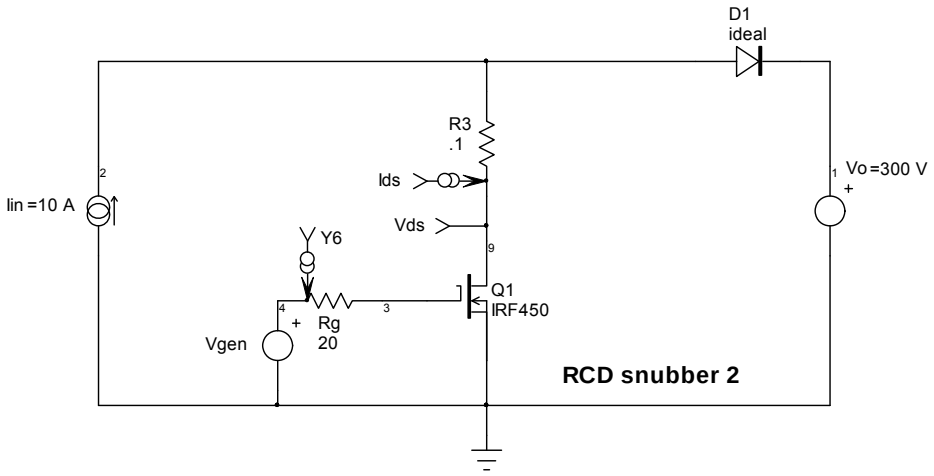


Figure 4-2, basic converter used as a starting point.

Snubber components will be added to this circuit to illustrate the basic operation of RLC-diode snubbers. Initially a realistic switch will be used with ideal diodes. This allows us to focus on the snubber behavior. Later, a real diode and parasitic elements will be added.

Typical waveforms associated with figure 4-2 are shown in figure 4-3.

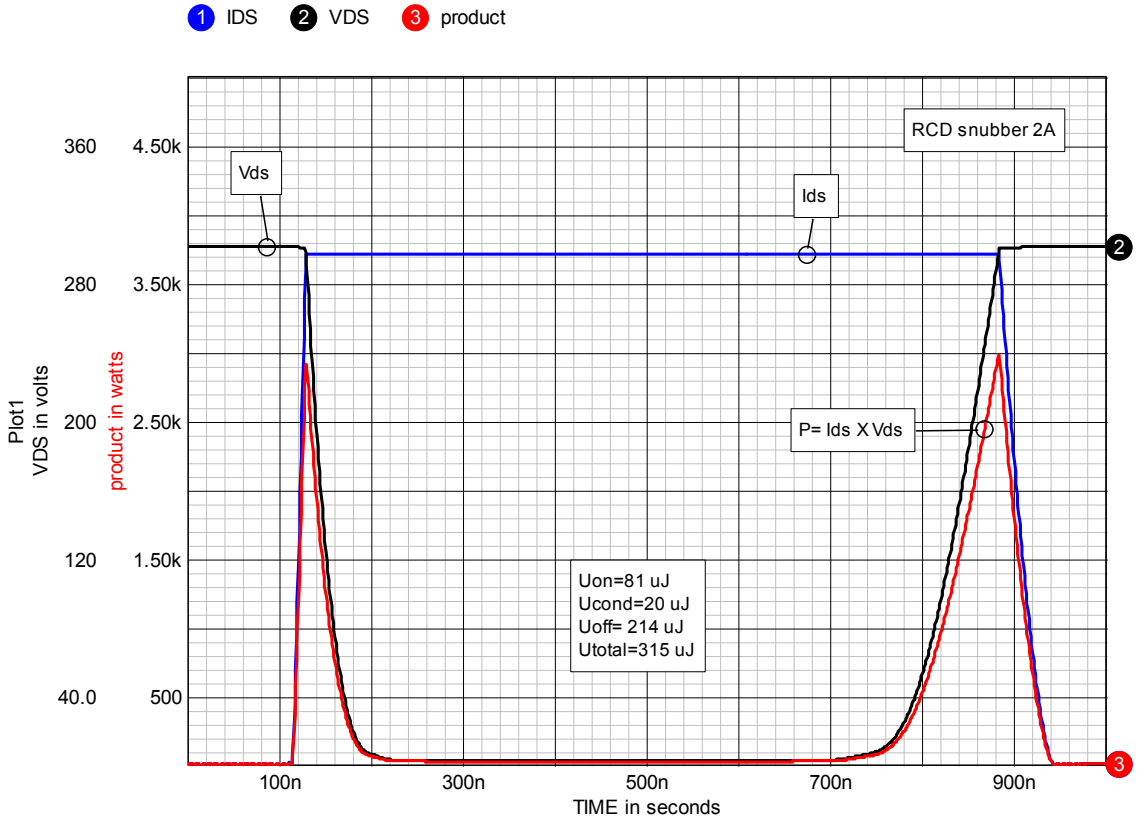


Figure 4-3, Typical Ids and Vds waveforms for the circuit in figure 4-2. The product Vds X Ids represents the instantaneous power dissipation.

The tabular insert in the figure lists the energy dissipation per switching cycle in µJoules. Uon is the energy lost at turn-on, Ucond is the conduction loss while Q1 is on, Uoff is the energy lost at Q1 turn-off and Utotal is a summation of the total loss per switching cycle. We will show this table on future figures to see if we are actually improving the circuit efficiency or not. The energy is obtained by integrating the instantaneous power (Vds X Ids) over the interval of interest. The power loss is simply the product of the switching frequency and the energy loss per switching cycle.

In the absence of a snubber, the peak power dissipation at turn-on and turn-off will be about 3 kW for Iin = 10 A and Vo= 300 V. The energy loss per switching cycle (Utotal) in this example is 315 µJ.

The load-line associated with the un-snubbed converter is shown in figure 4-4. It is nearly rectangular with the turn-on and turn-off portions of the traces lying on top of each other. The peak stresses are very high.

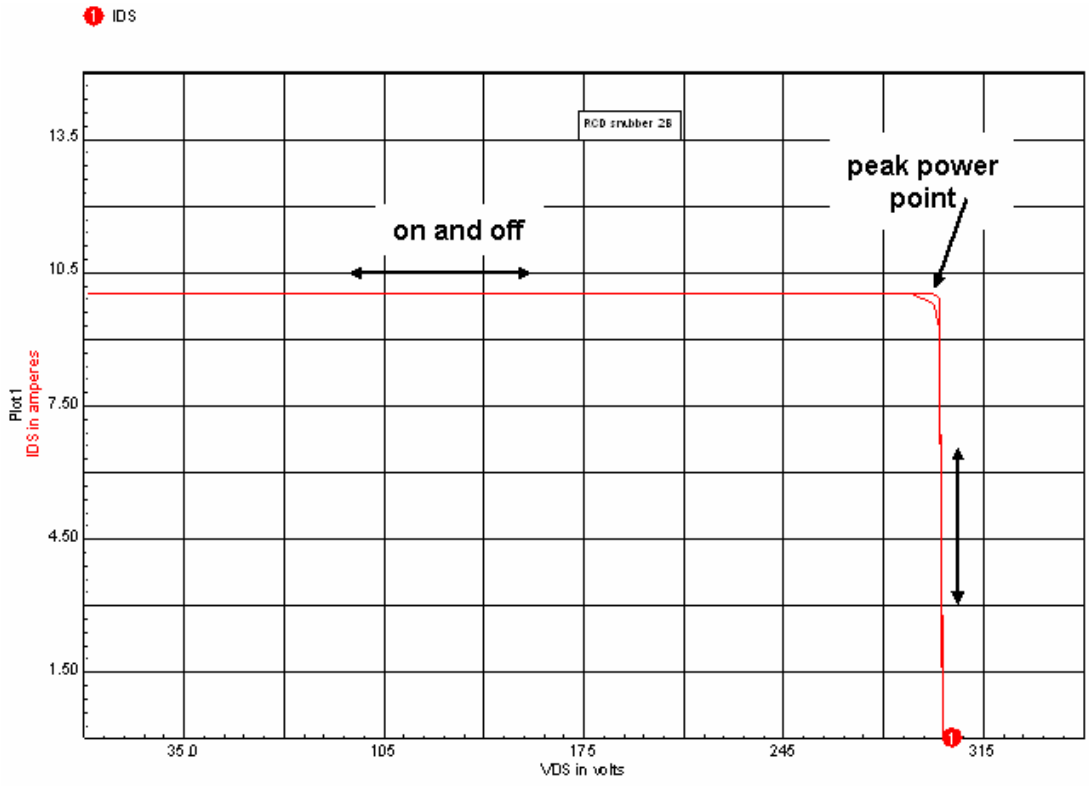


Figure 4-4, Load-line for un-snubbed operation.

A Turn-off snubber

Figure 4-5 shows the basic circuit (figure 4-2) with an RC-diode snubber (Rs, Cs and Ds) in parallel with Q1. R3 and R4 are for current metering in the model and are small enough to not affect circuit operation.

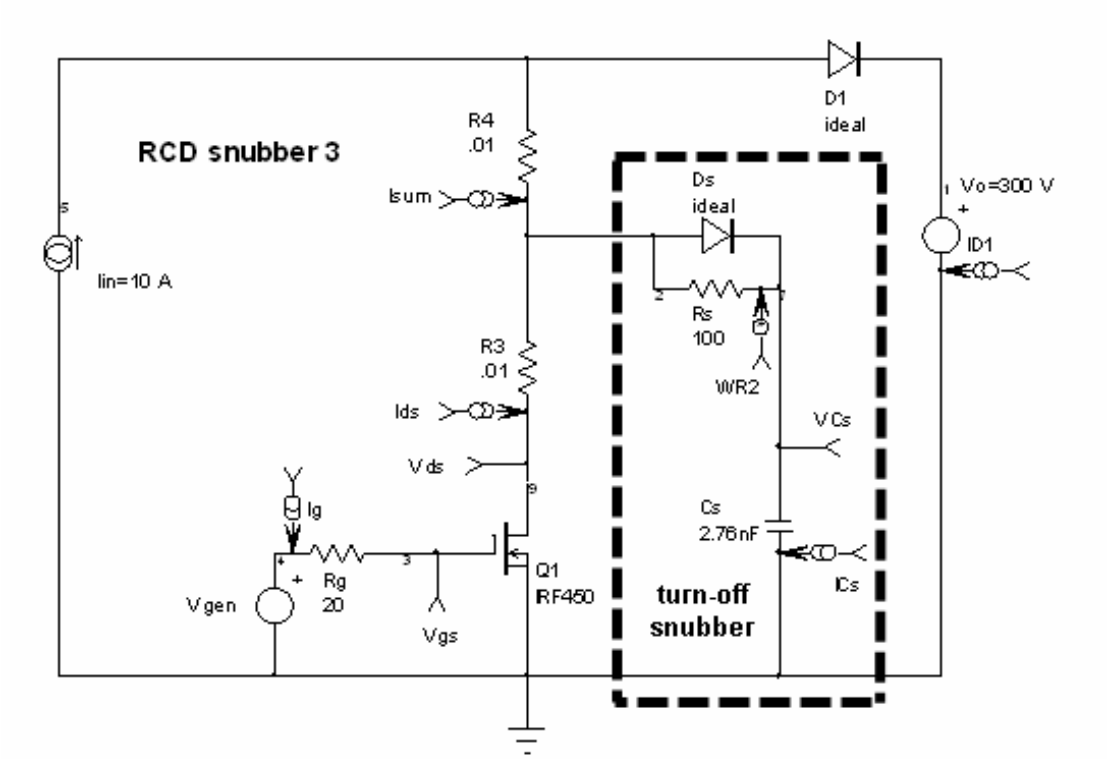


Figure 4-5, Boost converter with an R-C-diode turn-off snubber.

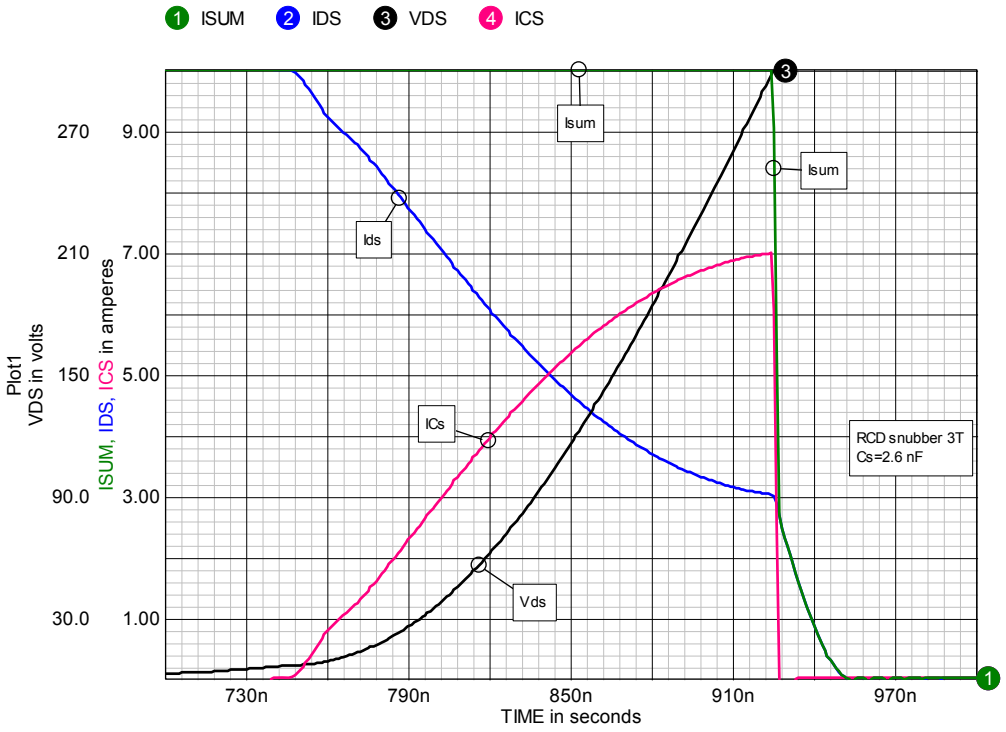


Figure 4-6, waveforms for Q1 and Cs at Q1 turn-off.

Initially, Q1 is on and Cs has been discharged through Rs during the on-time of Q1. At Q1 turn-off, Ids is diverted from Q1 through Ds into Cs, delaying the rise of Vds as shown in figure 4-6.

Figure 4-6 shows Ids, ICs and their sum (Isum) compared to Vds. The falling part of the Ids waveform in figure 4-6 is substantially different from the almost linear ramp for Ids shown in figure 4-3. In particular note that Ids and ICs are not linear and also, there is a knee in Ids at the point where Vds = Vo.

The gate-to-drain capacitance (Cgd, see figure 2-28) has a strong effect on the Ids waveform. At turn-off, as Vds rises a current will be injected into the gate though Cgd due to d(Vds)/dt. This current offsets the turn-off current flowing through Rg (the gate resistor), reducing the rate of fall of Vgs, and in turn slowing the fall-time of Ids. When Vds rises to Vo, it is clamped to Vo by D1 and d(Vds)/dt=0. At this point the current injected into the gate via Cgd goes to zero allowing Vgs to drop quickly, shutting off the last of Ids. At the point where Vds=Vo, ICs = 0 and the remaining Ids is commutated through D1. This happens at the knee in the Ids waveform.

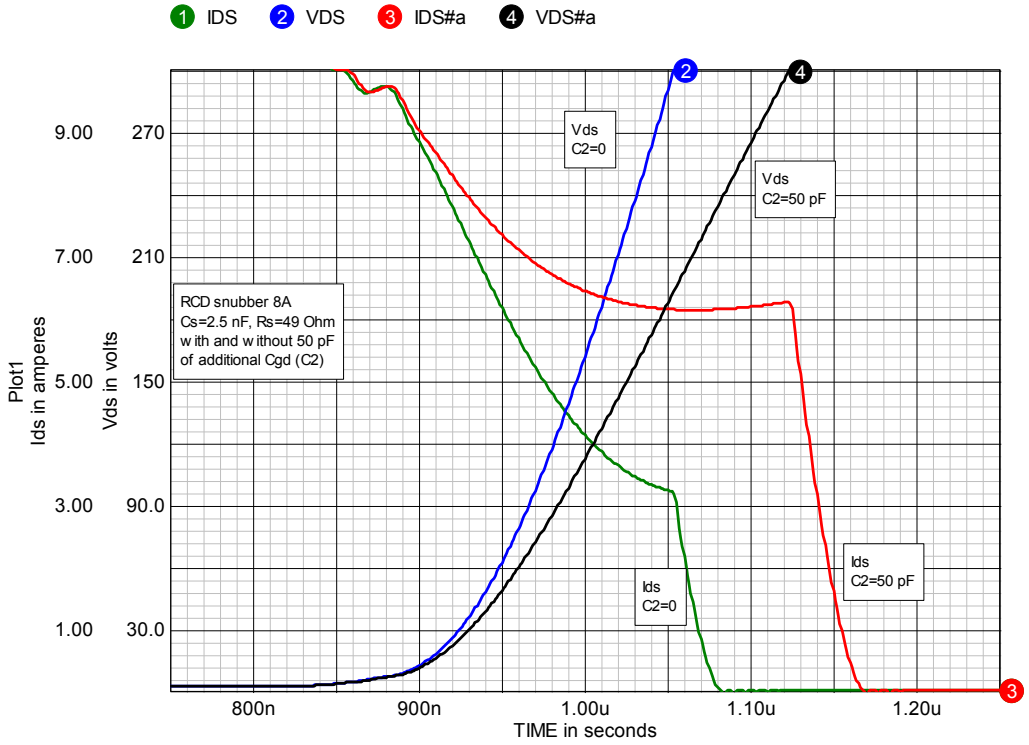


Figure 4-7, effect of additional gate-to-drain capacitance.

We can illustrate the effect of Cgd by adding 50 pF from drain-to-gate of Q1. The resulting waveforms are shown in figure 4-7 which compares the turn-off waveforms with and without the additional gate-to-drain capacitance. This is also warning to be careful not to introduce additional parasitic gate-to-drain capacitance in the circuit layout.

The value for Rg has a strong influence on Q1 switching times. The maximum voltage and the transition times of Vgen however, have only a small effect because most of the switching action occurs when Vgs is close to Vth, the threshold voltage. The interaction between the value for Rg, Ids turn-off time and the location of the Ids knee, is illustrated in figure 4-8 for a given value for Cs. A smaller value for Rg means a more rapid Ids fall-time and in turn, a greater effect for a given value of Cs.

This is a very good example of the interaction between switch behavior, drive circuit impedance and a snubber. Similar behavior occurs in BJT's and IGBT's.

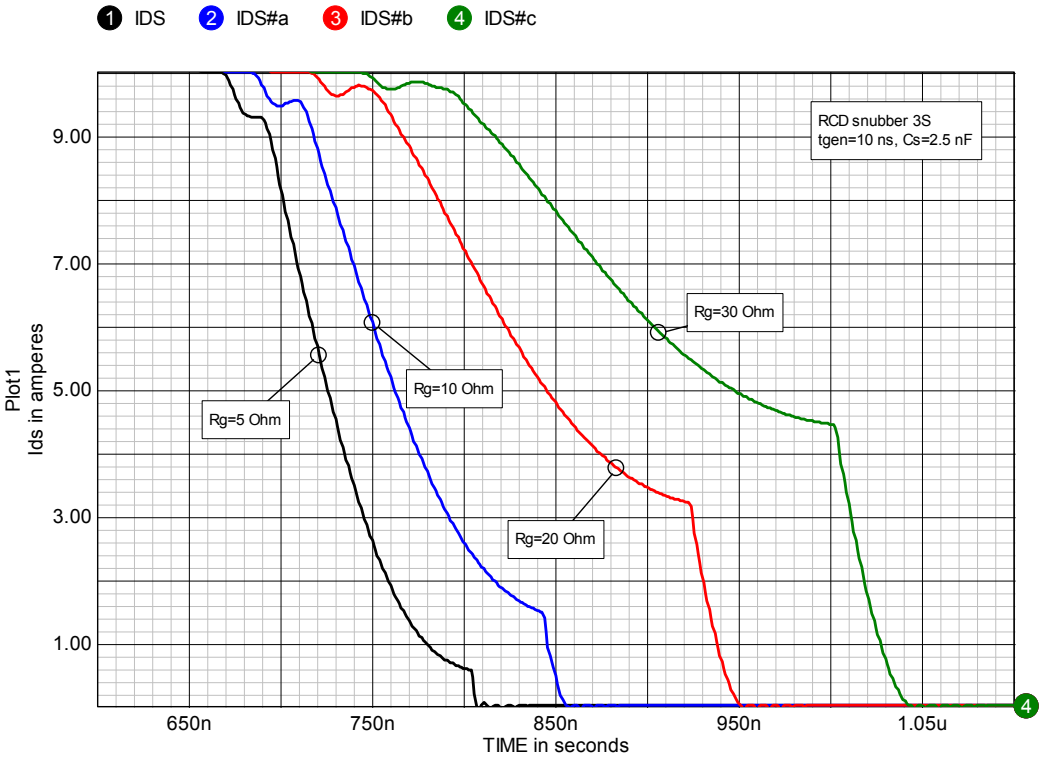


Figure 4-8, Illustration of the effect of Rg on Ids turn-off.

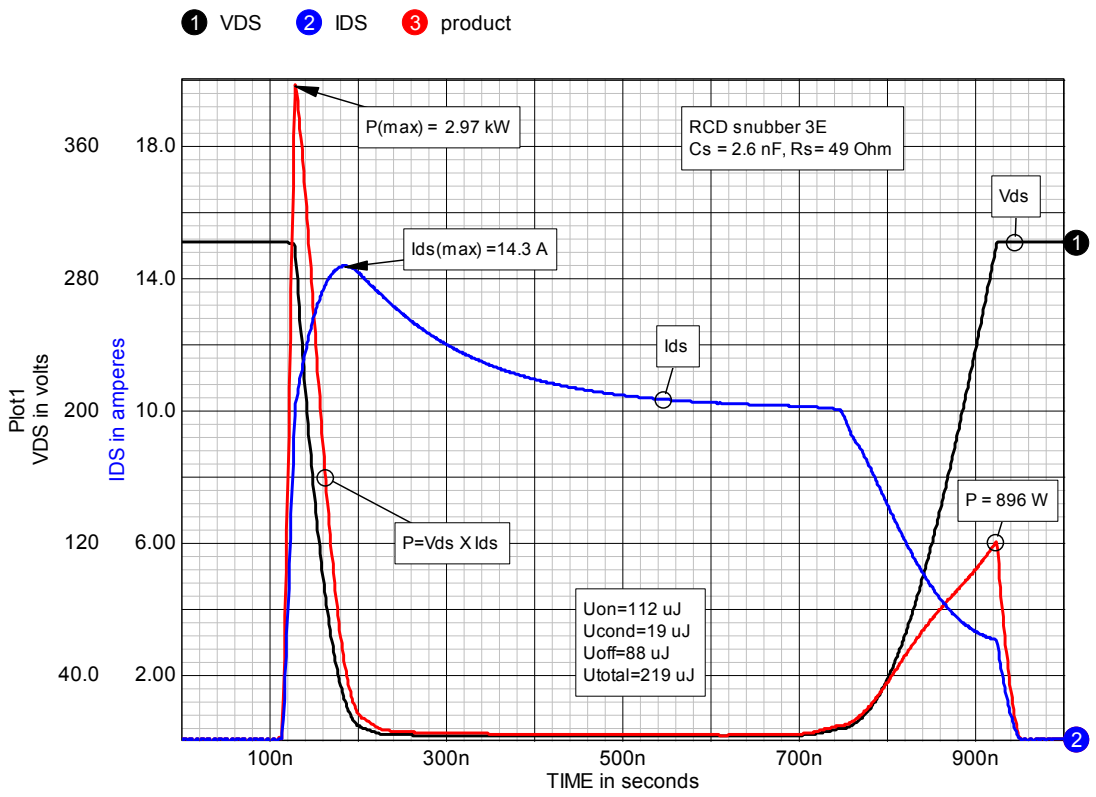


Figure 4-9, Waveforms associated with the circuit in figure 4-5.

Waveforms for the entire switching cycle are shown in figure 4-9. Compared to the un-snubbed case (figure 4-3), the peak power at turn-on has not changed significantly but the peak current is higher even though D1 is an ideal diode with no reverse recovery current. The additional current at turn-on is due to the discharge of Cs through Rs and Q1. The peak current can be reduced by increasing the value of Rs but Rs must be kept small enough to allow Cs to be discharged down to < 5% of Vo during the minimum on-time of Q1. Typically the Rs x Cs time constant should be about one fifth of the minimum on-time of Q1.

While at turn-on we have increased Ids, turn-off is improved. The peak power has gone from 3 kW to less than 900 W and the total energy dissipated in Q1 is reduced by 30%, from 315 to 219 µJ. The power dissipation in Q1 is reduced but the overall circuit loss is essentially the same due the energy dissipation in Rs (U=98 µJ, calculated from the current or power waveforms in Rs) during the discharge of Cs at Q1 turn-on, as shown in figure 4-10.

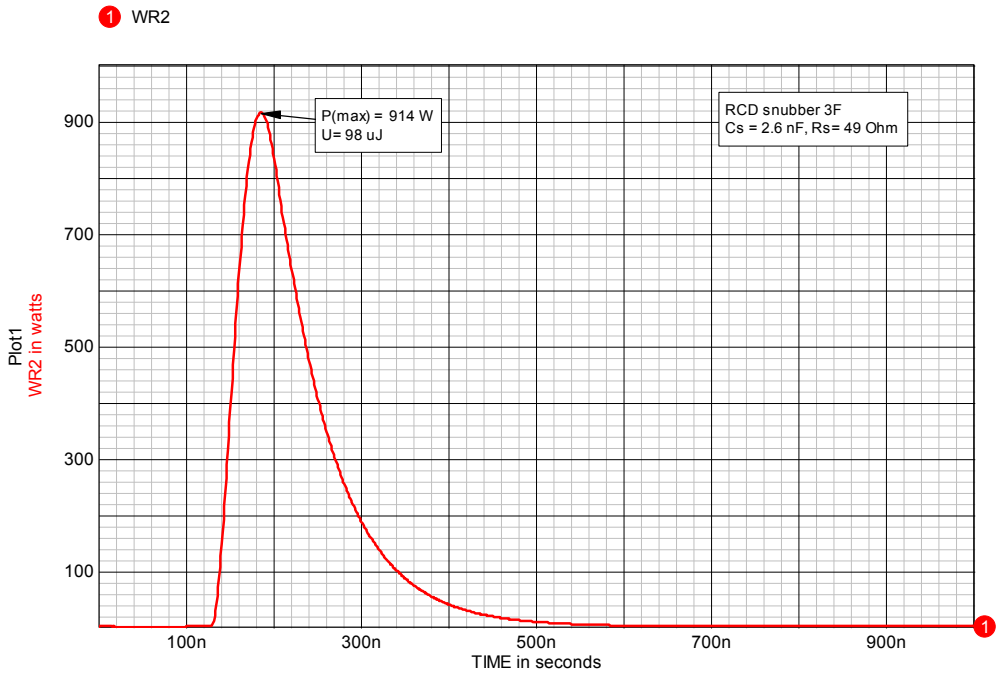


Figure 4-10, Power dissipation in Rs during the on-time of Q1.

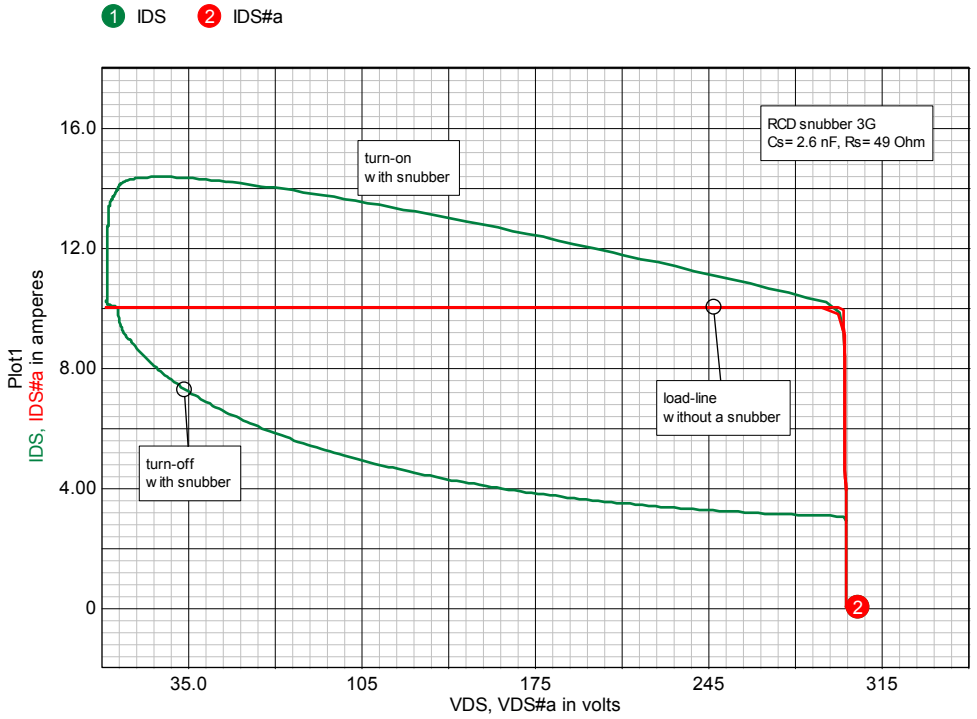


Figure 4-11, Load-line comparison with and without the turn-off RC-diode snubber.

The load-line associated with figure 4-9 is shown in figure 4-11, along with the un-snubbed load-line. Compared to the no-snubber case, the turn-off portion of the load-line is greatly improved. But this improvement comes at the expense of increased stress during turn-on. Just as we saw in the case of the RC-snubber, an improvement in one transition leads to higher stress in the other.

The details of Ids and Vds waveforms at turn-off, for a given load current, will depend on the value for Cs. Figures 4-12, 4-13, 4-14 and 4-15 show the effect of varying the value of Cs on these waveforms, the power dissipation and the load-line.

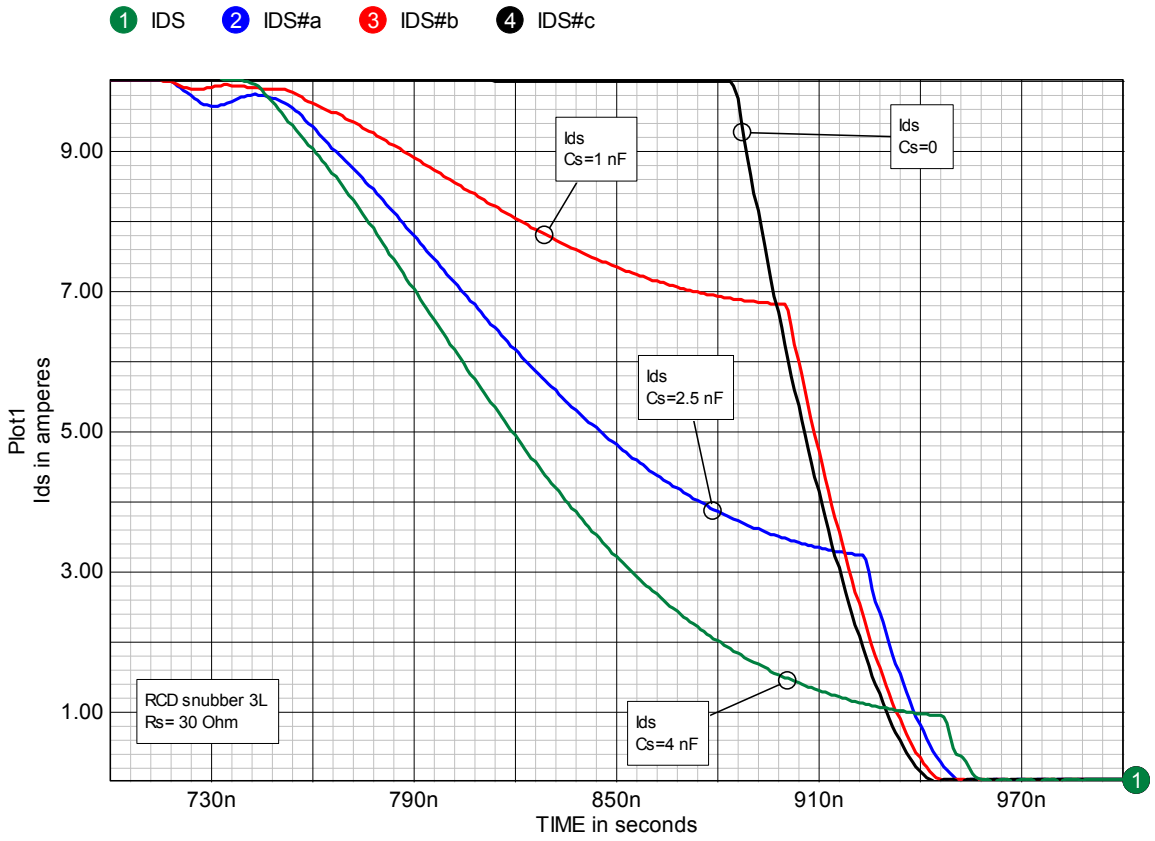


Figure 4-12, Turn-off Ids waveforms for various values of Cs.

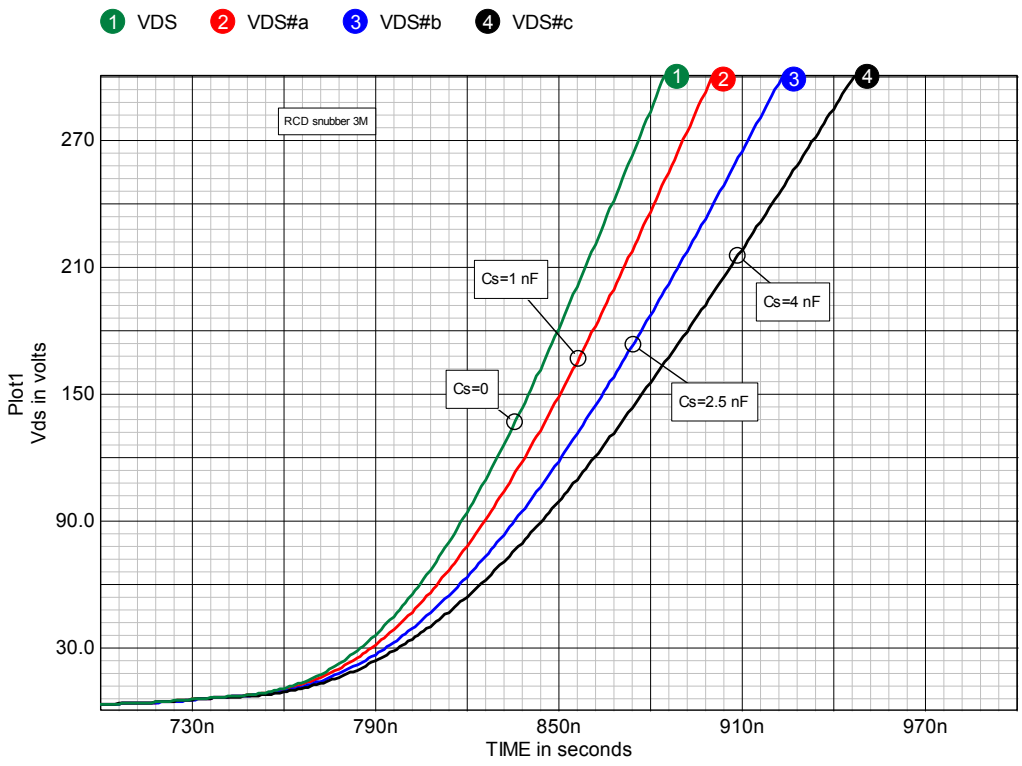


Figure 4-13, Turn-off Vds waveforms for various values of Cs.

Note that with a larger Cs, the rate of rise of Vds (d(Vds)/dt) is slower but d(Ids)/dt before the knee is more rapid. This is a direct consequence of Cgd (the gate-to-drain capacitance). As d(Vds)/dt decreases, less current is injected into the gate which allows Vgs to fall more rapidly.

Clearly the power dissipation at turn-off drops rapidly as the value for Cs is increased. However, just the opposite is happening at turn-on as shown in figure 4-15.

The widening of the power loss pulse at turn-on is due to the current flowing through Q1 during the discharge of Cs. The larger the value of Rs the smaller this effect will be but the maximum value for Rs is limited by the requirement to discharge Cs in the minimum switch on time available.

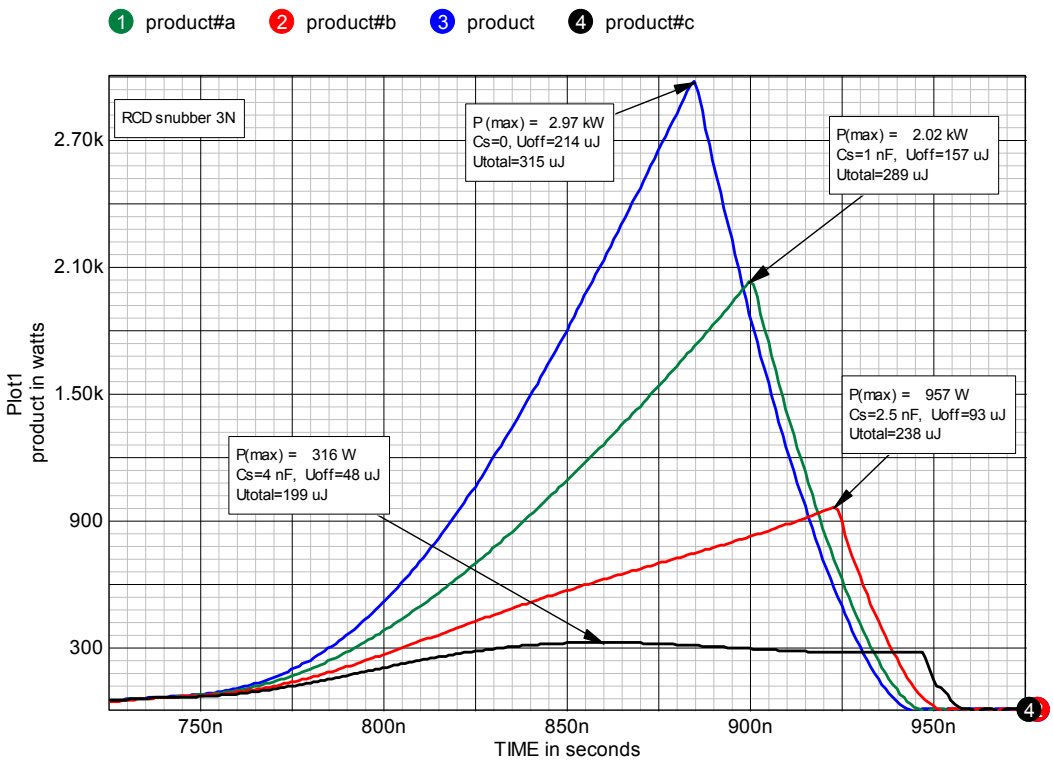


Figure 4-14, Turn-off power and total energy dissipation.

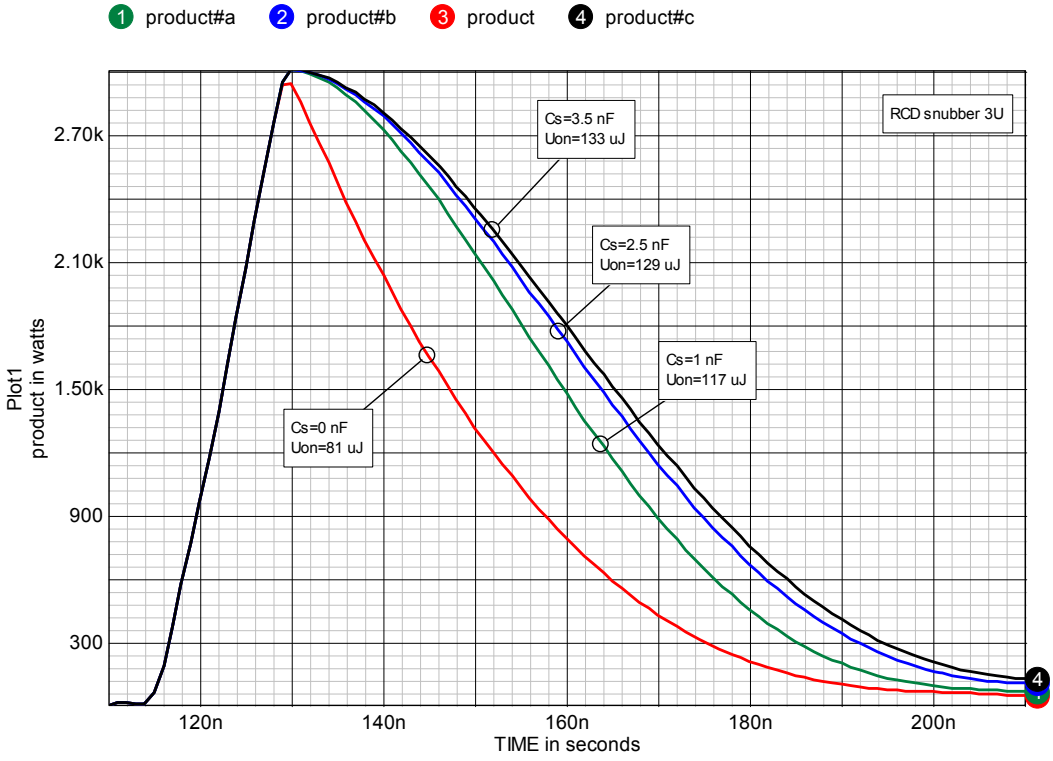


Figure 4-15, Turn-on power dissipation.

It is possible to trade a higher level of remnant charge on Cs (i.e. don't fully discharge Cs) during operation at the minimum on-time of Q1 for some reduction in turn-on dissipation by using a higher value for Rs. We could for example increase Rs from 49 to 100 Ohm. With Cs=2.5 nF, Utotal drops from 238 µJ to 210 µJ. A 10% reduction. However, Cs will now not be fully discharged so there will be a voltage step in Vds at turn-off. The voltage step can be seen at the beginning of the turn-off portion of the load line shown in figure 4-16.

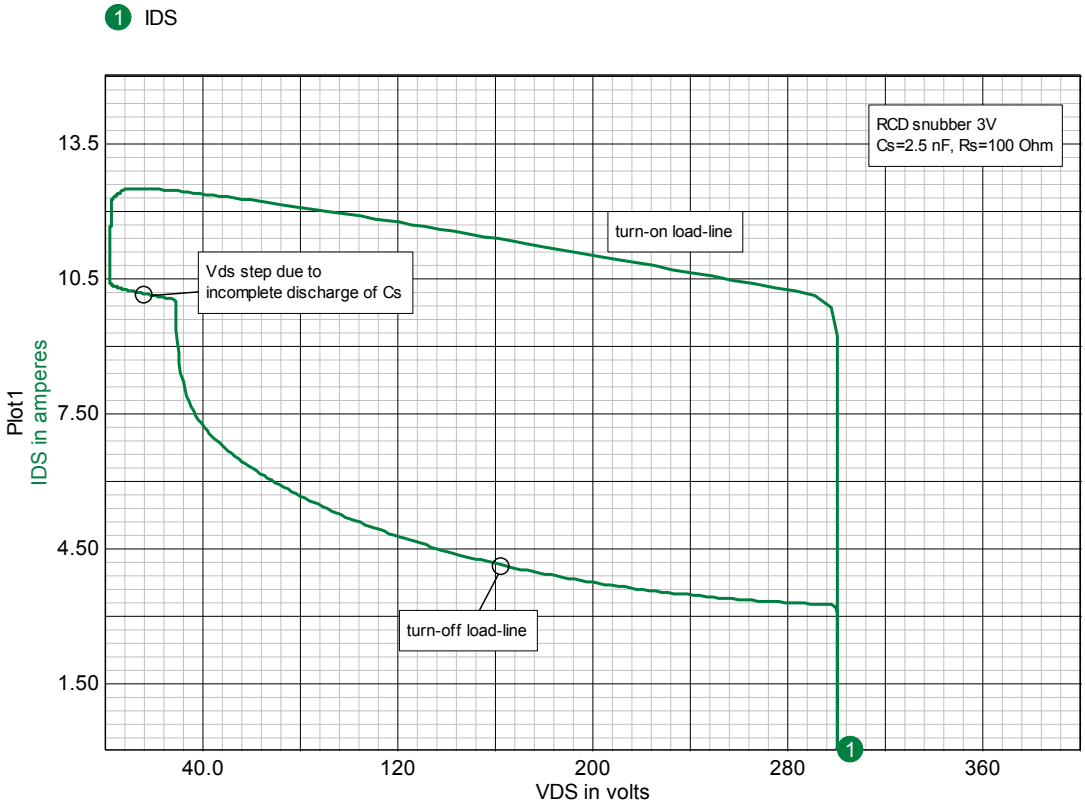


Figure 4-16, load-line with Rs=100 Ohm and Cs=2.5 nF.

The load-line will vary as the value for Cs is changed. Examples of load-lines for a range of Cs values are given in figure 4-17.

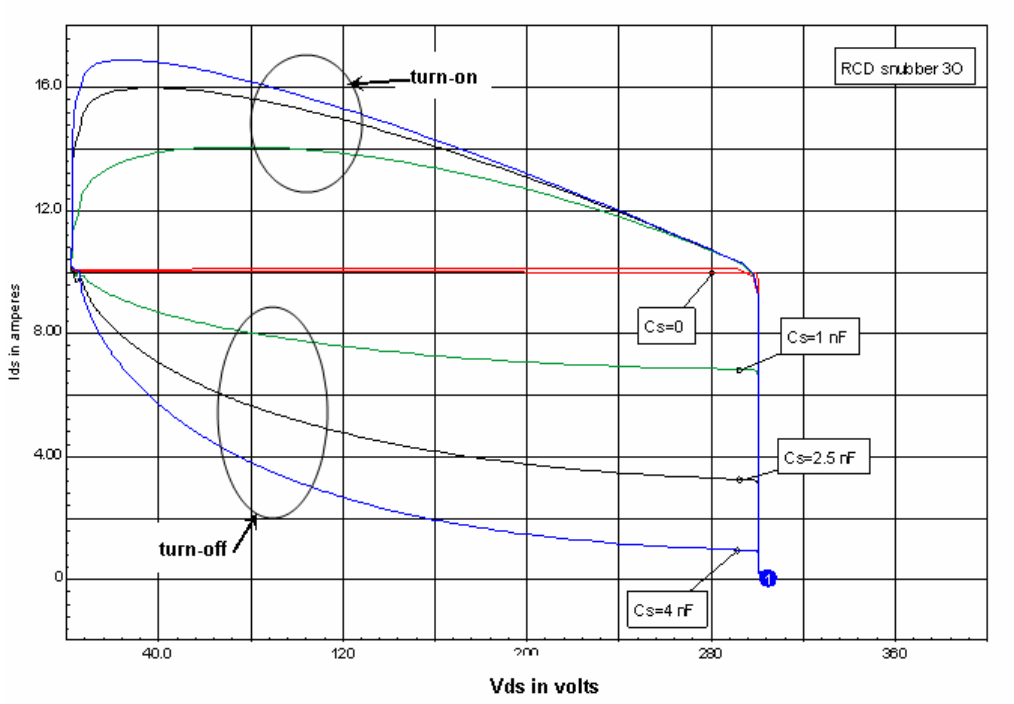


Figure 4-17, Load-lines for various values of Cs.

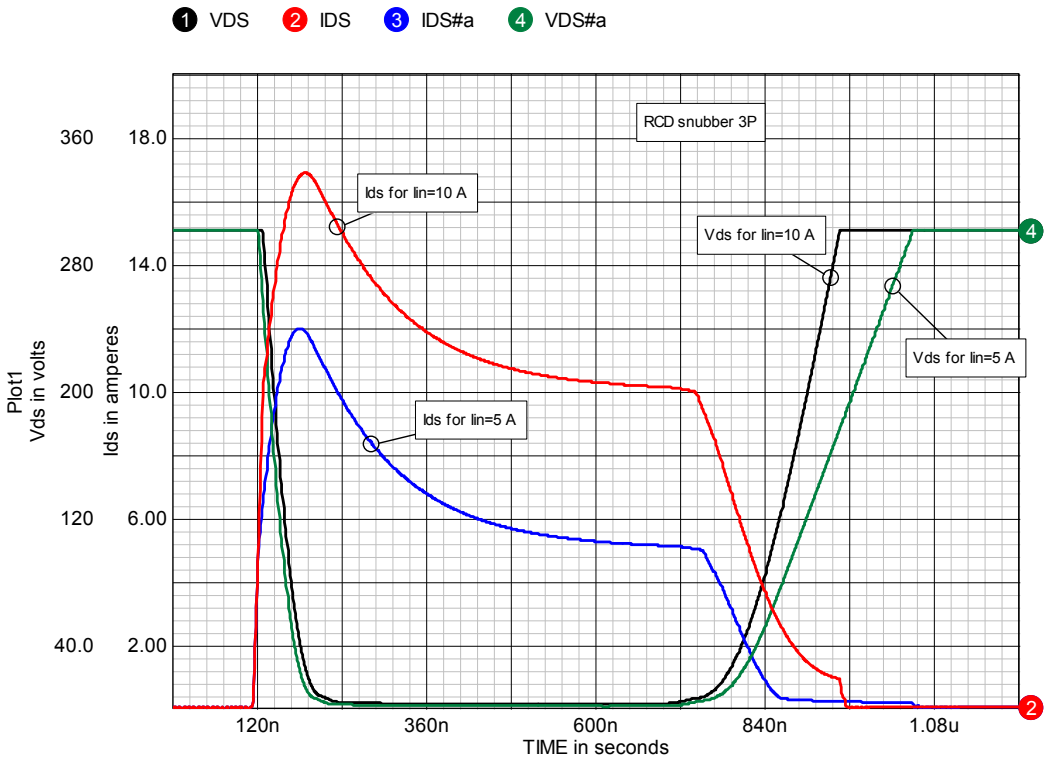


Figure 4-18, Effect of lower Iin on turn-off waveforms.

It is normal for a converter to operate over a range of load currents. The effect of the snubber on switch waveforms will change as the load current varies. Figures 4-18 and 4-19 demonstrate this effect.

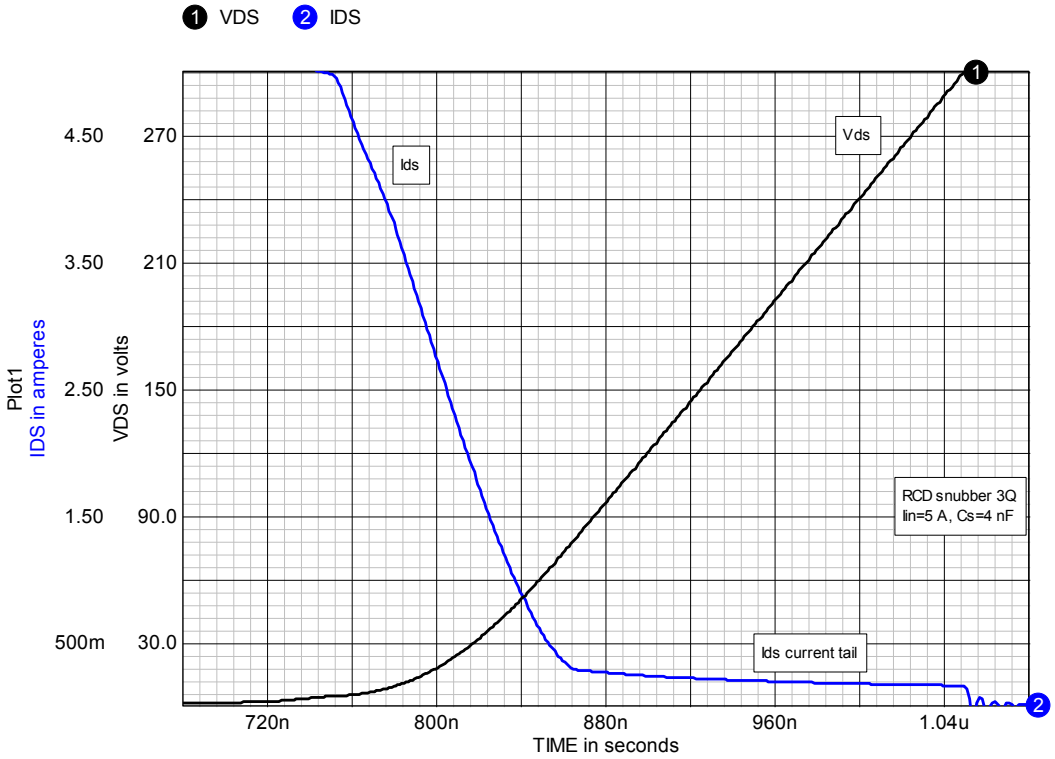


Figure 4-19, A closer look at the Ids current tail at turn-off.

As the load current is reduced, d(Vds)/dt decreases and the turn-off time increases. The Ids knee disappears but is replaced by a small current tail. Figure 4-19 gives an expanded view of this current tail. This current tail is due to the switch shunt capacitance (Coss in this example). The current flows, even though the channel in the MOSFET switch has turned off, due to d(Vds)/dt. The current ceases when d(Vds)/dt = 0. The effect of lower load current is much like increasing the value of Cs: d(Vds)/dt is reduced and the turn-off time gets longer. At low load currents the effective duty cycle of the switch may be much longer than the duty cycle of the drive waveform which will impact the control characteristics. In some cases the behavior at light load may limit the maximum usable value of Cs and the effectiveness of the snubber at full load.

Parasitic inductance and the turn-off snubber

Up to this point we have used ideal diodes and omitted parasitic inductances in the models. Real circuits of course have real diodes and will always have some parasitic inductance.

In normal operation the current in Ds will be zero, or very nearly so, when Q1 turns on. This means there will be little stored charge and a minimal reverse recovery current spike. In practice Ds does not have to be an fast recovery diode. D1 however, does have to be a fast diode and the turn-off snubber has no effect on the reverse recovery current spike in this diode which appears at Q1 turn-on.

An example with parasitic drain inductance is given in figure 4-20. Figure 4-21 shows the associated Vds and Ids waveforms.

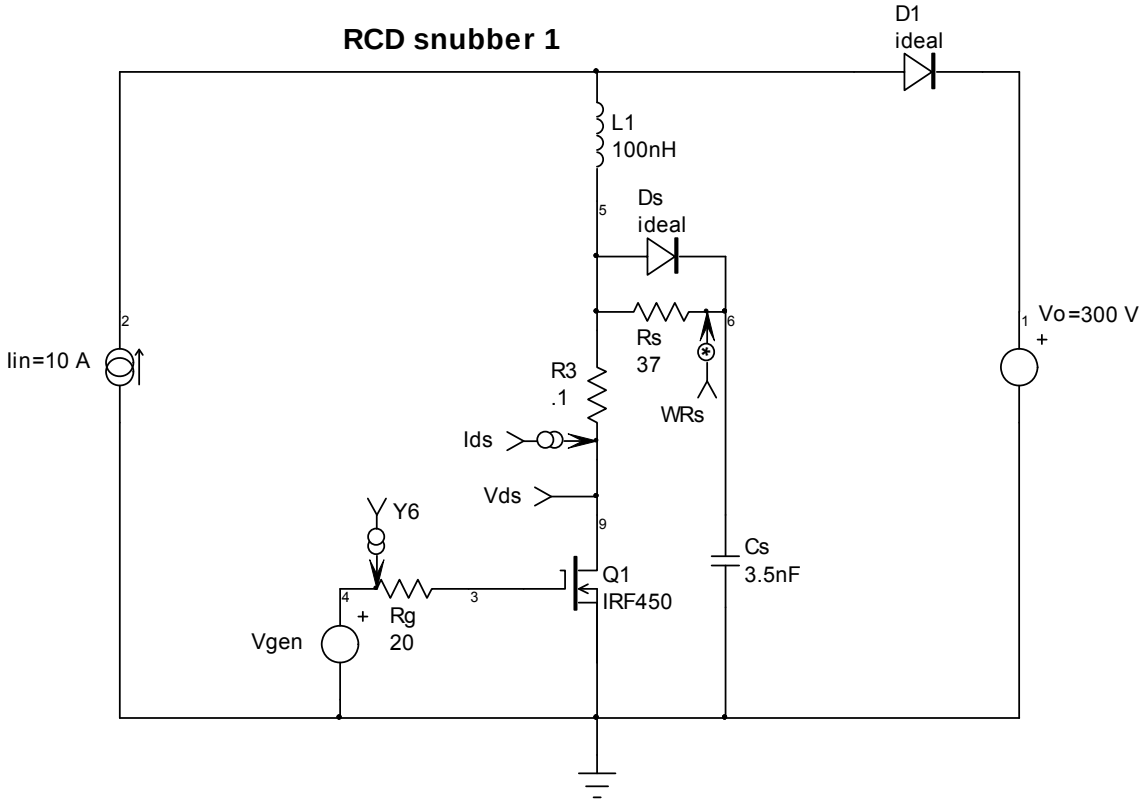


Figure 4-20, adding parasitic inductance (L1) in the drain of Q1.

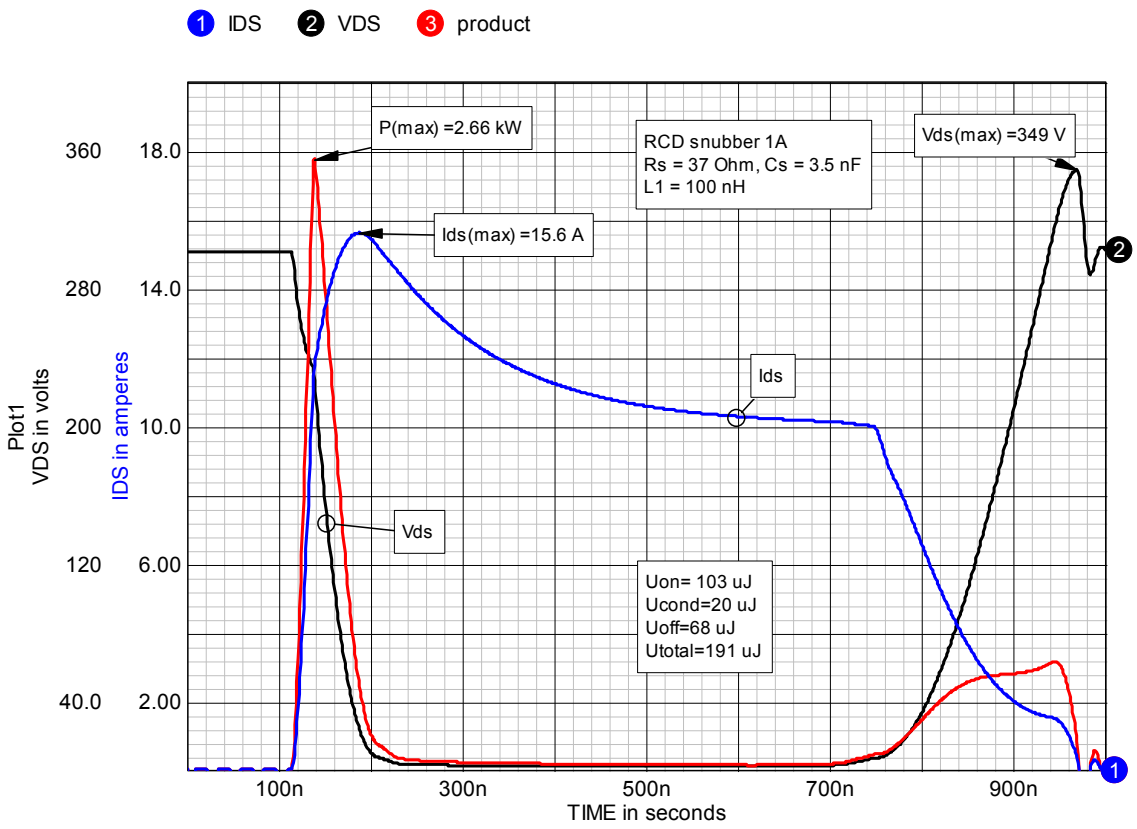


Figure 4-21, waveforms with parasitic drain inductance.

From the waveforms in figure 4-21 we can see that at turn-on L1 acts like a turn-on snubber, reducing the peak power (2.97 kW to 2.66 kW) and Utotal from 219 µJ down to 191 µJ. However, at turn-off there is now a voltage spike of about 50 V added to Vds.

The load-lines with and without parasitic inductance are shown in figure 4-22. The effect of the parasitic inductance is to improve the turn-on load-line but add ringing and voltage overshoot to the turn-off portion of the load-line.

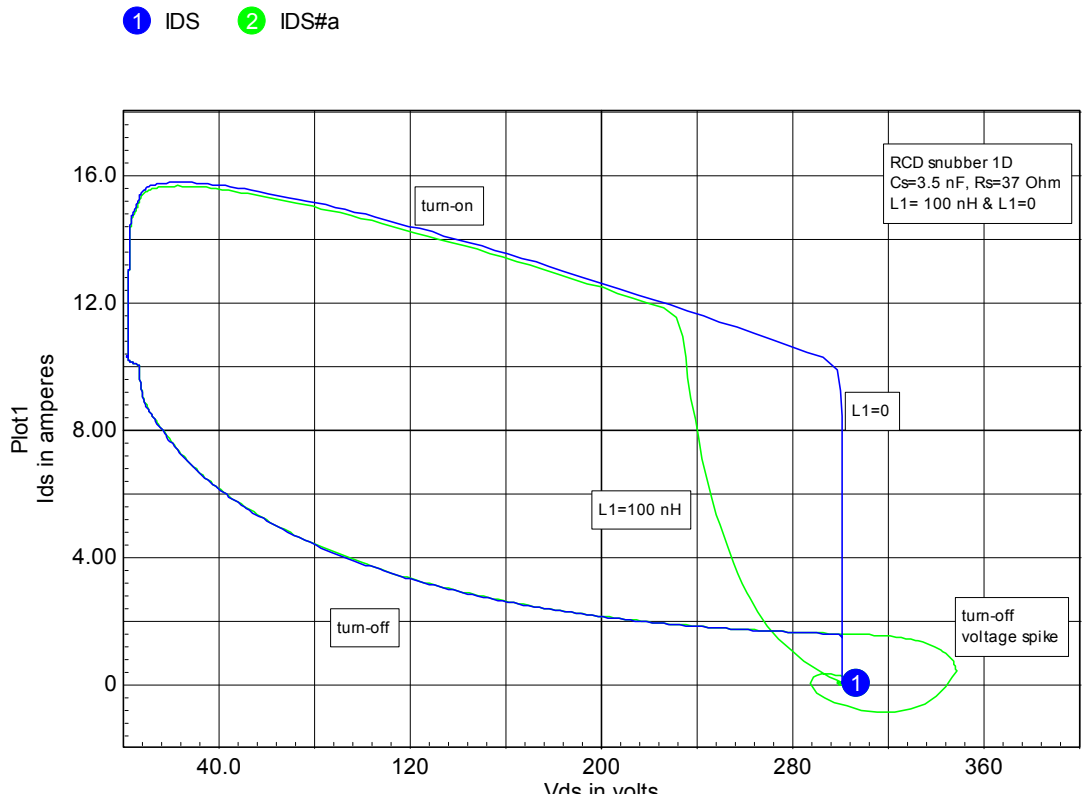


Figure 4-22, load-line with parasitic inductance.

The loop at the end of the turn-off portion of the load-line is due to Vds overshoot. The voltage spike can be reduced by making Cs larger. Rs provides some damping for the voltage spike.

The turn-on snubber

We can create a turn-on snubber by deliberately adding inductance in the drain and provide a mechanism for discharging the energy stored in this inductor. An example of an inductive turn-on snubber is given in figure 4-23. For the moment we will continue to let D1 be an ideal diode so we can examine the snubber operation but shortly we will have to use a real diode to get the complete picture. Ls is the turn-on snubber with Ds and Rs providing a means for discharging the energy in Ls at Q1 turn-off.

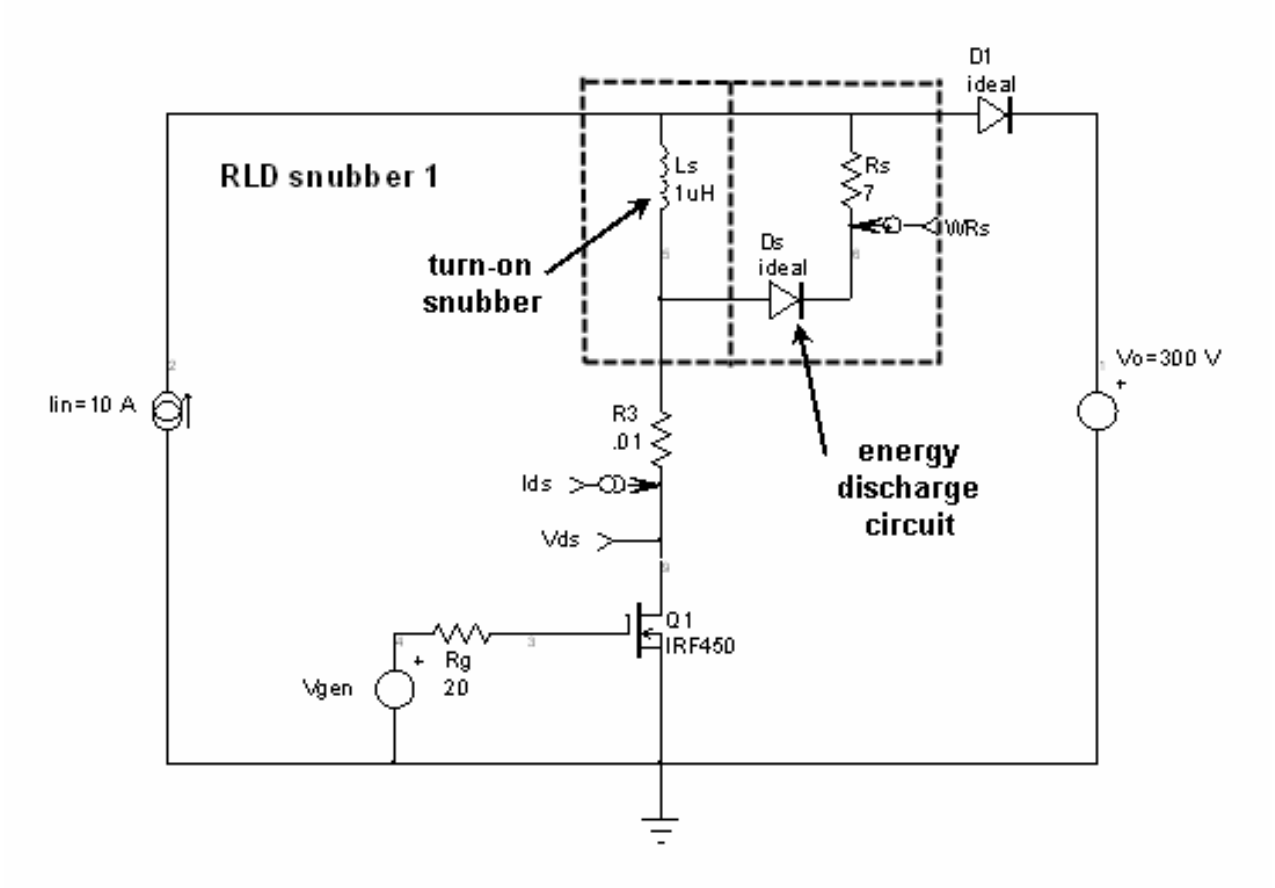


Figure 4-23, Typical inductive turn-on snubber.

At Q1 turn-on d(Ids)/dt) is limited by Ls. At Q1 turn-off the energy stored in Ls is dissipated in Rs via Ds.

Typical switching waveforms are shown in figure 4-24. At turn-on, Vds starts to fall before Ids reaches full amplitude. The result is a much lower peak power (≈1 kW) at turn-on rather than the 3 kW without the snubber. At turn-off however, the peak power is still 3 kW and there is now a voltage spike due to the current from Ls flowing through Rs. Utotal has been reduced from 315 µJ, in the un-snubbed case, to 300 µJ. The energy in Ls is dissipated in Rs, adding another 25 µJ so the total circuit loss is actually increased slightly.

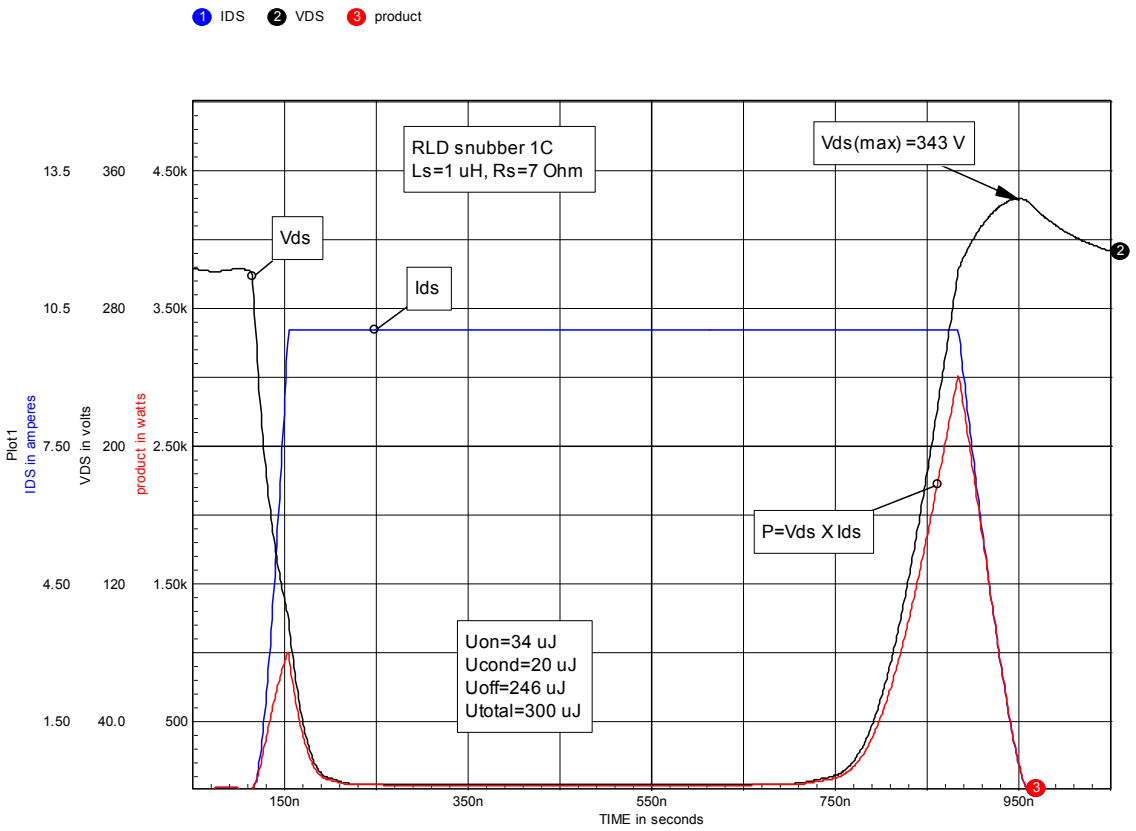


Figure 4-24, typical Q1 waveforms with a turn-on snubber.

An expanded view of the turn-on waveforms with and without the snubber is given in figure 4-25. Note how much these waveforms resemble the turn-off waveforms using the RC-diode turn-off snubber except that the voltage and current waveforms are interchanged. The reason for this similarity is that the two snubbers are electrical duals:

> *The turn-on snubber is the series connection of an inductor and a switch turning on, while the turn-off snubber is a parallel combination of a capacitor and a switch turning off.*

Comparing the waveforms with and without the snubber, we see that d(Ids)/dt and d(Vds)/dt, down to the point of the knee, are reduced.

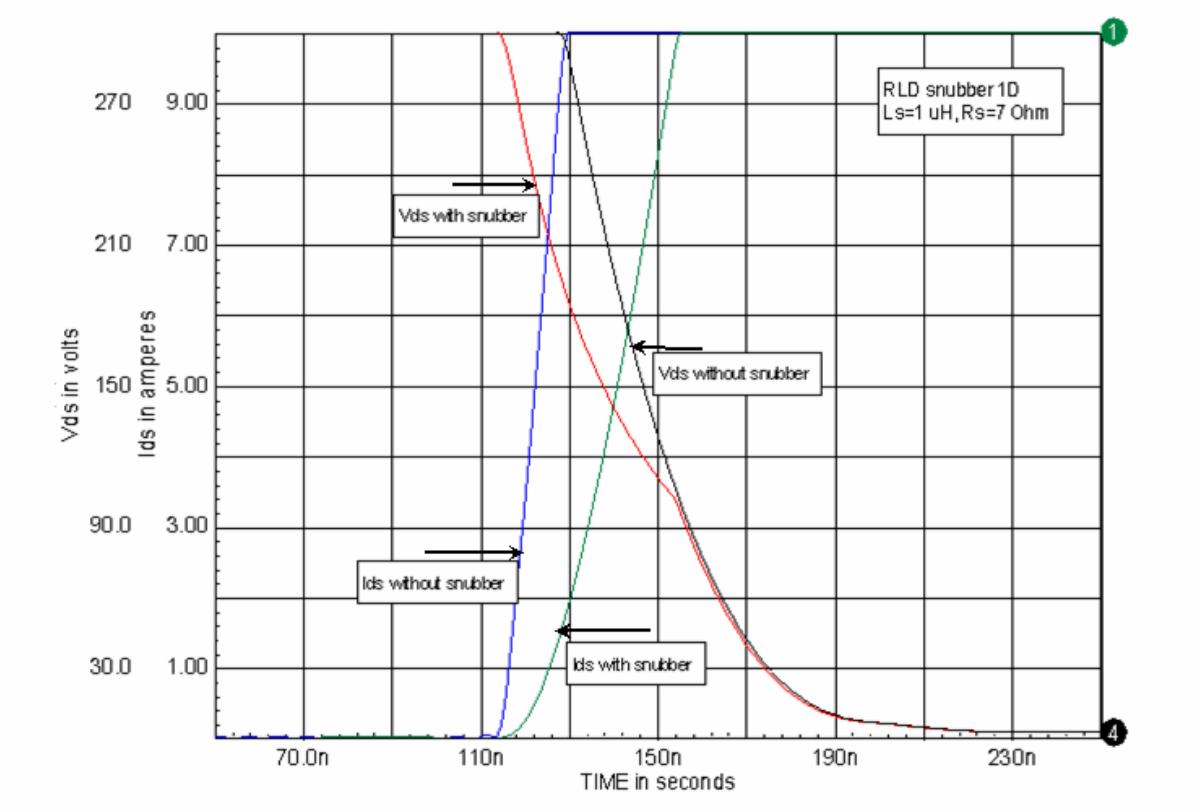


Figure 4-25, turn-on waveform with and without the snubber.

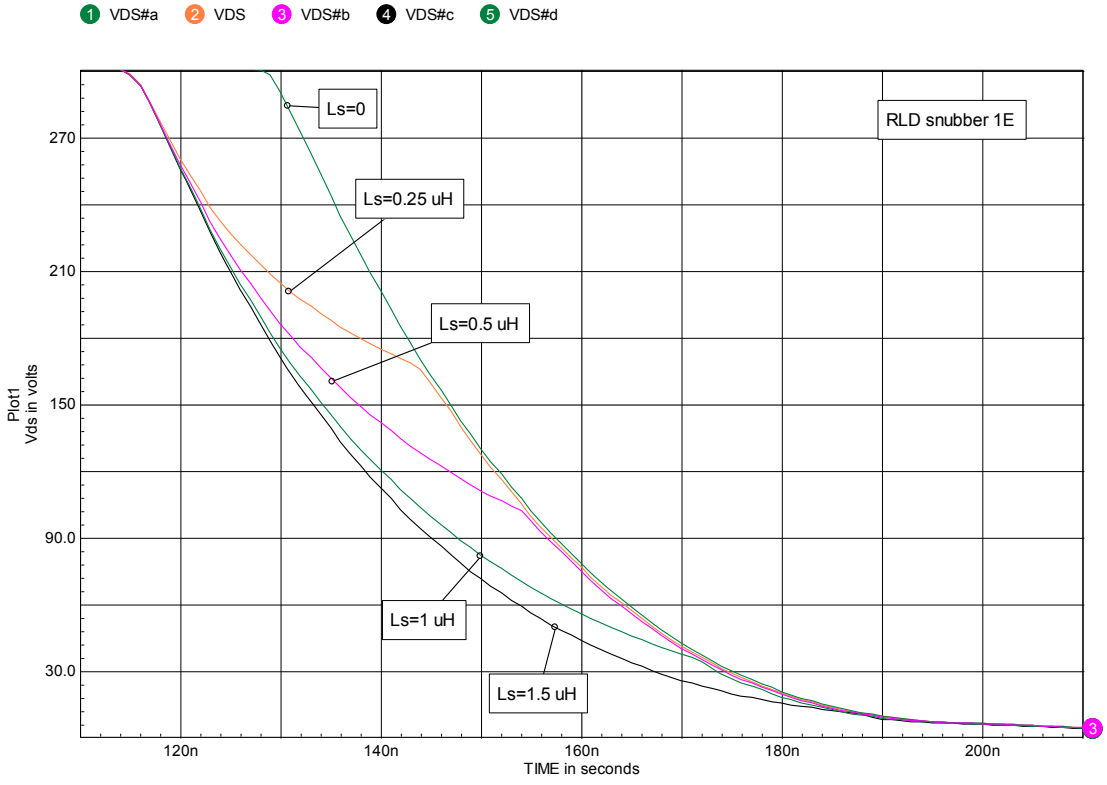


Figure 4-26, effect of the value for Ls on turn-on Vds waveforms.

The effect of different values of Ls on the turn-on waveforms is illustrated in figures 4-26 and 4-27.

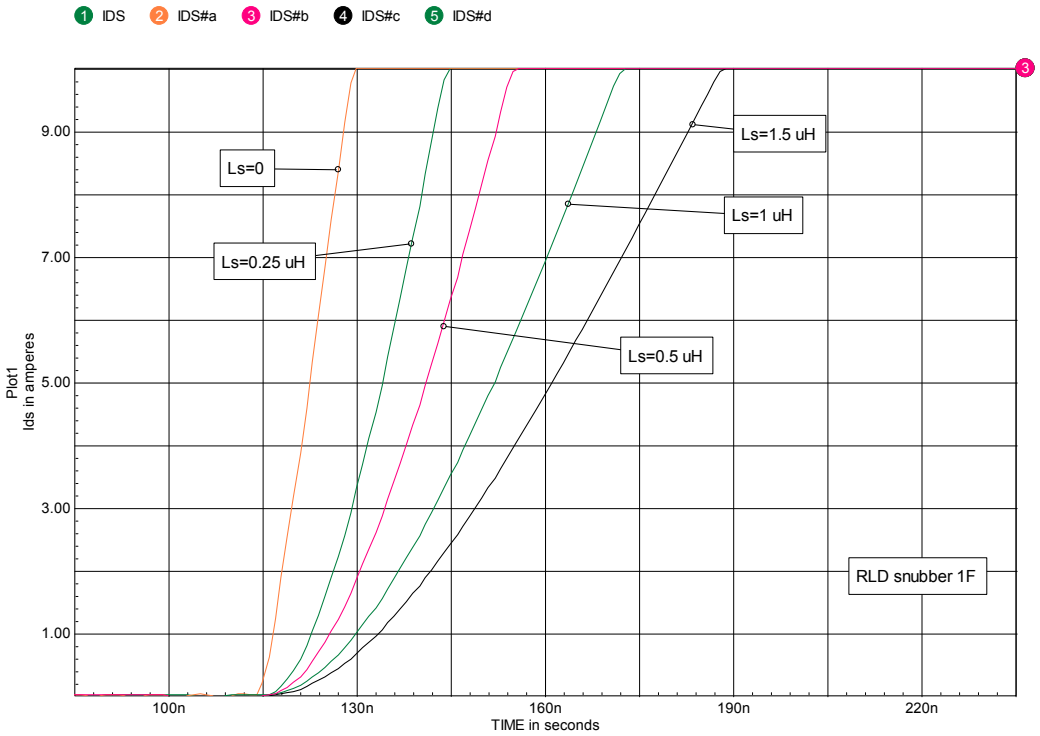


Figure 4-27, effect of the value for Ls on turn-on Ids waveforms.

Additional Cgd can alter the turn-on waveforms as shown in figure 4-28. This is similar to what we saw for the turn-off snubber.

Figure 4-29 shows the effect of different values for Ls on the Vds voltage spike at turn-off when using the turn-on snubber. In the case of the capacitive turn-off snubber we had a current spike on Ids at turn-on due to the discharge of Cs. Similarly, for the turn-on snubber there is a voltage spike on Vds due to the discharge of Ls. The larger we make Ls, the larger the voltage spike will be for a given value of Rs. If we make Rs smaller then the spike will be reduced but the discharge time will increase. The minimum value for Rs is that which allows most of the energy in Ls to be dissipated during the minimum off-time of Q1. This, along with the current at turn-off, sets a minimum value for the voltage spike.

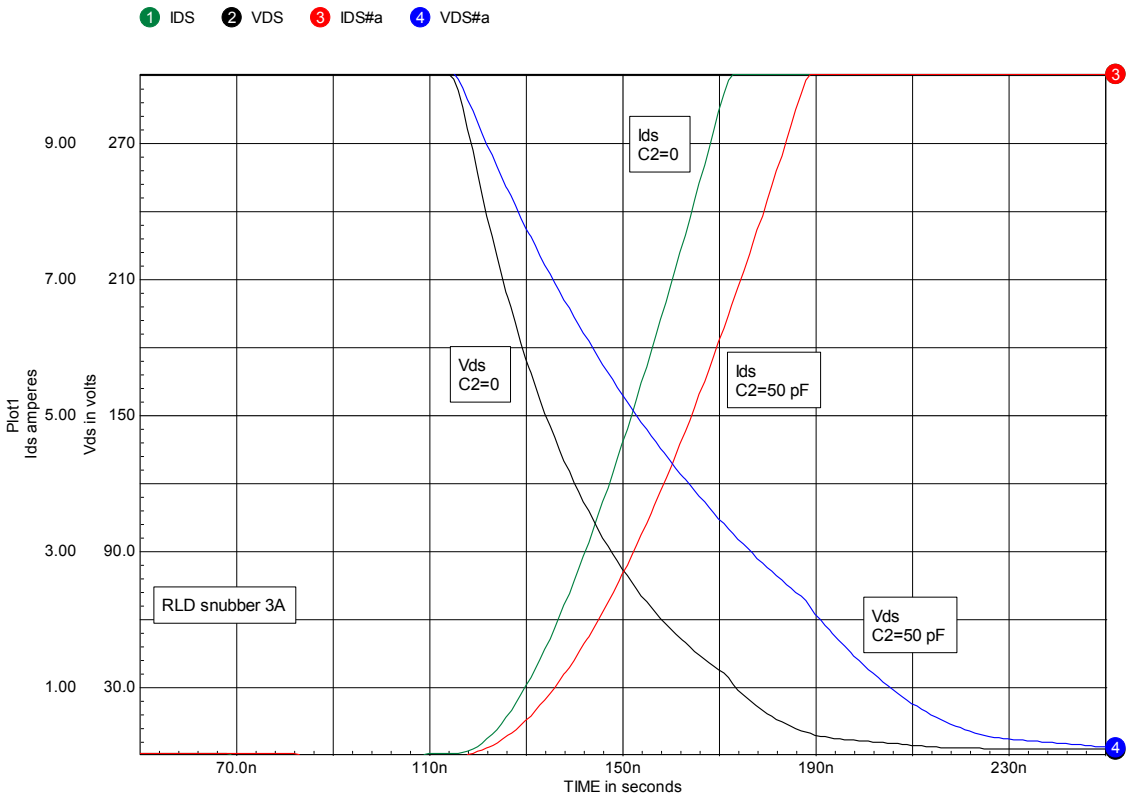


Figure 4-28, effect of additional gate to drain capacitance on turn-on waveforms.

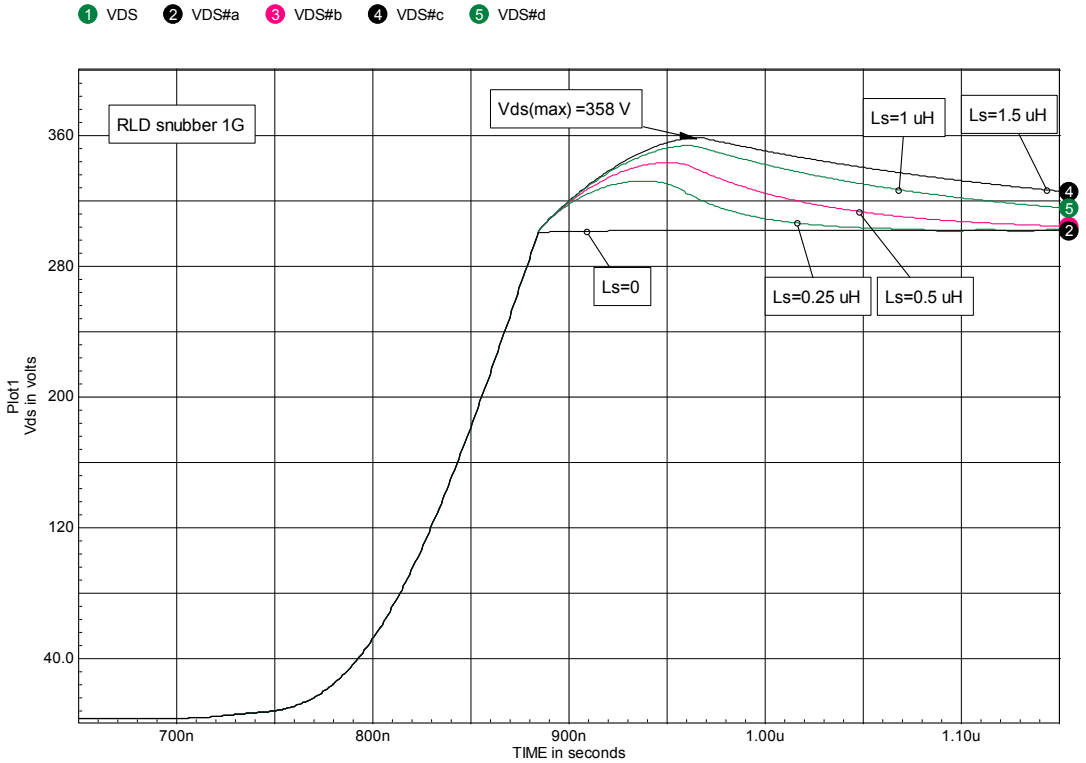


Figure 4-29, Vds overshoot at turn-off for various values of Ls.

Load-lines associated with the various values of Ls are shown in figure 4-30.

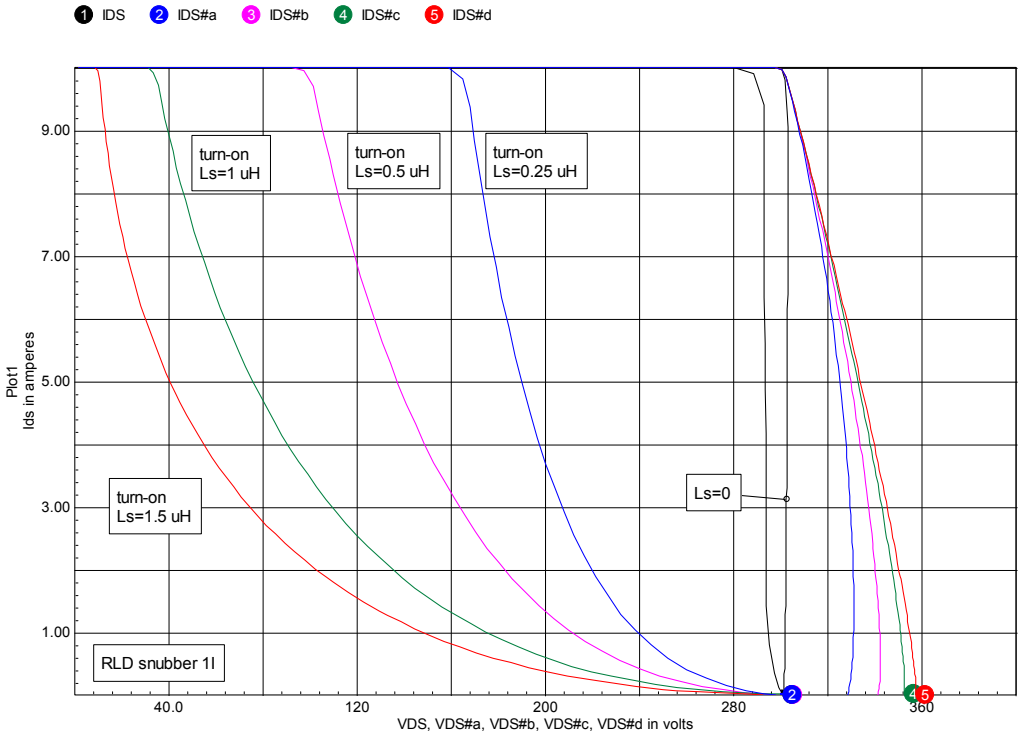


Figure 4-30, load-lines associated with various values of Ls.

An examination of the power dissipation in Q1 as the value for Ls is varied will give us some insight as to why the turn-on snubber seems to provide no improvement in total circuit loss and in fact appears to increase the total circuit loss. The turn-off power dissipation waveforms are given in figure 4-31 for various values of Ls along with values for Uon, Uoff and Utotal.

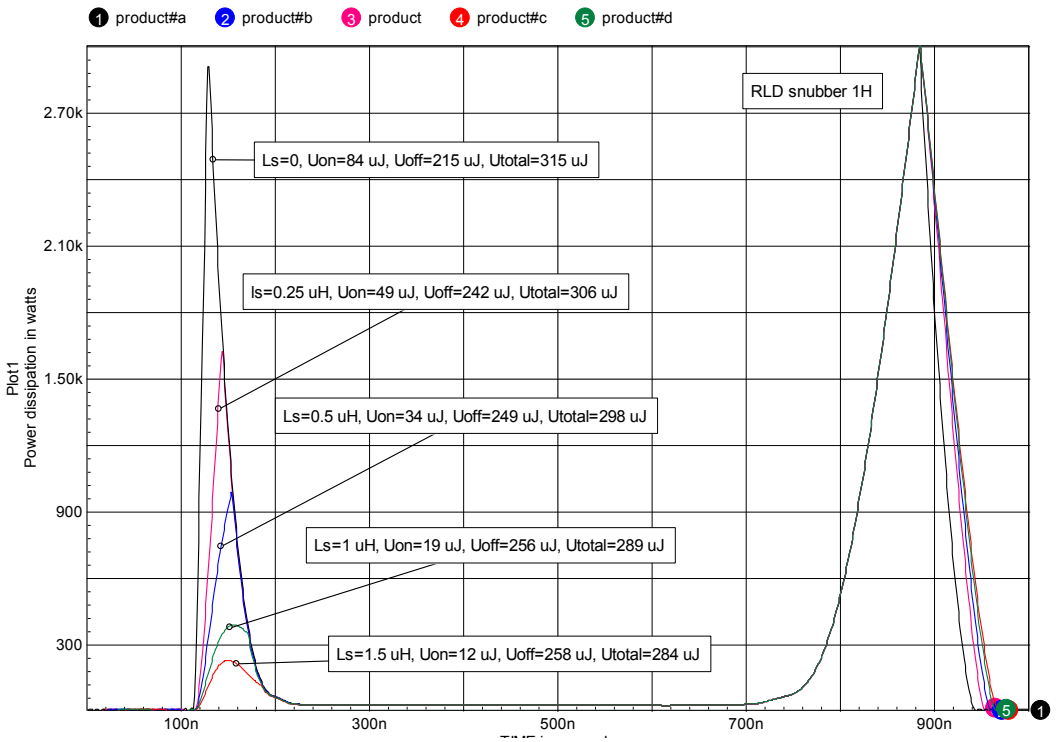


Figure 4-31, power dissipation and total energy loss for various values of Ls.

At turn-on both the peak power and the energy loss during turn-on fall quickly as the value of Ls is increased but Utotal only falls slowly. The reason for this is the increase in switch dissipation at turn-off, as shown by the broadening of the turn-off power waveform. The increased loss at turn-off can be understood by examining the turn-off waveforms in figure 4-24. Ids does not begin to fall until Vds=Vo, which in this example is 300 V. While Ids is falling, Vds increases above Vo due to the discharge of Ls, which increases the power loss. The larger the value of Ls, the higher the voltage spike and the greater the power loss at turn-off.

> *To obtain the lowest total switch loss with this snubber, it is vital to use the lowest possible value for Rs because that will reduce Vds during the Ids fall time.*

In the case of the turn-off snubber we saw a similar increase in power dissipation at turn-on (figure 4-15).

Turn-on snubber with a real diode

We have assumed D1 to be ideal, i.e. no reverse recovery current spike. It's time to examine the circuit behavior using a real diode (an HFA08TB60) as shown in figure 4-32.

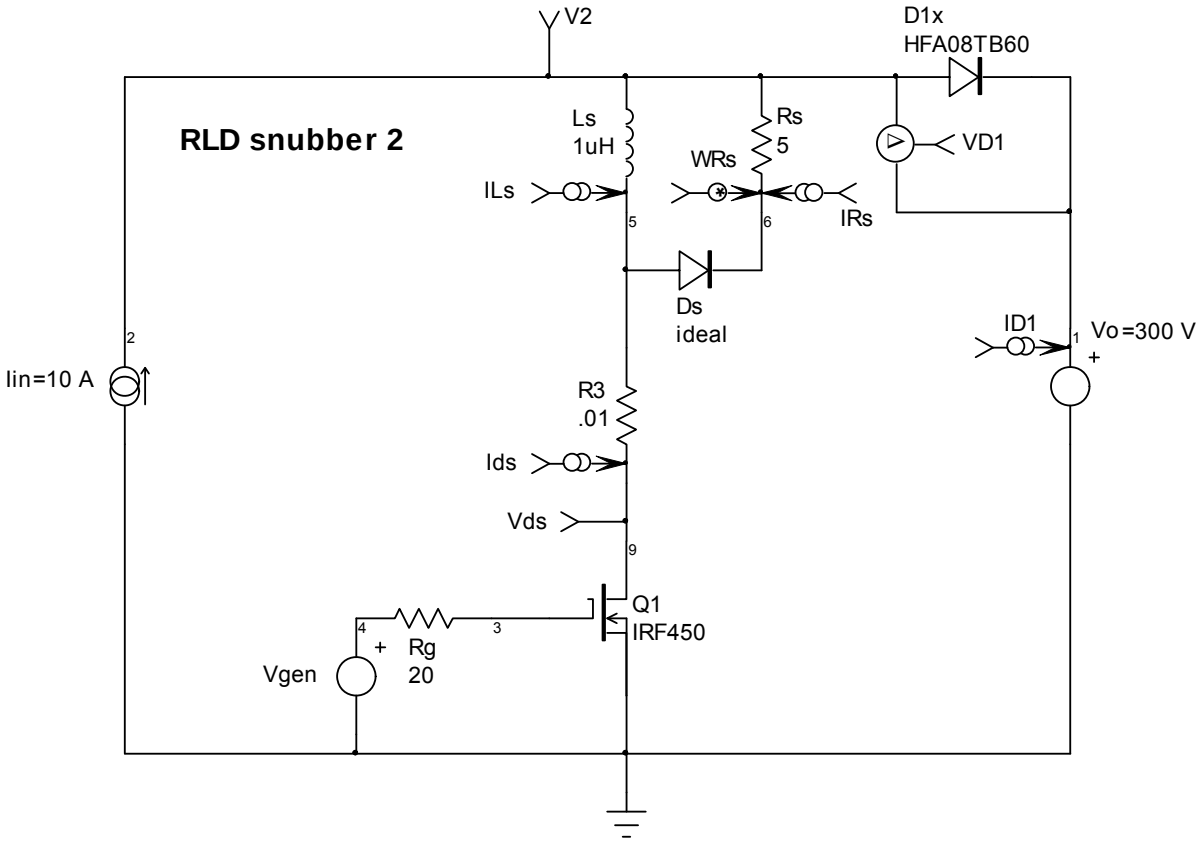


Figure 4-32, A turn-on snubber with D1 a real diode.

To illustrate how much the improvement is gained by using the turn-on snubber in a circuit with a real diode we will start with the voltage and current waveforms for Q1 and D1, without a snubber. These are shown in figures 4-33 and 4-34.

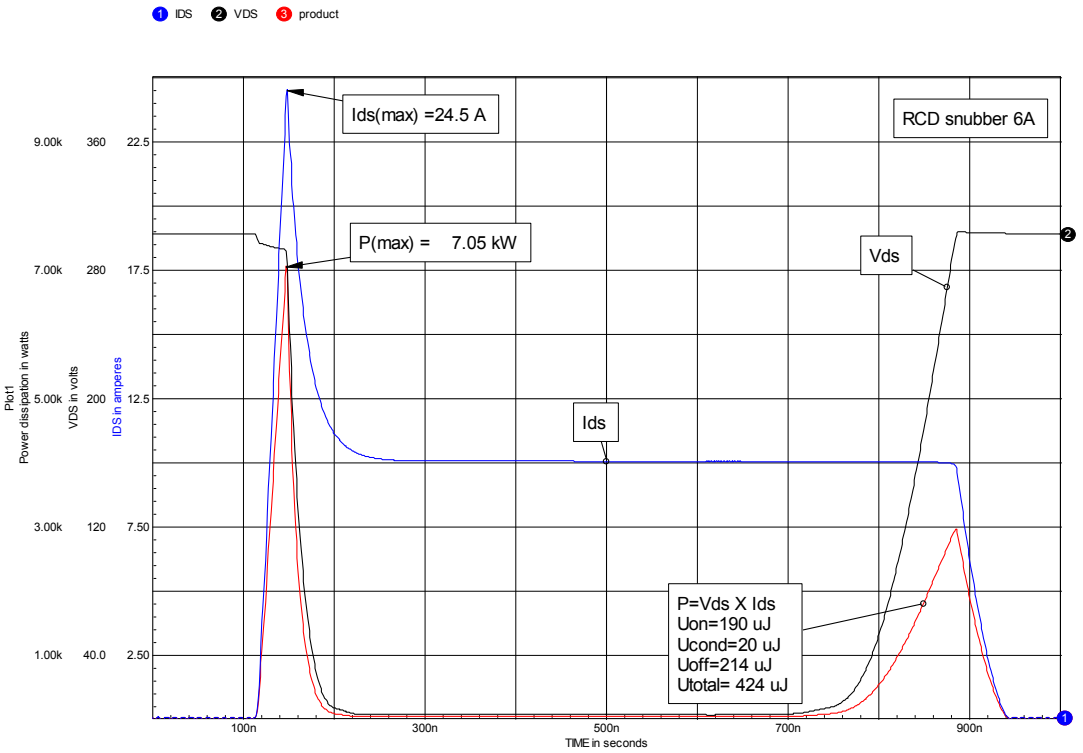


Figure 4-33, Ids and Vds waveforms with D1 a real diode without a snubber.

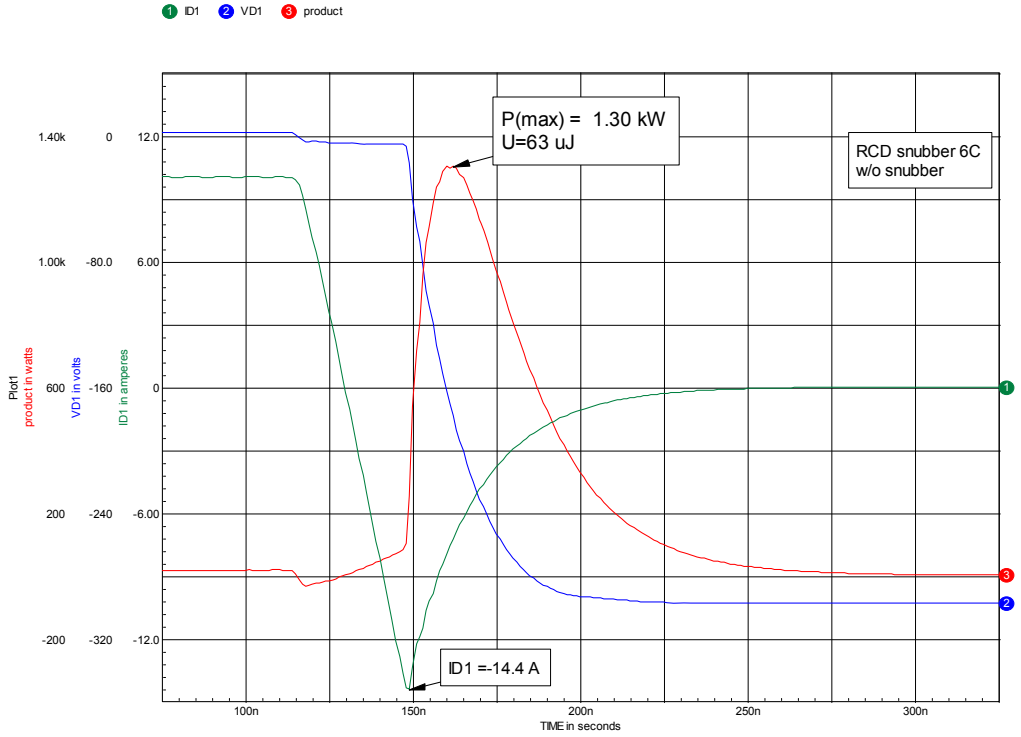


Figure 4-34, Waveforms for D1 without a snubber.

Without the snubber, the switching loss in Q1 is 424 µJ and in D1, 63 µJ, for a total circuit loss of 487 µJ per switching cycle in the two semiconductors. Uon is now nearly the same as Uoff. Clearly a real diode has considerable effect on circuit operation and needs to be considered.

Waveforms for Q1, with the turn-on snubber (Ls=1 uH), are shown in figure 4-35.

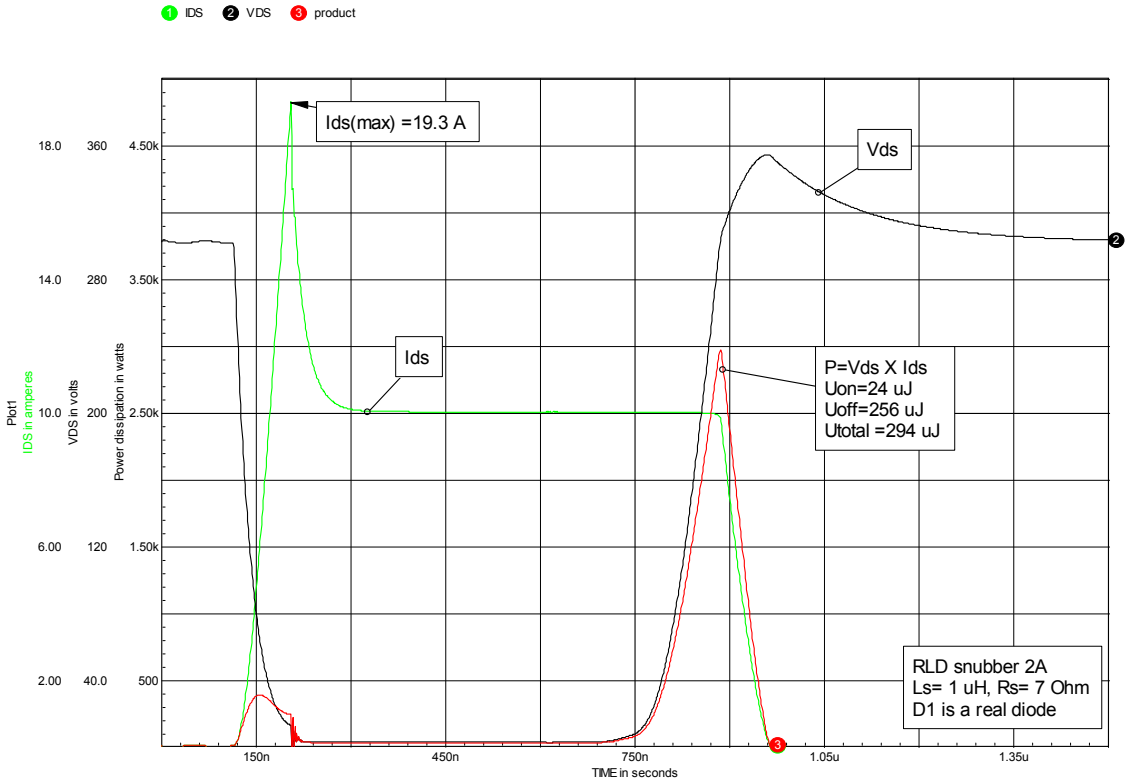


Figure 4-35, Ids and Vds waveforms with D1 a real diode and with a turn-on snubber.

There is a decrease in the peak value of Ids (from 24.5 A down to 19.3 A) and while useful, this is not the primary impact of the snubber. Without the snubber the peak power at turn-on is above 7 kW and the total switch loss per cycle is 424 µJ. With the snubber, the peak power at turn-on is reduced to 450 W and the total energy loss per cycle is now 294 µJ. This is a significant improvement and illustrates a major reason that the inductive turn-on snubber is so often used to reduce losses due to diode recovery.

The reason for the dramatic decrease in peak power at turn-on is shown in figure 4-36.

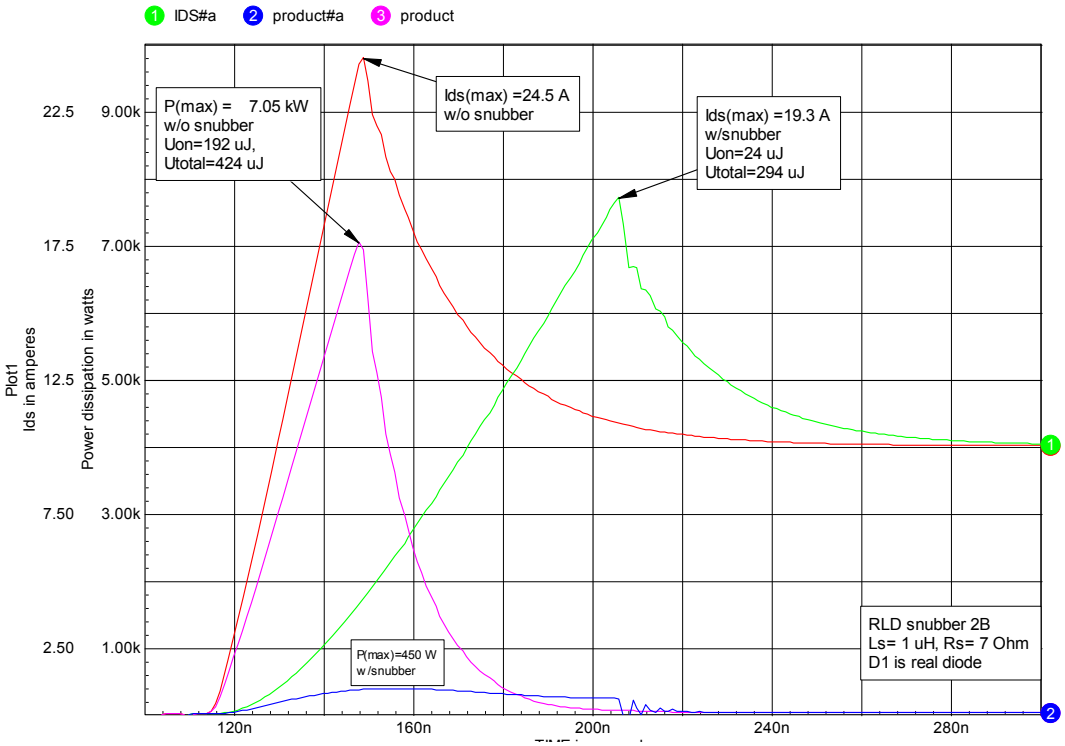


Figure 4-36, turn-on waveforms with and without the snubber.

The primary effect of the turn-on snubber is to make Vds fall sooner and delay the rise of Ids. This results in reduced peak power (from 7 kW to 450 W) and reduced Uon (from 192 µJ to 24 µJ).

Figure 4-37 shows the current waveforms in Q1, Ls and Rs. Note that there are <u>two</u> current pulses in Rs corresponding to two energy discharge intervals for Ls through Rs (IRs). The first discharge is initiated when the reverse current in D1 reaches its peak and begins to decline. ILs has to fall from the combination of Iin plus ID1 reverse = 19.4 A to ILs= 10.2 A during Q1 conduction. This means that the energy stored in Ls due to D1 recovery has to be discharged and it does this by dissipating the energy in Rs. The second discharge interval for Ls is initiated by Q1 turn-off. At this point ILs has to fall from 10 A to zero. This stored energy is also dissipated in Rs. Utotal in Rs for this example is 83 µJ.

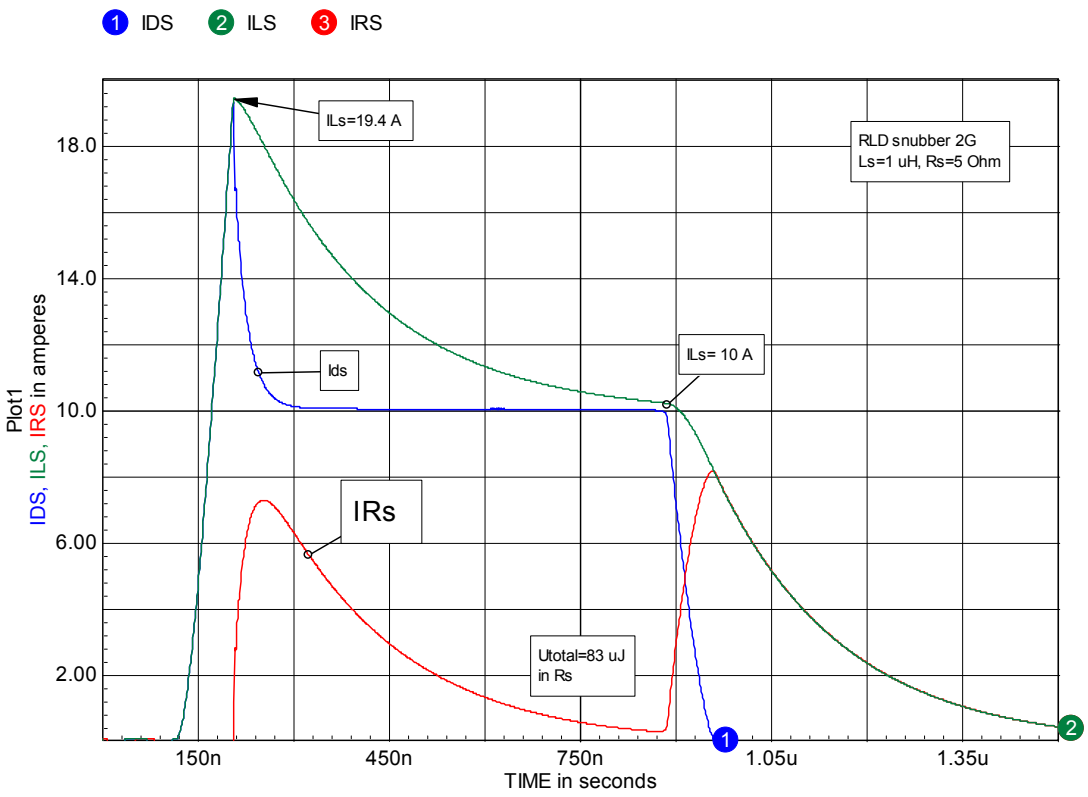


Figure 4-37, Current waveforms in Q1, Ls and Rs.

But wait a minute! The peak energy in Ls (Upeak) is much larger than this: Upeak=Ls*ILs^2/2= 188 µJ. Where has the remaining 105 µJ been dissipated if not in Rs? In the first discharge interval U=(19.4^2-10.2^2)/2 = 138 µJ but the dissipation in Rs=39 µJ. It turns out that a lot of this "missing" energy is dissipated in D1. Voltage and current waveforms for D1 are given in figure 4-38. The dissipation in D1 is about 63 µJ, most of which occurs during reverse recovery. The remaining 40 µJ is dissipated in Q1.

At Q1 turn-off the dissipation in Rs=44 µJ and U=10.2^2/2 = 52 µJ. That tells us that about 8 µJ from Ls are dissipated in Q1. We could use the modeling value for Rs dissipation but a conservative power rating for Rs would be simply to assume all the energy (Upeak) was dissipated in Rs.

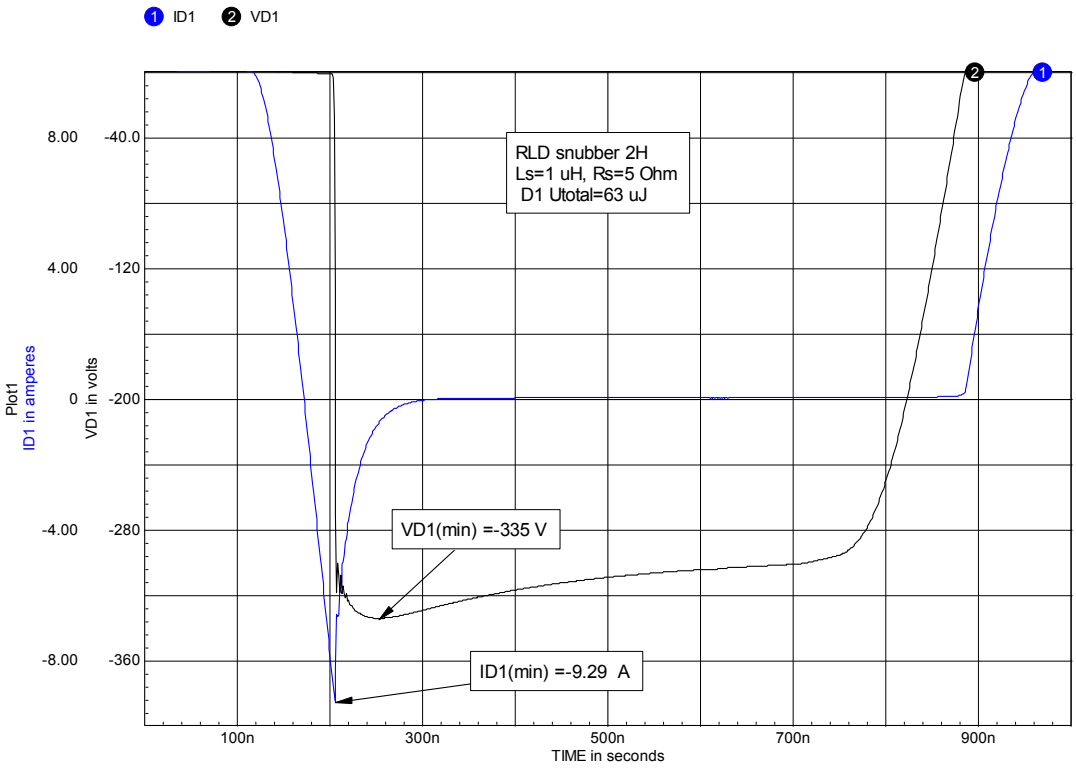


Figure 4-38, ID1 and VD1 waveforms.

Comparing waveforms in figures 4-34 (without the snubber) and 4-38 (with the snubber), we see that the peak reverse current in D1 has been reduced from 14.4 A to 9.3 A but there is now a 35 V voltage spike added to the reverse voltage. The energy loss in D1 per switching cycle has not changed however. The penalty for D1 from the use of the snubber is to increase the reverse voltage.

The total switching loss per cycle was 487 µJ, without the snubber. With the snubber this is reduced to 440 µJ. Not a huge reduction but still useful. The loss in Q1 however, has dropped from 424 µJ to 294 µJ! That is significant.

A comparison of the load-lines with and without the snubber is given in figure 4-39.

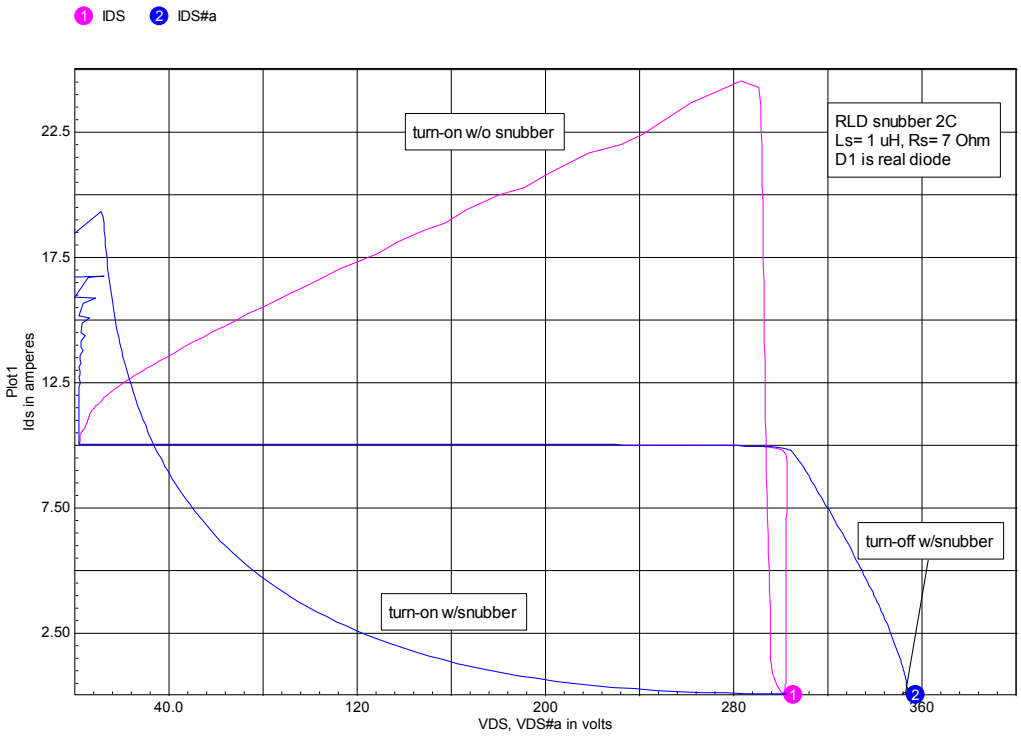


Figure 4-39, comparison of load-lines with and without the turn-on snubber.

When the behavior of a real diode is taken into account, the turn-on snubber is shown to be very effective for reducing switching loss and stress at turn-on.

The combination snubber

Turn-on and turn-off snubbers can used simultaneously as shown in figure 4-40. It is possible to retain the advantages of both snubbers and to use one snubber to minimize the switching stresses introduced by the other. Working together, the total switching loss can be greatly reduced.

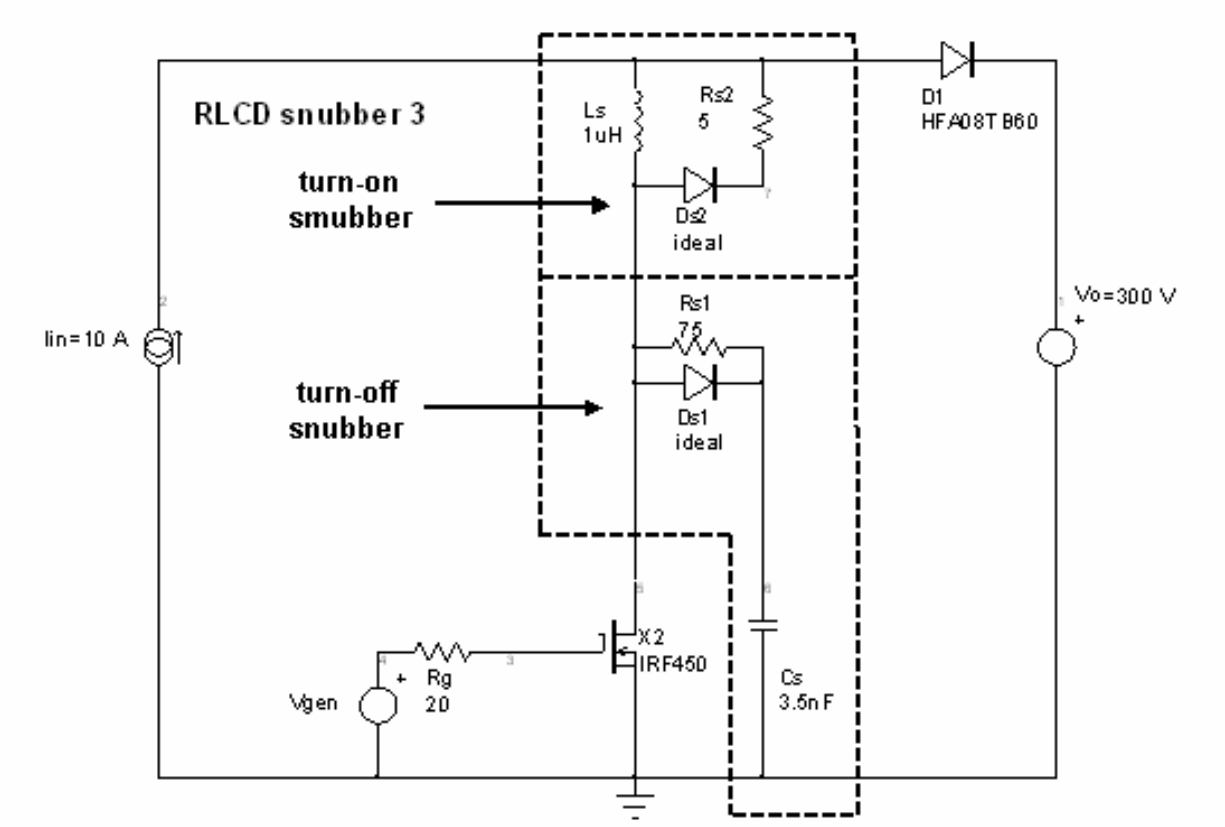


Figure 4-40, An example using both turn-on and turn-off snubbers simultaneously.

In this example I have chosen to use the snubber component values from the earlier examples and to include a real diode for D1. This does not necessarily give the optimum performance but is a reasonable starting point. One advantage of this circuit is that there are two snubber resistors. This allows us to optimize both turn-on and turn-off independently.

Ids and Vds waveforms associated with figure 4-40 are shown in figure 4-41.

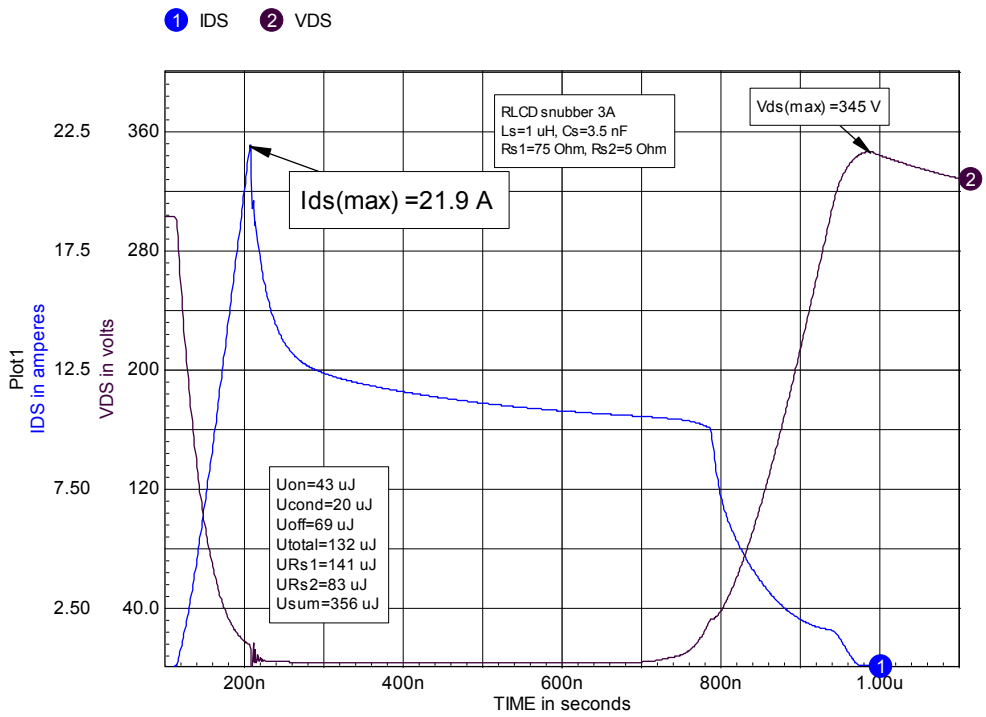


Figure 4-41, Ids and Vds waveforms associated with the circuit in figure 4-40.

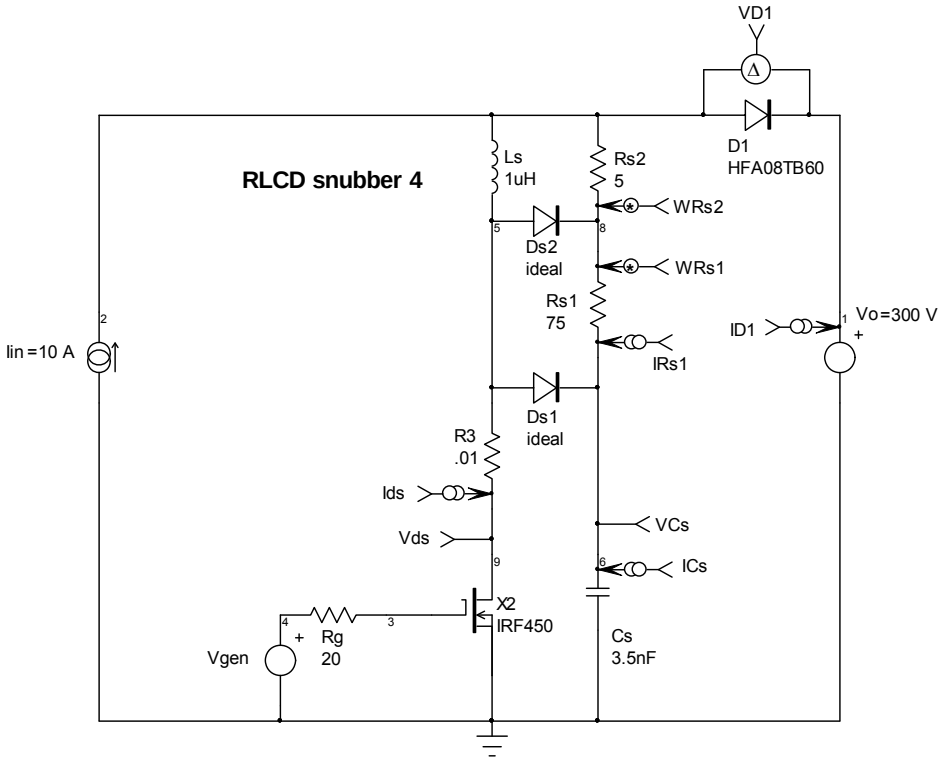


Figure 4-42, Rs1 connected to discharge Cs through Ls.

The combination of the two snubbers has reduced the total switch loss to 132 µJ per cycle which is a reduction of nearly 70% from 424 µJ without the snubber. However, if we add back in the losses in Rs1 and Rs2, the sum is 356 µJ, only a modest decrease overall.

We can make a small improvement in the snubber operation by connecting Rs1 so that it discharges Cs through Ls at Q1 turn-on as shown in figure 4-42.

The waveforms associated with this change are shown in figure 4-43.

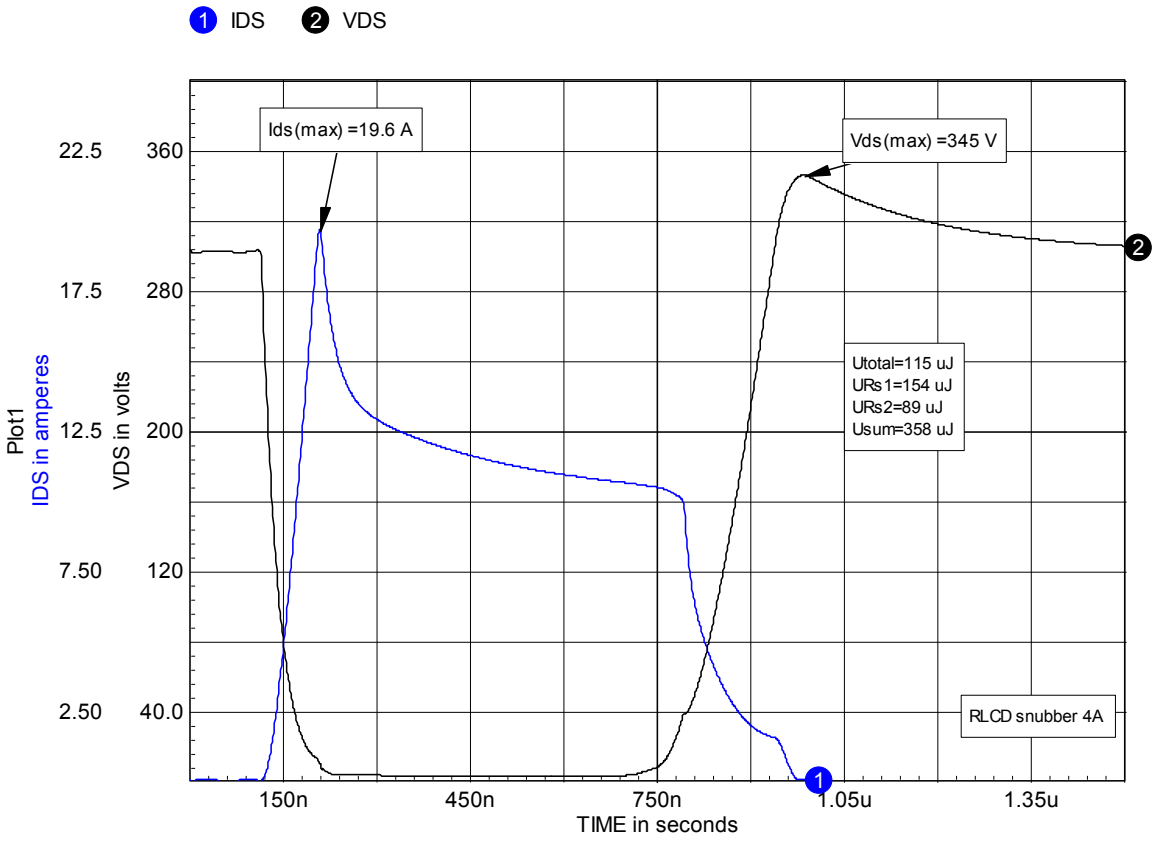


Figure 4-43, Vds, Ids and power dissipation with Rs connected to discharge Cs through Ls.

Comparing figures 4-41 and 4-43, we see that the effect of routing discharge of Cs through Ls has a number of benefits. The peak power at turn-on is cut almost in half (from 645 W to 380 W), Q1 loss is reduced by another 10% and the peak current at turn-on is also reduced by 10%. The sum of all the losses including Rs1 and Rs2

however, is still essentially the same. The performance of this snubber arrangement could be optimized bit by varying the values of Ls, Cs, Rs1 and Rs2. The load-line for this combined snubber is shown in figure 4-44. For comparison a resistive load-line going from Vds=300 V to Ids=10 A is shown. Over much of the transition the power with the snubber is actually lower than for a resistive load. However, we still have the current spike at turn-on and a voltage spike at turn-off.

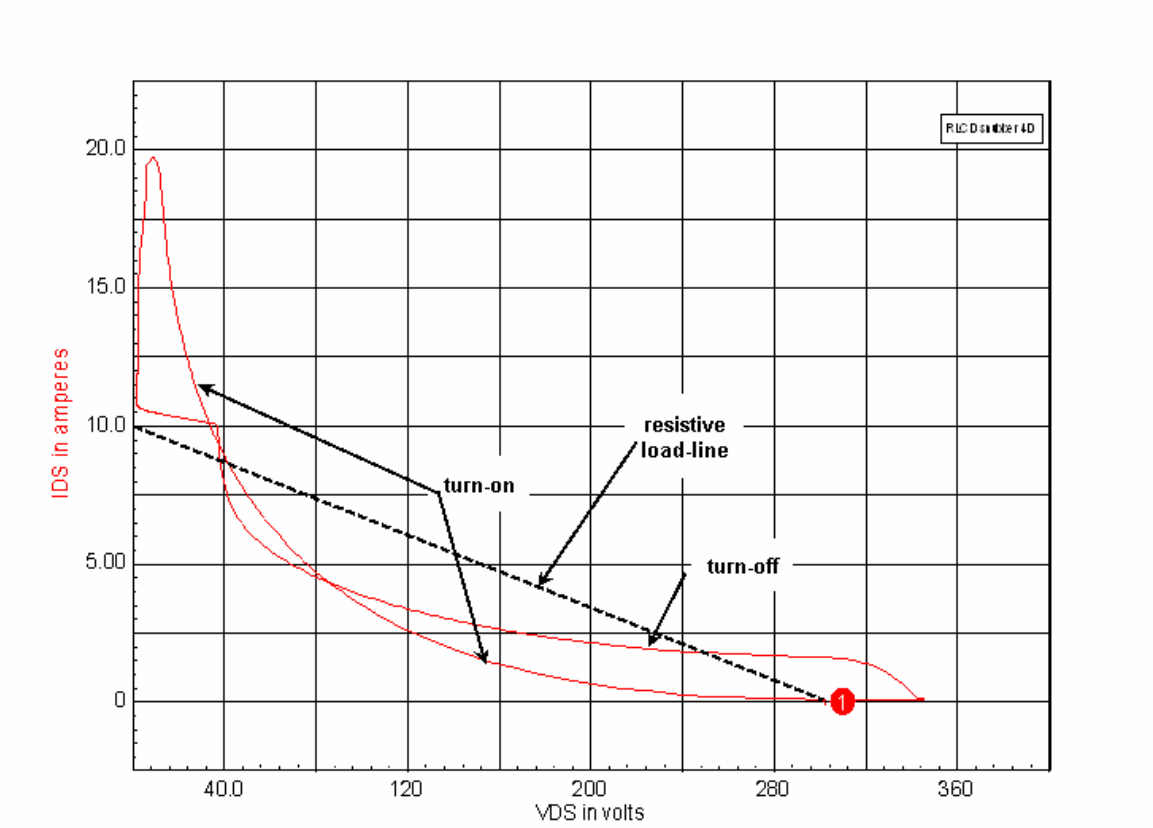


Figure 4-44, load-line for the combined snubber in figure 4-42.

A simplified combination snubber

In practice the snubbers shown in figures 4-40 and 4-42 are not commonly used. By far the most common version of the combination snubber uses only one resistor and one diode as shown in figure 4-45. This version of a combination snubber uses one less diode and one less resistor. That's all well and good, however, as we will see shortly the problem with this is that we can no longer optimize the

turn-on and turn-off behavior of the snubber independently by varying Rs1 and Rs2.

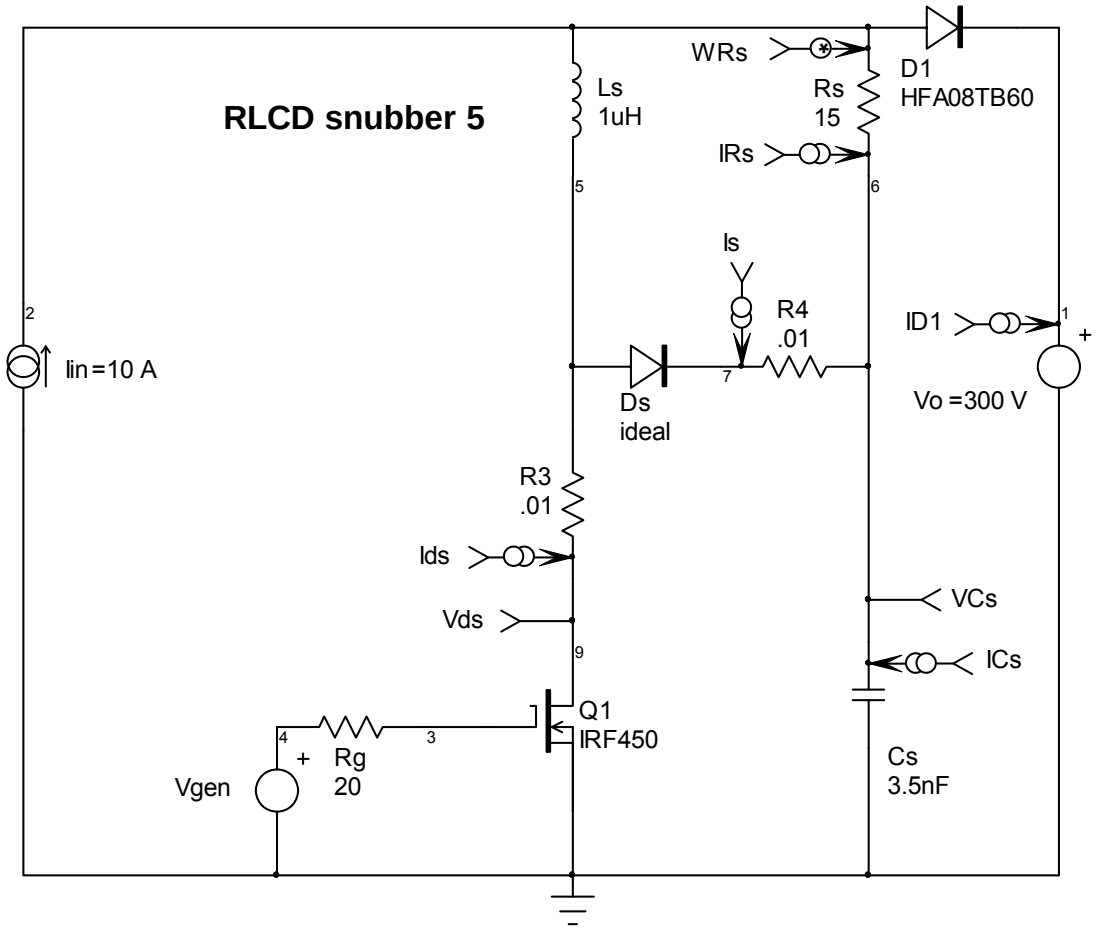


Figure 4-45, Combination snubber using only one resistor (Rs) and one diode (Ds).

Waveforms associated with the circuit in figure 4-45 are shown in figure 4-46.

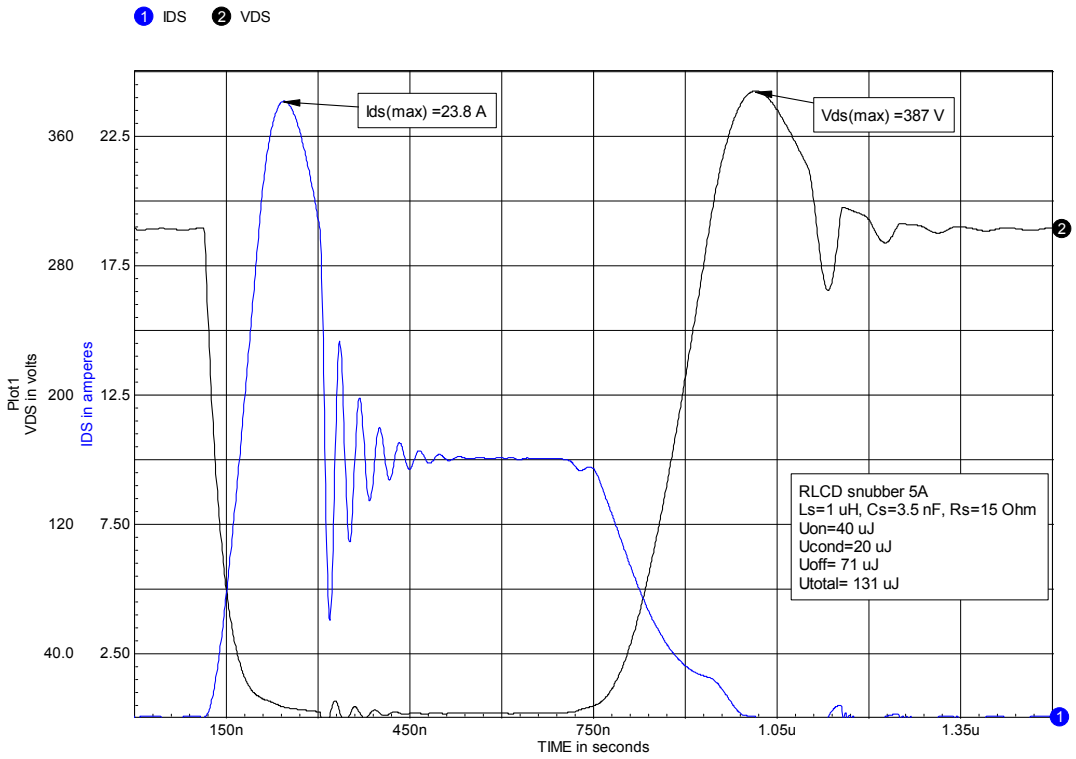


Figure 4-46, Ids and Vds waveforms for the circuit in figure 4-45.

The waveforms in figure 4-46 are significantly different from those in figure 4-43 and in general, less desirable. Both peak Ids at turn-on and peak Vds at turn-off are higher, Utotal is higher and there is a great deal of ringing on both the waveforms. In addition there are some discontinuities in the ringing due to Ds going into and out of conduction. We need to take a closer look at what's going on and see what can be done to improve things.

We can begin by varying the value of Rs: 5, 15 and 30 Ohms for example. The effect on the Ids turn-on waveform is shown in figure 4-47 and the effect on the Vds turn-off waveform is shown in figure 4-48. As can be seen in the figures, increasing the value of Rs improves the Ids turn-on waveform but has the opposite effect on the Vds turn-off waveform. You can chose to damp one waveform but at the expense of have less damping on the other. That is the problem with this snubber circuit. It uses one less diode and one less resistor but you cannot optimize the turn-on and turn-off waveforms independently.

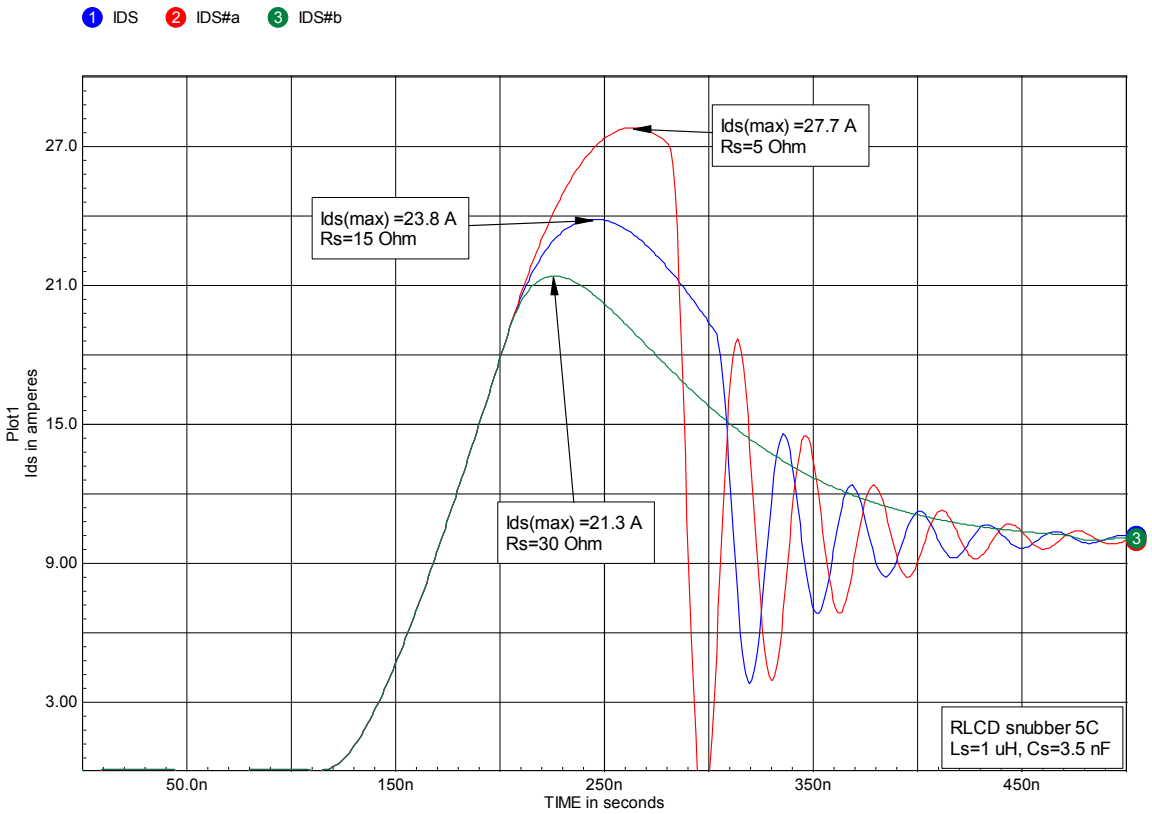


Figure 4-47, Ids turn-on waveforms for Rs = 5, 15 and 30 Ohms.

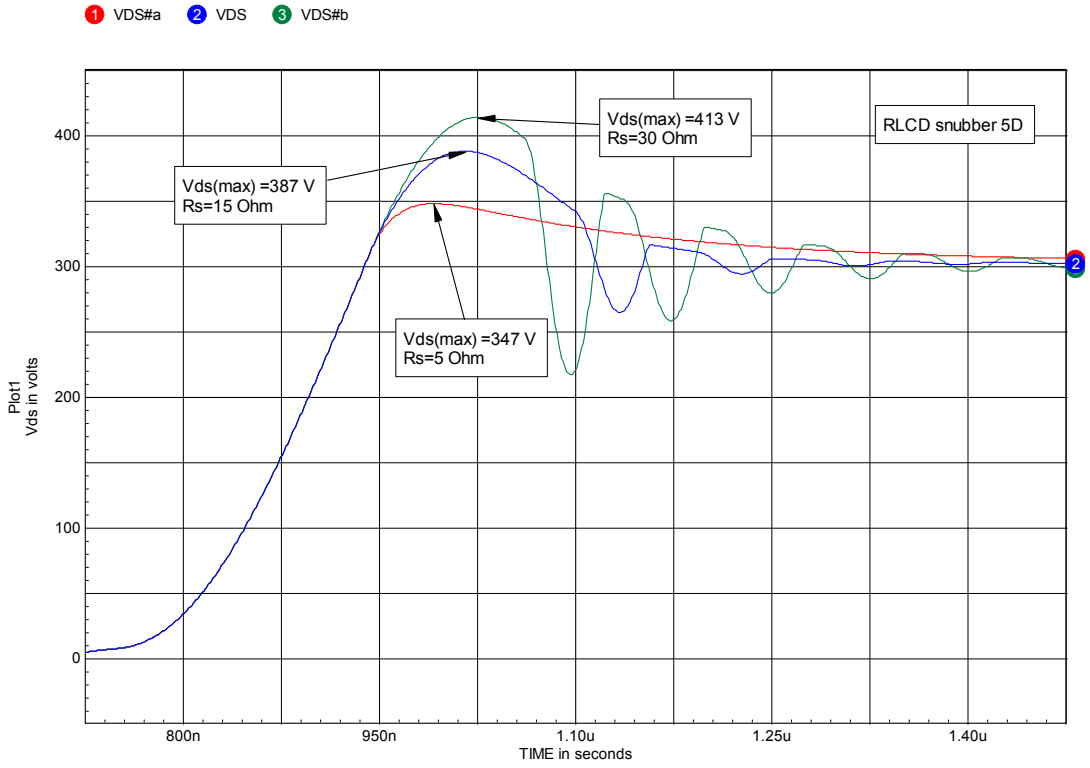


Figure 4-48, Vds waveforms at turn-off for Rs = 5, 15 and 30 Ohms.

Waveform discontinuities

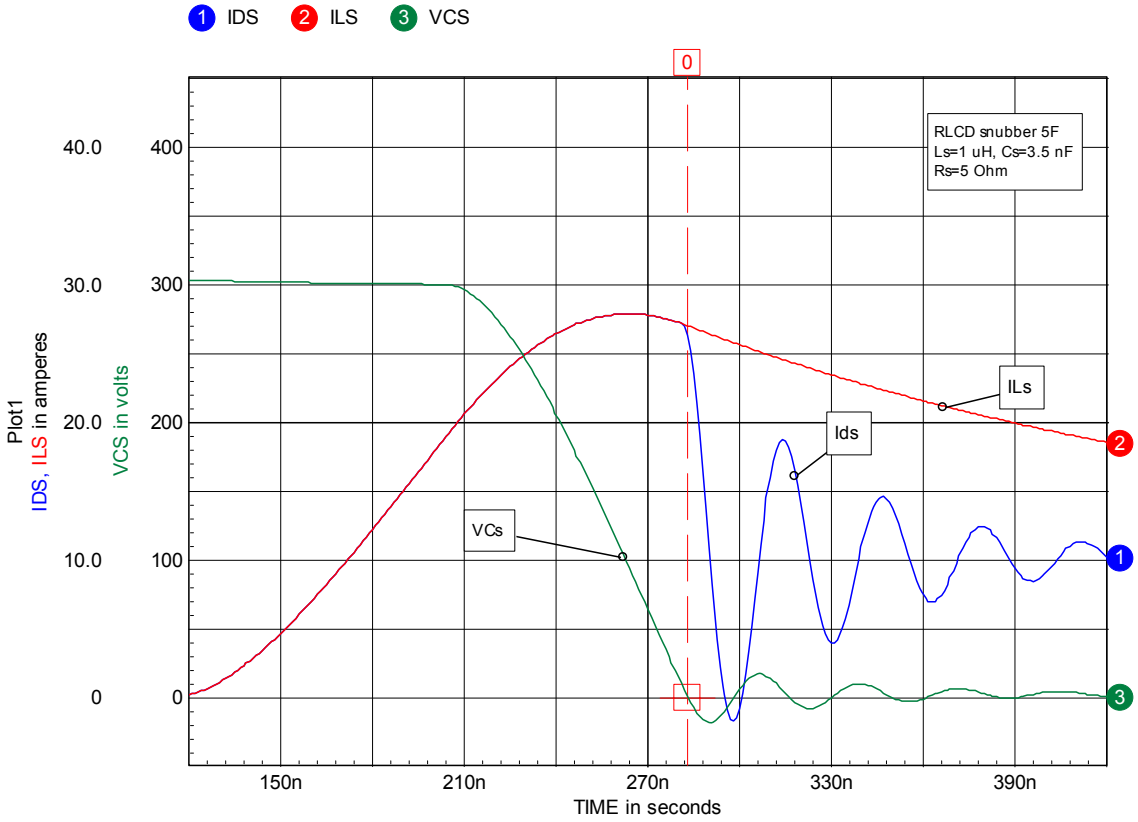


Figure 4-49, Ids, ILs and VCs at Q1 turn-on.

It may be helpful to understand the discontinuities in the waveforms. Figure 4-49 shows the waveforms for the current in Ls (ILs), the voltage across Cs (VCs) and Ids at Q1 turn-on. The discontinuity in Ids occurs at the point in time where VCs = 0. This relationship is emphasized by the dashed vertical red line. That is also the point where Ds starts conducting and Cs is connected to the drain of Q1. The ringing in Ids is due to the presence of approximately 8 nH of drain-source package inductance in Q1. The ringing frequency is determined by the resonance of the package inductance with Cs. As Rs is made larger, the decay of VCs is slowed and the decay of ILs is speeded up so that the conduction of Ds occurs later and at a lower value for ILs. Besides the packaging inductance of Q1, in an actual circuit you would have some layout inductance associated the loop formed by Q1-Ds-Cs. In addition there will be package inductance in Ds and some equivalent series inductance (ESL) in Cs. All of these will contribute to the ringing.

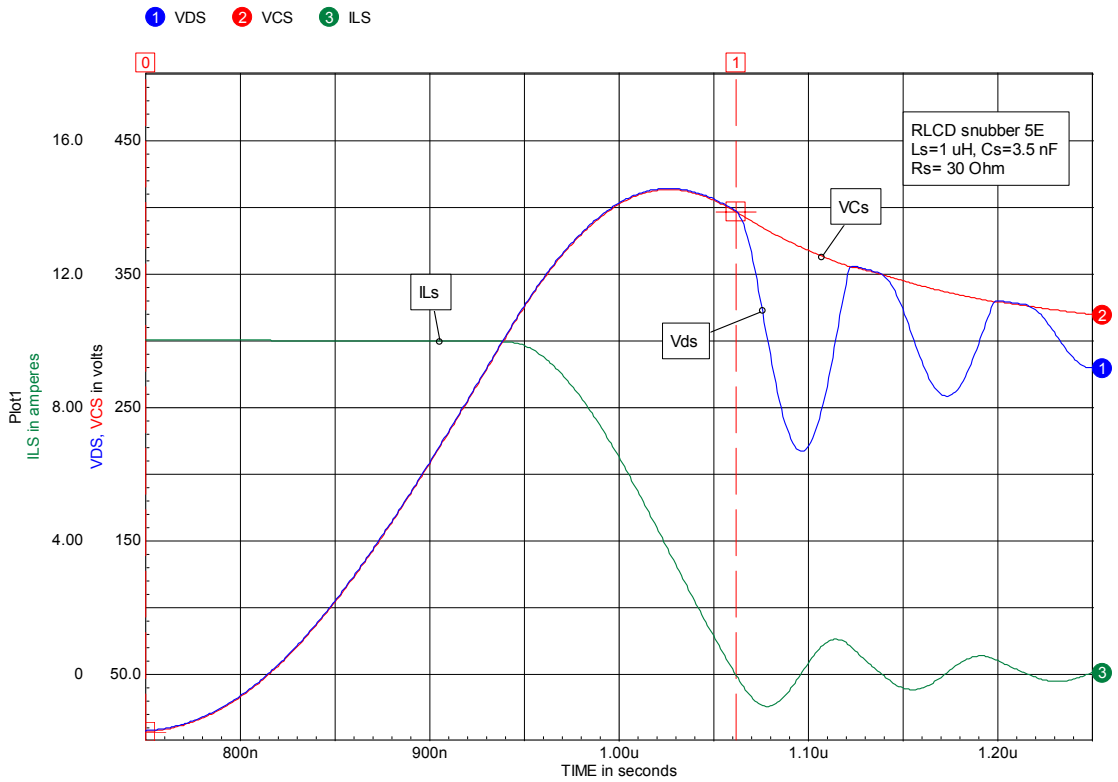


Figure 4-50, Vds, VCs and ILs at Q1 turn-off.

Figure 4-50 shows the waveforms for ILs, VCs and Vds at Q1 turn-off. The first discontinuity in Vds occurs at the point where ILs=0. At this point Ds stops conducting. The ringing is due to the resonance of Ls and the output capacitance (Coss) of Q1. The current ringing is large enough that Ds goes back into conduction and then out of conduction at several later points as indicated by the additional Vds waveform discontinuities.

There is a way to dampen the turn-on Ids ringing. In figure 4-45 there is a metering resistor (R4) in series with Ds. It's value is only 0.01 Ohm. If we increase R4 to 2 Ohms (which is equivalent to adding a series 2 Ohm resistor in the actual circuit) then the Ids waveform at Q1 turn-on will be damped as shown in figure 4-51.

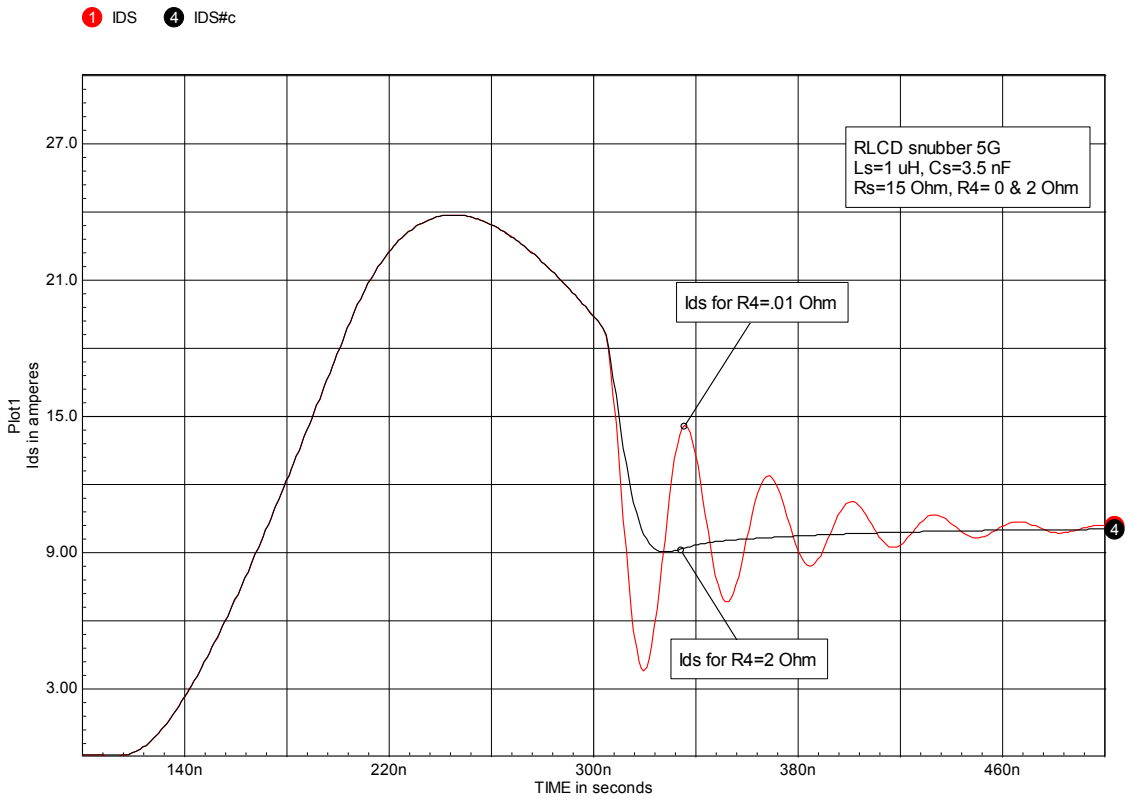


Figure 4-51, Damping of Ids ringing at Q1 turn-on with R4= 0.01 and 2 Ohms.

The Vds waveform at Q1 turn-off is only very slightly changed by adding resistance in series with Ds. Of course we are now back to two snubber resistors but we still have only one snubber diode. However, we still cannot separately optimize the peak Ids at turn-on and the peak Vds at turn-off.

> *In practice the disadvantage of having one additional diode is usually more than offset by the advantages of being able to independently optimize the turn-on and turn-off waveforms as can be done with the snubber circuit in figure 4-42.*

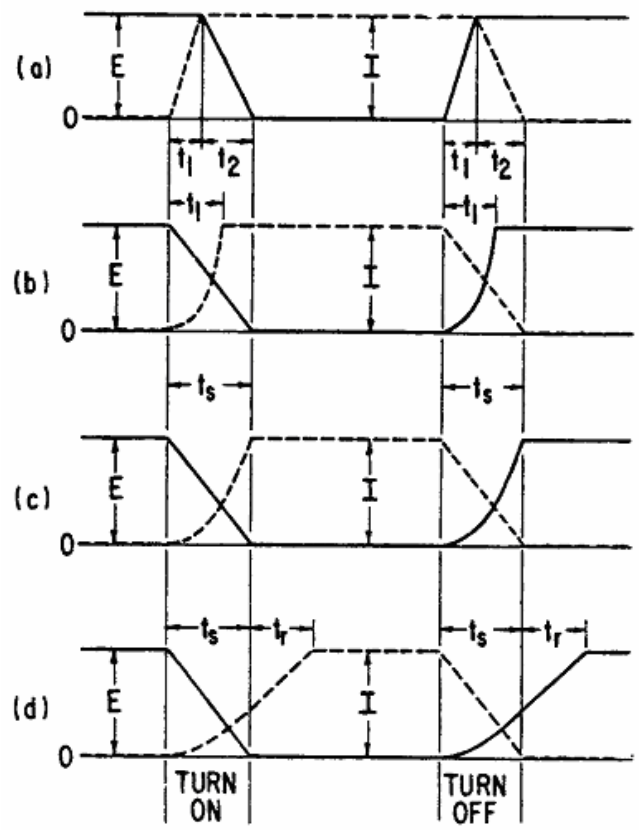
Choosing the initial snubber component values

Up to this point we have been discussing how these snubbers operate and their effect on circuit waveforms and switch losses. Although the values used in the examples seem to work quite well we

haven't seen where they came from. Now it's time to see how to make the initial choices for snubber component values. Keep in mind that these choices, as in the case of the RC snubber, are a reasonable first guess, the final values may have to be adjusted in the actual circuit.

McMurray's 1979 PESC paper[290] has an excellent discussion of the RCL-diode family of snubbers. This paper is highly recommended reading but for now we will just use one of his figures and some of his equations to explain the choice of component initial values.

Figure 4-52 shows how the switch waveforms (idealized) vary with the size of Ls and Cs. Figure 4-52a represents the switch waveforms before adding a snubber.



Voltage (solid lines) and current (dashed lines) waveforms for transistor switching inductive load
(a) no snubbers
(b) small snubbers
(c) "normal" snubbers
(d) large snubbers

Figure 4-52, Idealized Q1 waveforms from McMurray[290], figure 6.

Progressing from (a) to (d) Ls and Cs are made progressively larger and the switching stress on Q1 is reduced. Case (c) is referred to as a "normal" snubber (Cn). In (c), at turn-on, Vds just reaches it's

minimum value when Ids reaches it's maximum. At turn-off, Ids reaches zero at the same time that Vds reaches it's maximum.

Normal snubbers are defined by:

$$Ln = \frac{Et_s}{2I}, \quad i = I \ when \ t = t_s$$

$$Cn = \frac{It_s}{2E}, \quad e = E \ when \ t = t_s$$

$$t_s = t_1 + t_2$$

t_1, t_2 and t_s are defined in figure 4-52a, the un-snubbed case.

Now, let's apply these equations to our original un-snubbed circuit in figure 4-2. To make the calculation easier we will expand the un-snubbed waveforms as shown in figures 4-53 and 4-54.

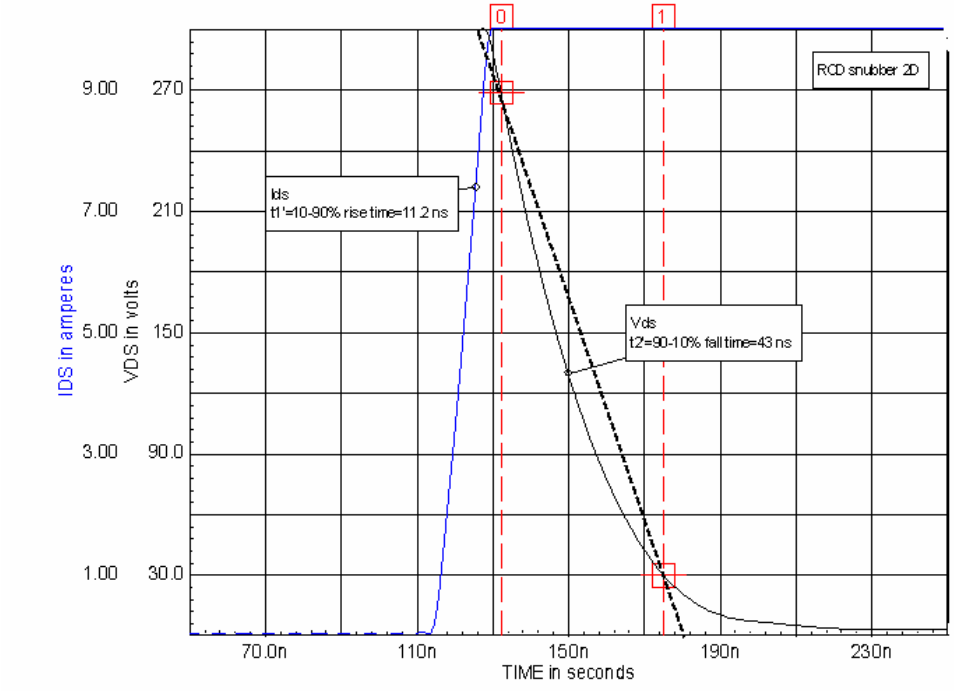


Figure 4-53, turn-on waveforms for Vds and Ids in a converter with no snubber.

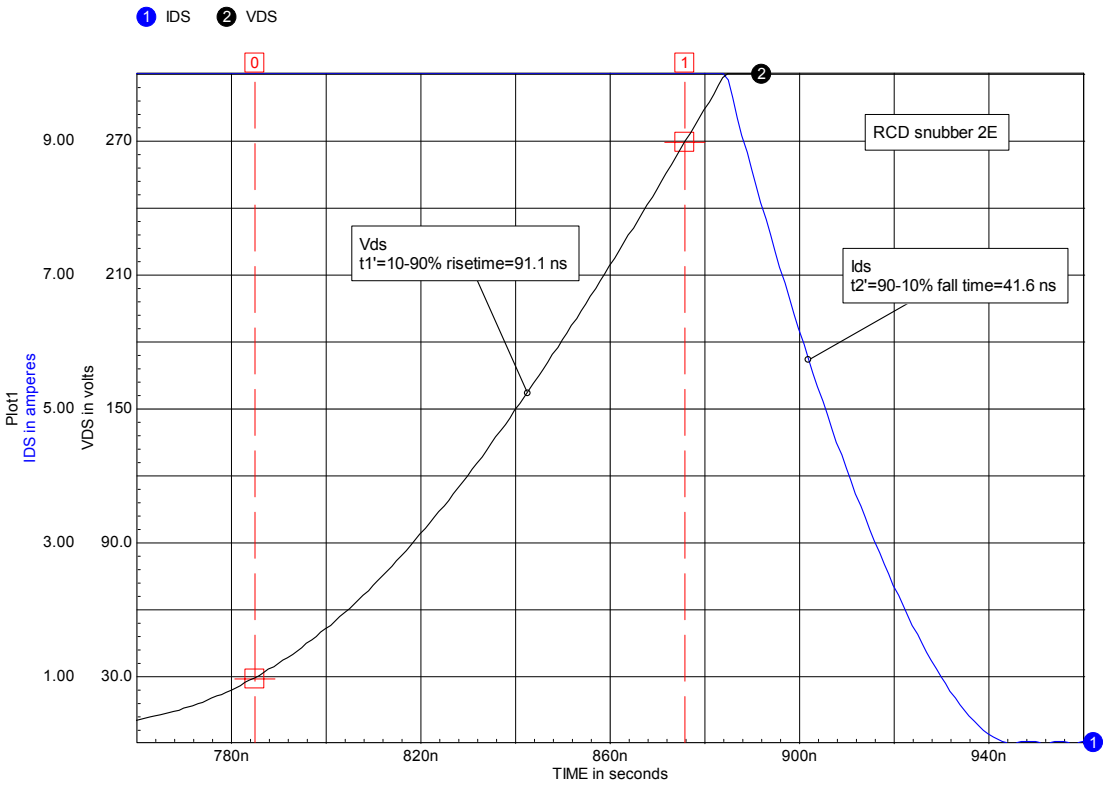


Figure 4-54, turn-off waveforms for Vds and Ids in a converter with no snubber.

Obviously these waveforms do not have the exactly the same shape as the waveforms shown in figure 4-52a. That's ok, McMurray has suggested an approximation: draw a straight line through the 10% and 90% points on the waveforms and use the difference in time between the maximum and minimum intercept points for either t_1 or t_2 . We could draw the line as shown but we don't actually need to, instead we can simply take the time difference between the 10% and 90% points (t_1' and t_2') and divide by 0.8. This gives the straight line approximation value for t_1. Most SPICE modeling programs will calculate the 10-90% transition times (t_1' and t_2') for you or you can do it on an oscilloscope with the actual circuit.

From the waveform times in figure 4-53 we can calculate the value for L_n:

$$t_1' = 11.2ns \Rightarrow t_1 = 14ns$$

$$t_2' = 43ns \Rightarrow t_2 = 53.8ns$$

$$t_s = t_1 + t_2 = 67.8ns$$

$$L_n = \frac{Et_s}{2I} = \frac{(300)(.0678)}{2(10)}\mu H = 1.02\mu H$$

The resulting waveform with Ls = 1 uH is shown in figure 4-55.

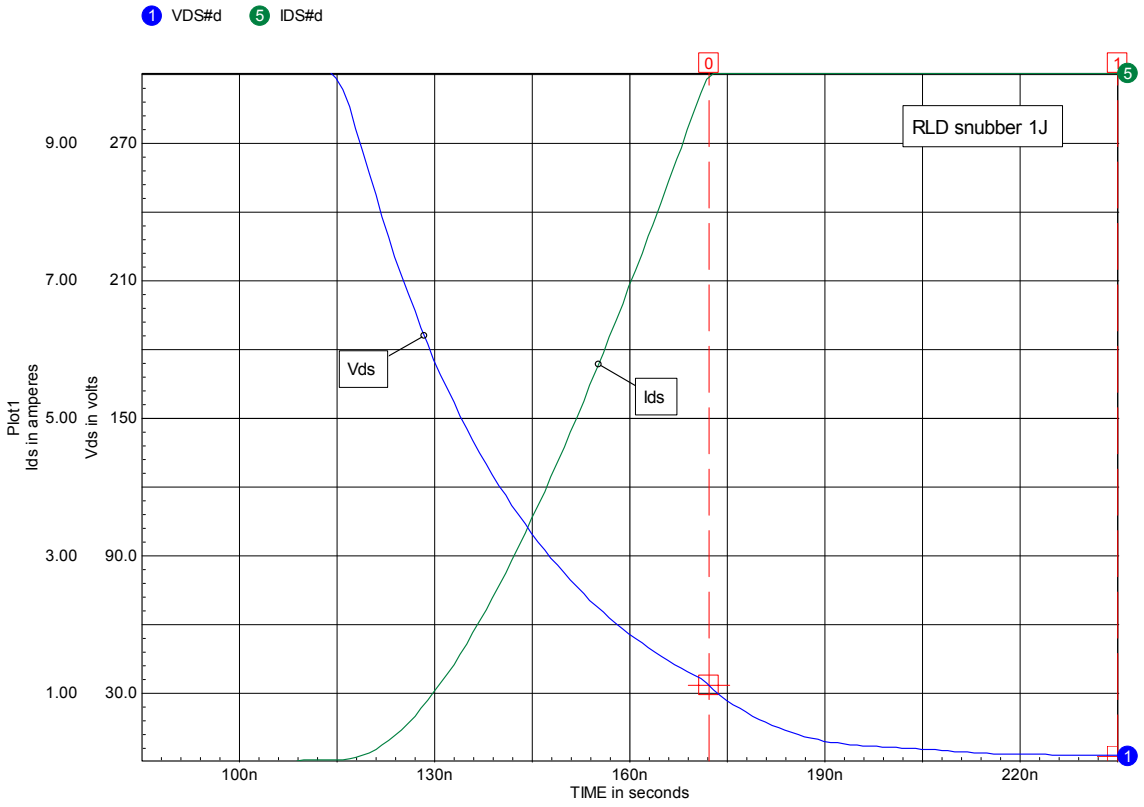


Figure 4-55, snubbed turn-on waveform, Ls = 1 uH.

As the cursor shows, at the time that Ids reaches its maximum, Vds is not quite down to its minimum. The calculation does give a good approximation however, and Ls could now be made a bit larger if heavier snubbing is desired.

We can now repeat this exercise for figure 4-54 and determine the value for Cn.

$$t_1^{'} = 91.1ns \Rightarrow t_1 = 113.9ns$$

$$t_2^{'} = 41.6ns \Rightarrow t_2 = 52ns$$

$$t_s = t_1 + t_2 = 165.9ns$$

$$C_n = \frac{It_s}{2E} = \frac{(10)(.0678)}{2(300)} nF = 2.76nF$$

The resulting waveform using this value for Cs is shown in figure 4-56.

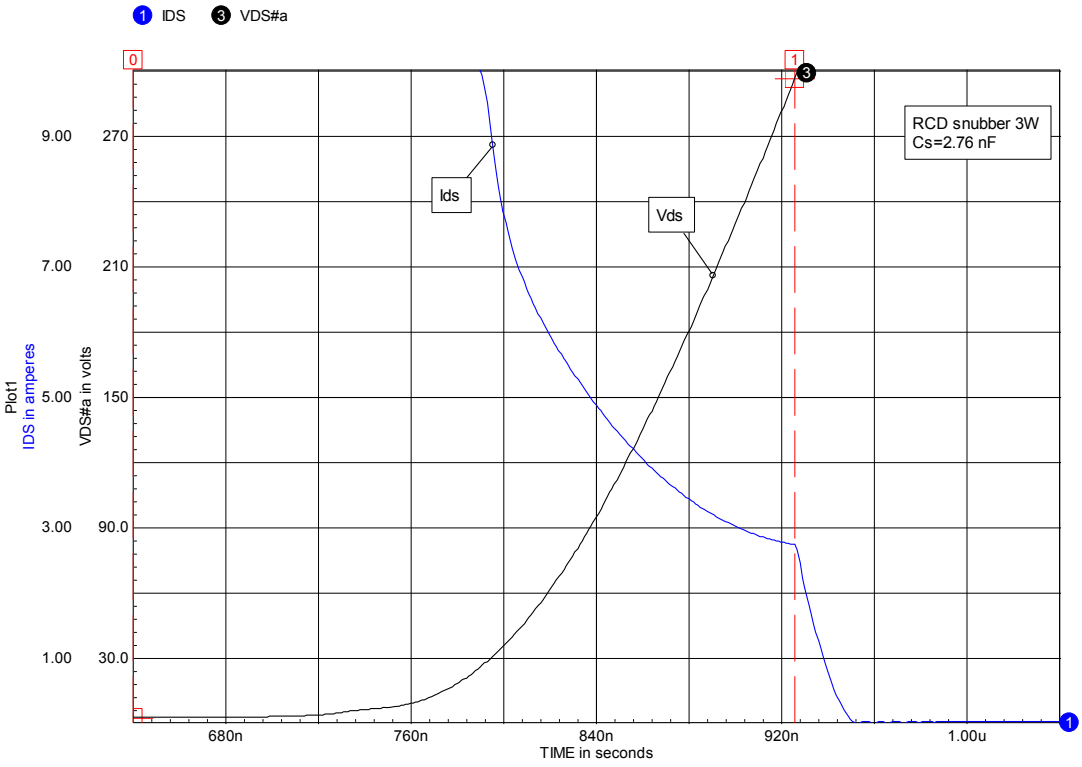


Figure 4-56, snubbed turn-of waveform, Cs = 2.76 nF.

For this value of Cs, Ids does not quite reach zero when Vds reaches it maximum (300 V). Again McMurray's equations give an

approximation which is a reasonable starting point. If heavier snubbing is desired then Cs can be increased.

As pointed out earlier, the values chosen for the discharge resistors (Rs, Rs1, Rs2, etc) are determined by the minimum times available for discharge of Ls and/or Cs. It is not necessary to completely discharge either Ls or Cs but normal practice is to allow the RsCs or Ls/Rs time constants to be 1/3 or less of the minimum available discharge time. 1/5 is usually used if there is sufficient time.

In the case of Cs, the tradeoff between full and partial discharge is to limit the peak discharge current at turn-on by using a larger value for Rs, which reduces the turn-on loss, versus some increased loss at turn-off. In the case of Ls, the value of Rs determines the turn-off Vds peaking. Making Rs smaller reduces the voltage peak at turn-off and improves the turn-off loss but reduces the discharge of Ls so that there is some increase in loss at turn-on. In either of these cases it may well be that using a larger (for Cs) or smaller (for Ls) value of Rs may result in a net reduction in switching loss.

The minimum discharge times occur at the extremes of switch duty cycle (i.e. maximum or minimum on-time). It may be to your advantage to accept less than full discharge of the snubber energy storage elements at these points if, in exchange, the overall circuit efficiency is improved at more nominal operating duty cycles.

Other design considerations

Throughout all the examples given above, Ids was assumed to be the same at turn-on and turn-off. That was done to make the modeling simpler and had no effect on the explanation of snubber operation. This is an artifact of using a current source on the input in place of a voltage source and a series inductor. However, almost always the inductor current and Ids will change during the on time of Q1. A more typical Ids waveform for Q1 will have a lower value at turn-on (I_a) and a higher value at turn-off (I_b) as shown in figure 4-57. The shape of the current waveform will depend on whether the circuit is operating in the CCM (continuous inductor current) or DCM (discontinuous inductor current) modes. I_a, I_b and the conduction mode will depend on the load current, the switching frequency and the value of the input inductor in the actual circuit.

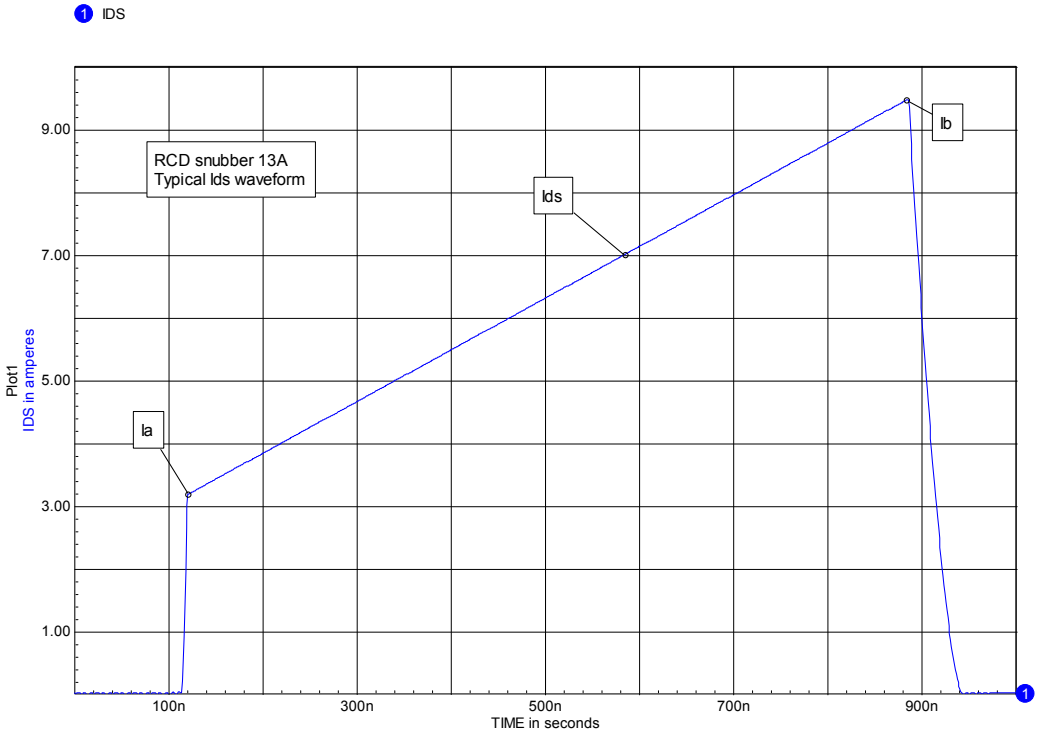


Figure 4-57, typical Ids waveform.

I_a = 0 in DCM.

It is normal for Ids to vary with load, sometimes over a wide range. This change in Ids will have a direct impact on the effect of the snubber on the circuit waveforms as was demonstrated in figure 4-18. This may make it necessary to use a less aggressive snubber at full load to obtain acceptable performance at light loads. It is also very common for source voltages to vary widely, altering the peak values for Vds in many circuits.

Normal variations in Ids waveform shape, input source voltage and output load current, make it necessary to check the behavior of the circuit at a minimum of four points:

Low line and light load	low line and full load
high line and light load	high line and high load

It may be necessary to optimize the circuit performance at any of these points or at some intermediate point.

Snubber interactions

While the examples to this point have all been for a single ended boost converter, the switch action in more complex converters is essentially the same and snubbers find wide application in these circuits. However, some interactions between snubbers associated with different switches can occur and degrade circuit performance.

Converters using half and full-bridge switch connections are very common. A typical example is given in figure 4-58.

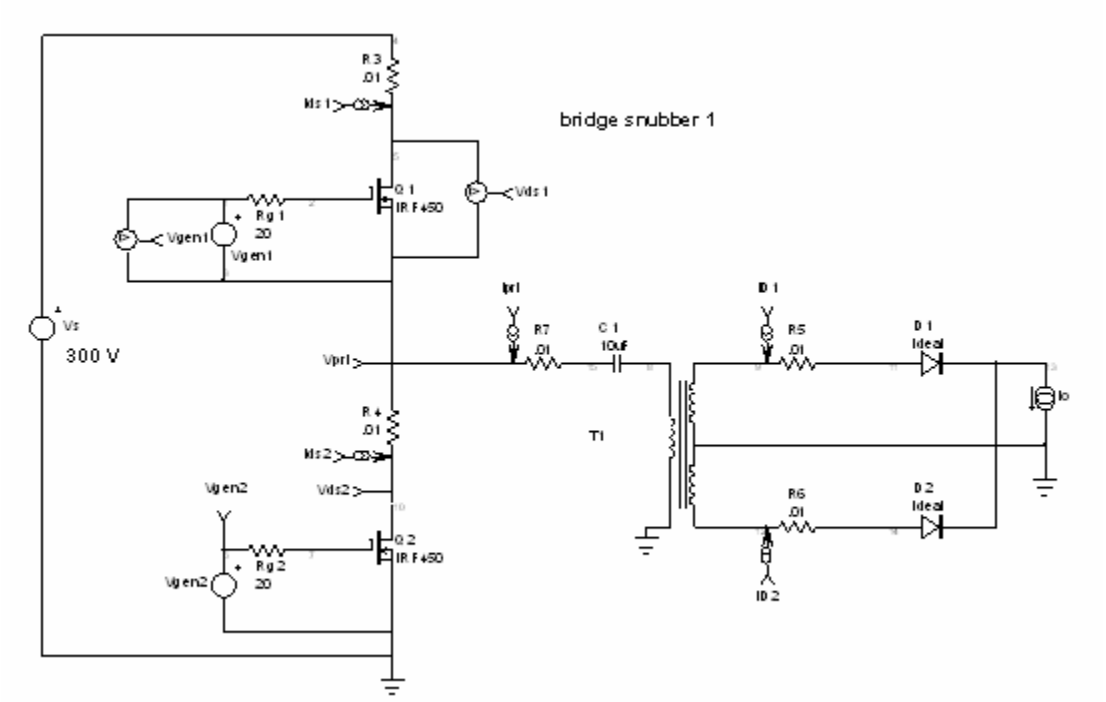


Figure 4-58, a half-bridge quasi-squarewave converter example. T1 turns ratio is 1:1, no snubbers and ideal diodes on the secondary.

For the moment we will let D1 and D2 be ideal diodes. This will allow us to more easily see the interaction when turn-off snubbers are added across Q1 and Q2. Later we will show the effect of using real diodes on the switch waveforms.

Ids and Vds waveforms associated with Q2 (Ids2 & Vds2) are shown in figure 4-59.

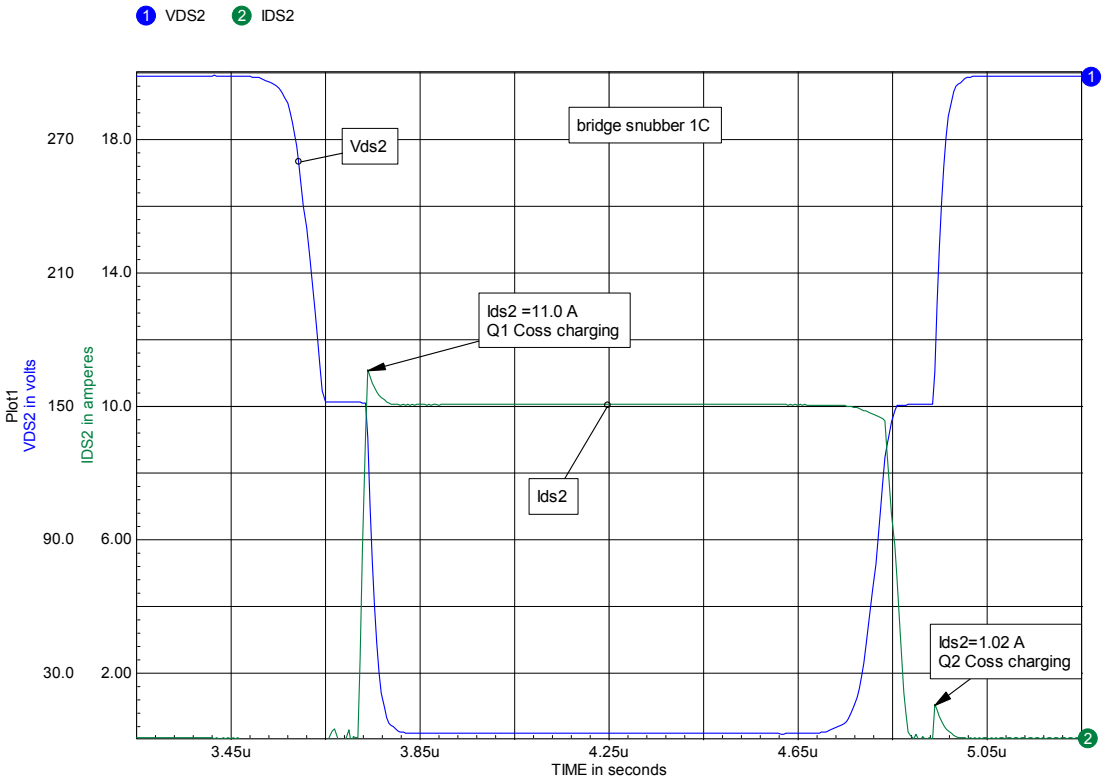


Figure 4-59, Ids2 and Vds2 waveforms for Q2.

The waveforms for Q1 will be the same except shifted by 180 degrees. Note that even though the source voltage (Vs) is 300 V, the Vds transition at turn-on and turn-off is only 150 V. The final off-voltage across a given switch (300 V) is not reached until the complimentary switch turns on. Note also the current spikes associated with charging the off-state switch capacitances. In an actual circuit these current spikes will be larger due to the parasitic capacitances associated with circuit layout, heat sinks, drive circuits, etc.

The load-line associated with the waveforms in figure 4-59 is shown in figure 4-60.

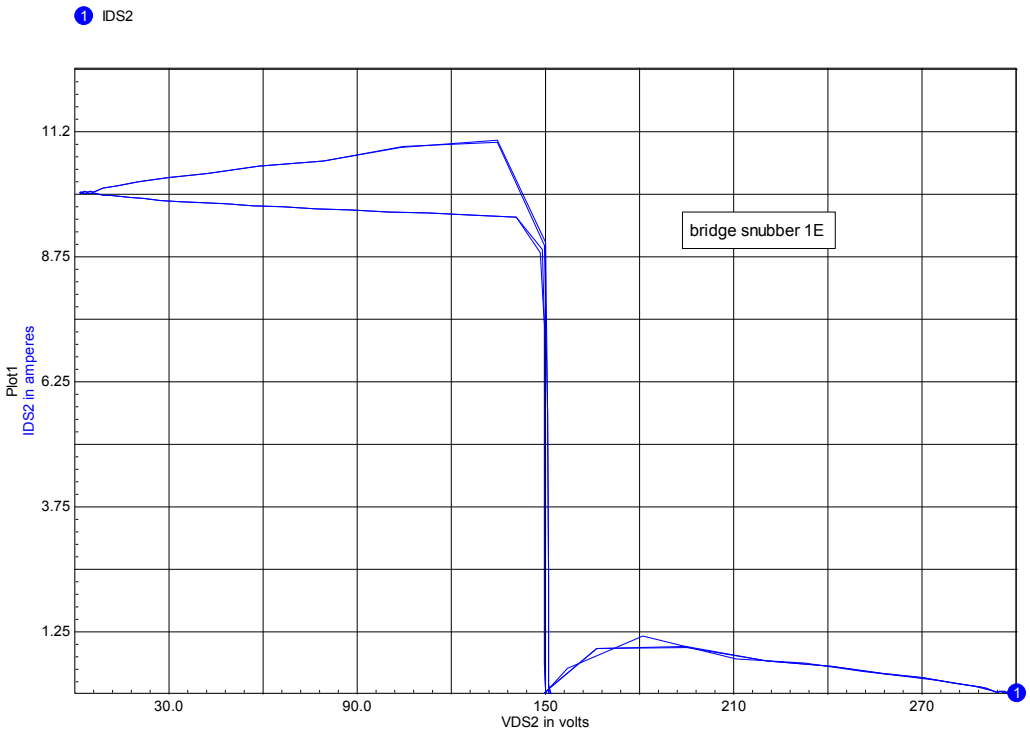


Figure 4-60, half-bridge converter switch load-line.

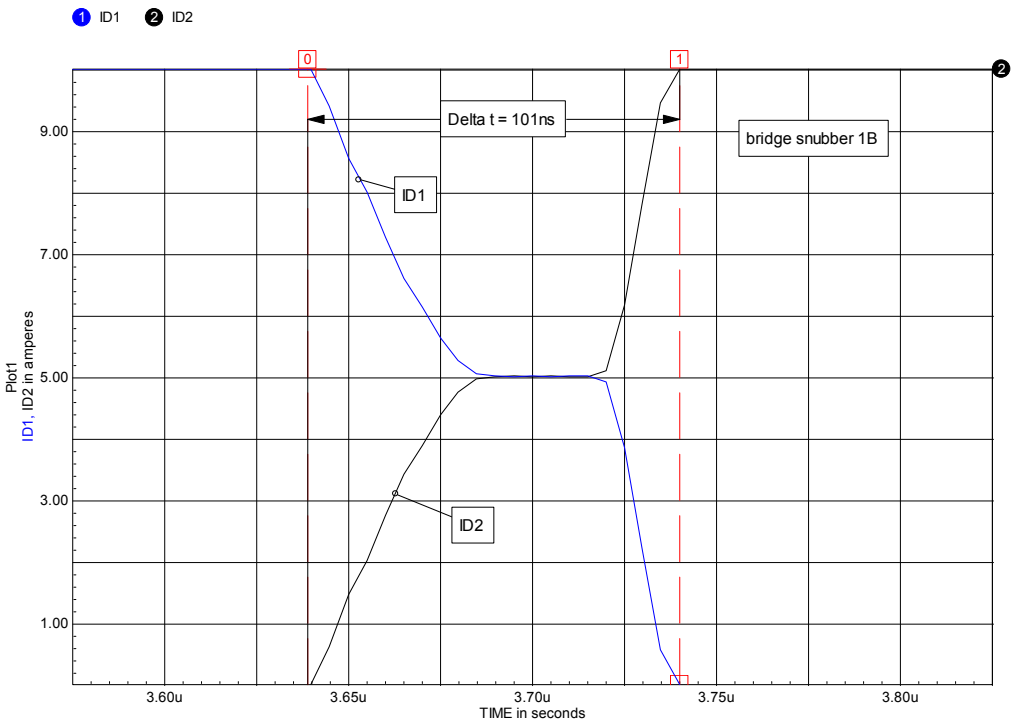


Figure 4-61, ID1 and ID2 during diode current commutation. This corresponds to the 150 V plateau during the switch deadtime.

Now, let's add a pair of turn-off snubbers, one across each switch as shown in figure 4-62.

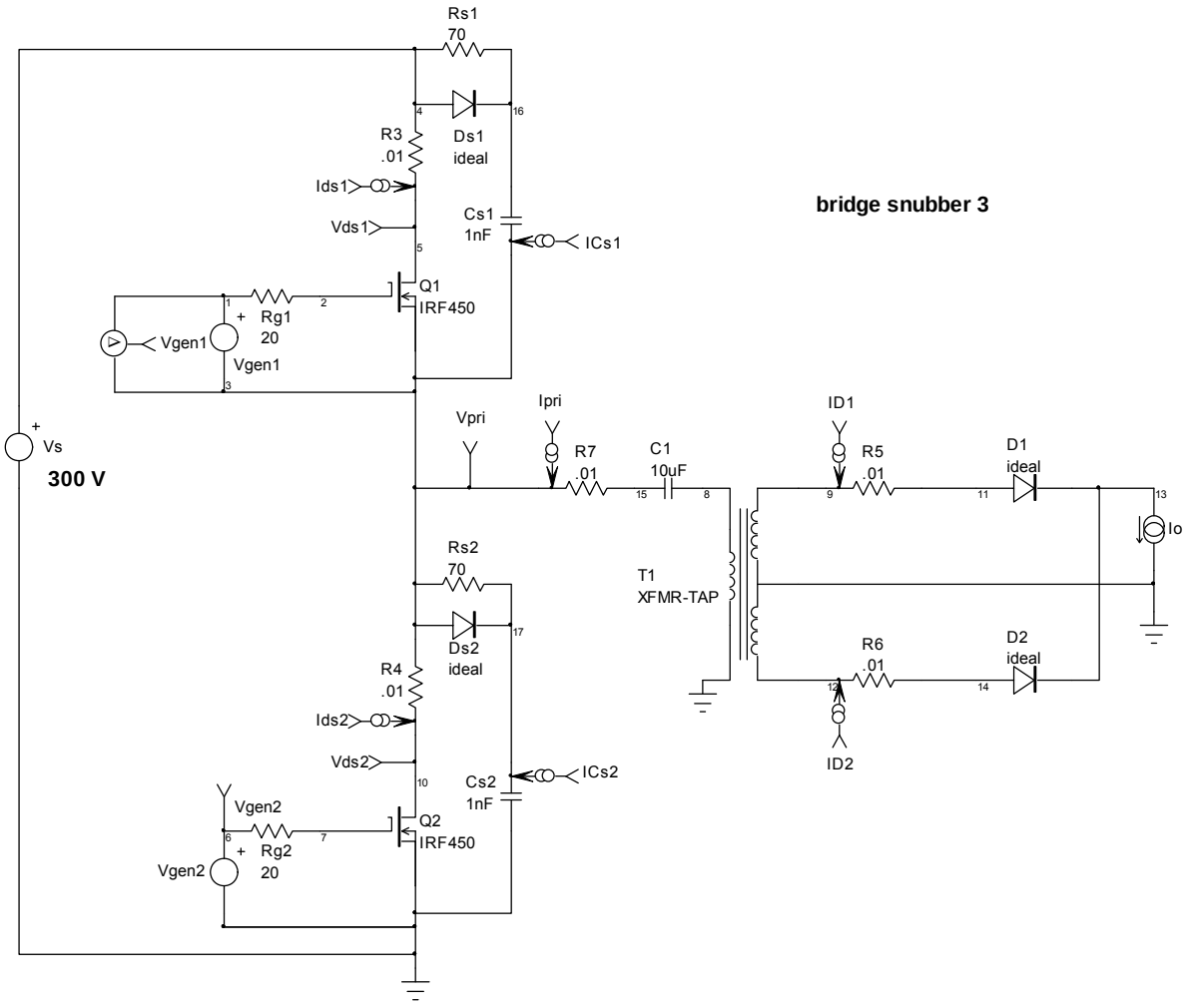


Figure 4-62, quasi-squarewave converter with turn-off snubbers added.

Ids and Vds waveforms for the circuit with the snubbers added are shown in figure 4-63.

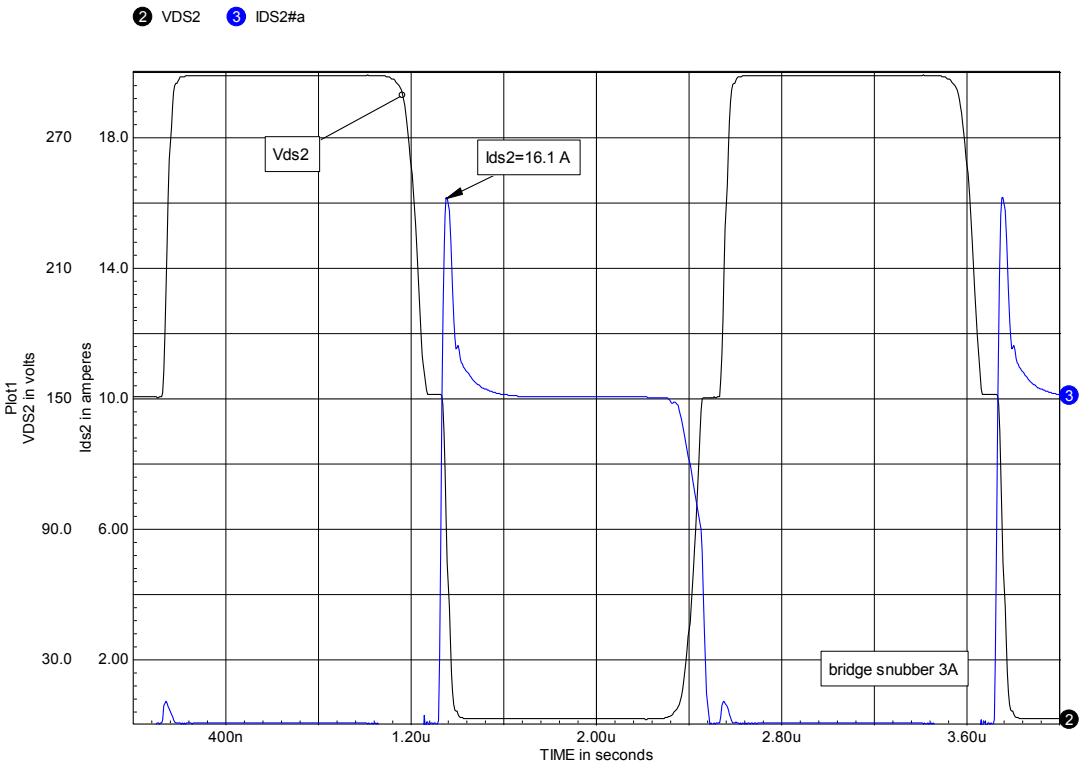


Figure 4-63, Ids and Vds waveforms with turn-off snubbers added to Q1 and Q2.

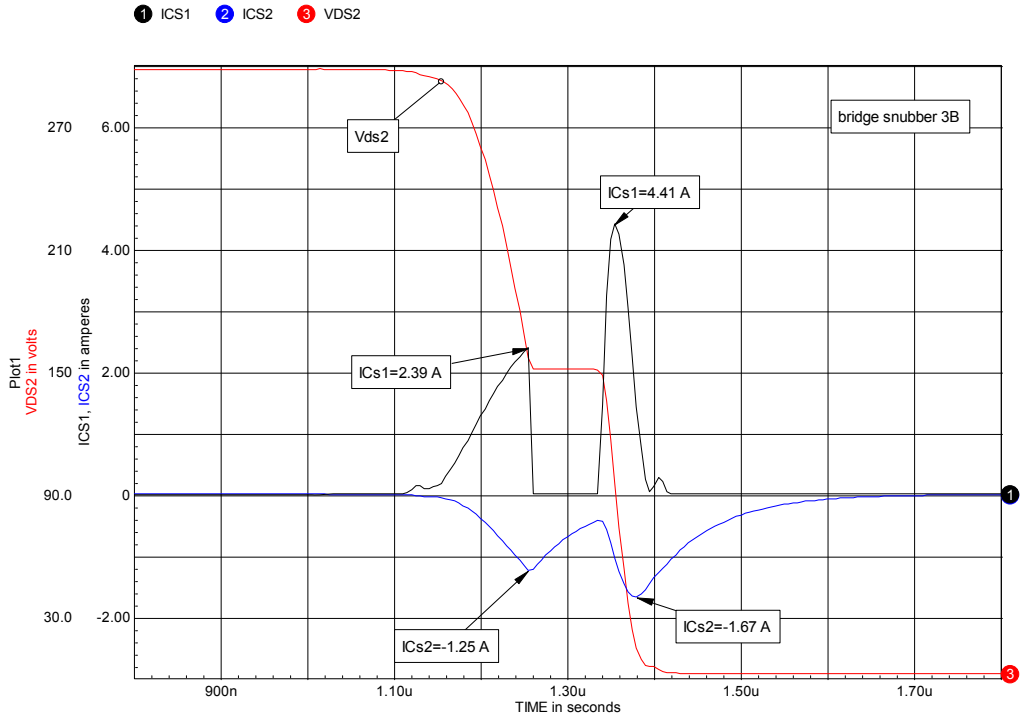


Figure 4-64, Cs1 & Cs2 current waveforms and Vds2 waveform.

There is now a large (6.1 A) current spike on Ids2. Because we are using ideal diodes in the secondary, this current spike can only be due to charging and discharging the snubber capacitors.

The source of this spike needs some explanation. Figure 4-64 shows the current waveforms in Cs1 and Cs2 along with the waveform for Vds2. We can see there are two current pulses on each current waveform corresponding to the two Vds transitions: 300 to 150 and 150 to 0. The first transition corresponds to Q1 turn-off and the second to Q2 turn-on. The villain here is the second current pulse on ICs1 which seems quite large.

Referring to figure 4-62, we see that when Q2 turns on there is a direct path from Vs, through Ds1 and Cs1, to the drain of Q2. The only thing limiting the current amplitude is the rate of change of Vds2 (d(Vds)/dt). The same thing will happen with Ds2-Cs2 when Q1 turns on later in the cycle. This is an example of an undesirable interaction between the two snubbers. Unfortunately this is not the worst of it! Figure 4-65 shows what happens to the Ids2 waveform as we reduce the output load current from 10 A to 1 A, a typical load range.

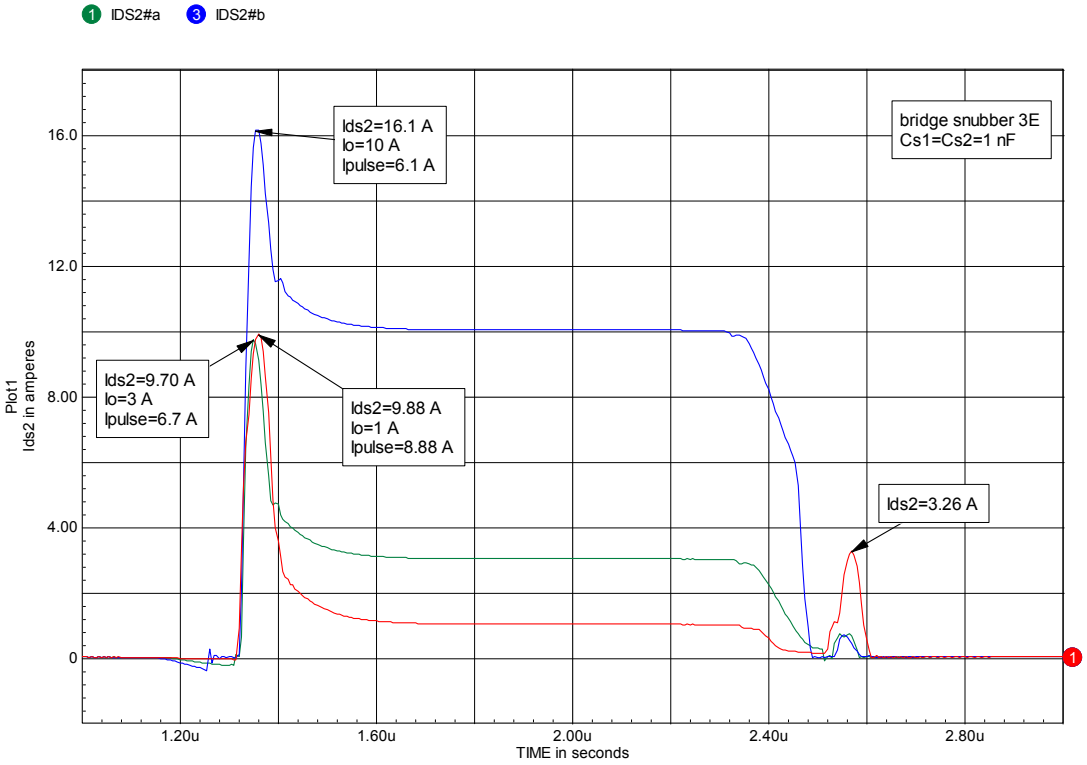


Figure 4-65, Ids2 waveforms as Io is reduced from 10 to 1 A.

To better see what is happing to Ids2 as Io is reduced we can expand the Q2 turn-on portion of the waveforms as shown in figure 4-66.

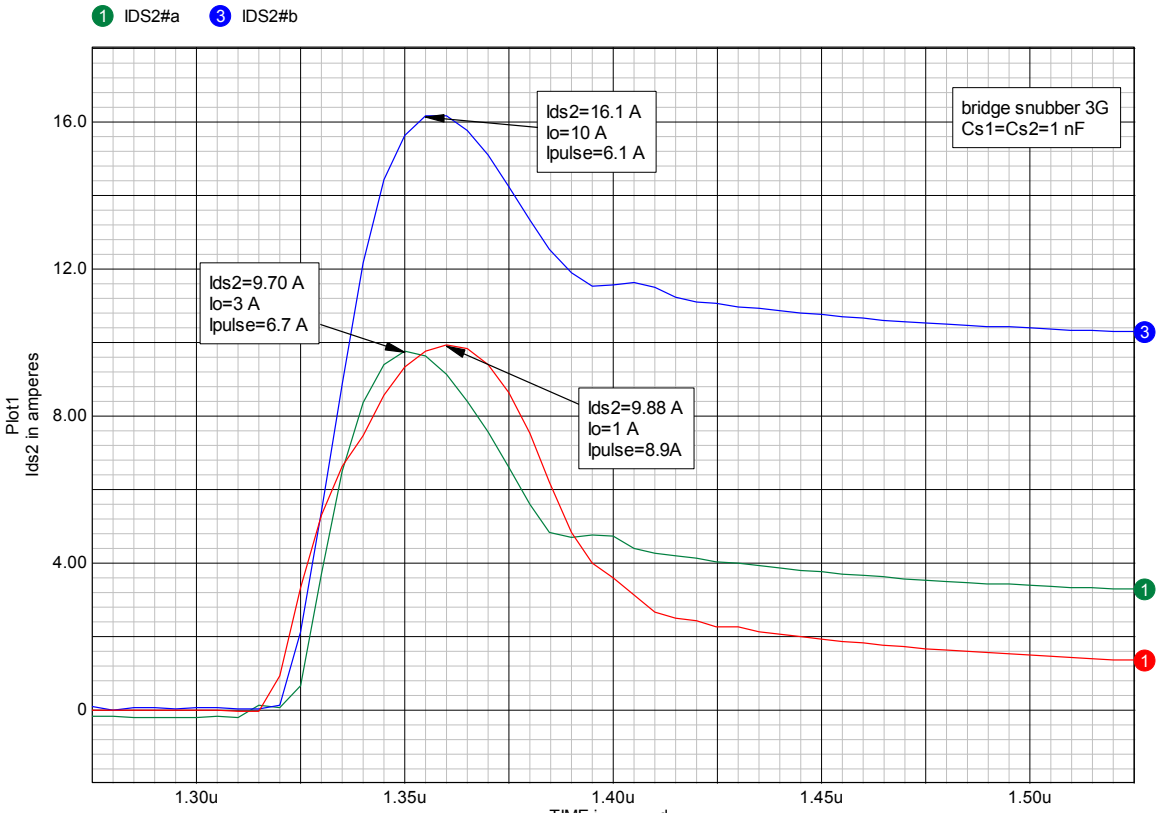


Figure 4-66, Ids2 waveforms at Q2 turn-on for Io=1, 3 and 10 A.

As Io is reduced the current pulse amplitude gets larger, going from 6.1 A when Io=10 A, to 8.9 A when Io=1 A. We also see that when Io=1 A, the Ids2 current pulse at Q1 turn-on jumps up to 3.3 A. The reason for the behavior of the current pulses can be seen by comparing the Vds2 waveforms as we reduce Io.

This comparison is made in figure 4-67. As we reduce Io, the current available to charge and discharge Cs1 and Cs2 is reduced. This means it takes more time for Vds2 to fall from 300 V to 150 V. This can seen by the reduction in the effective deadtime in figure 4-67. In fact when Io is down to 1 A, Vds2 has only declined to 240 V when Q2 turns on. This is where the large current spike comes from at Q2 turn-on. A similar thing is happening at Q1 turn-on. Vds2 has risen only to 60 V when Q1 turns on this leads to the 3.3 A spike in Ids2. The waveforms for Q1 are similar.

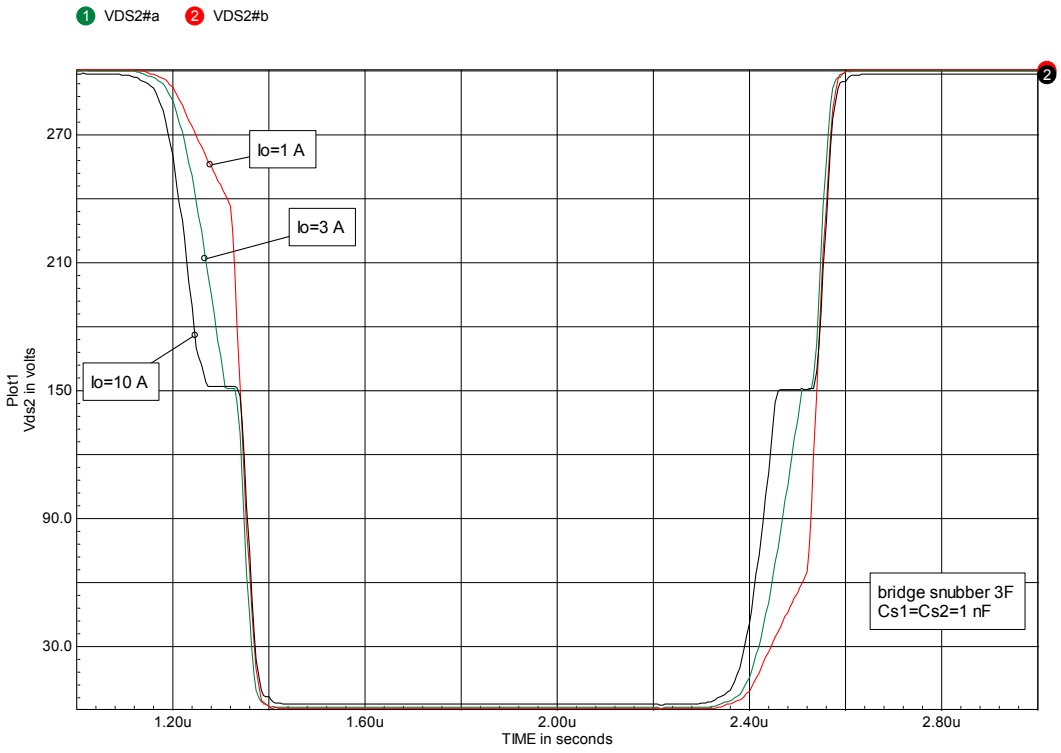


Figure 4-67, Vds2 waveforms as Io is reduced from 10 to 1 A.

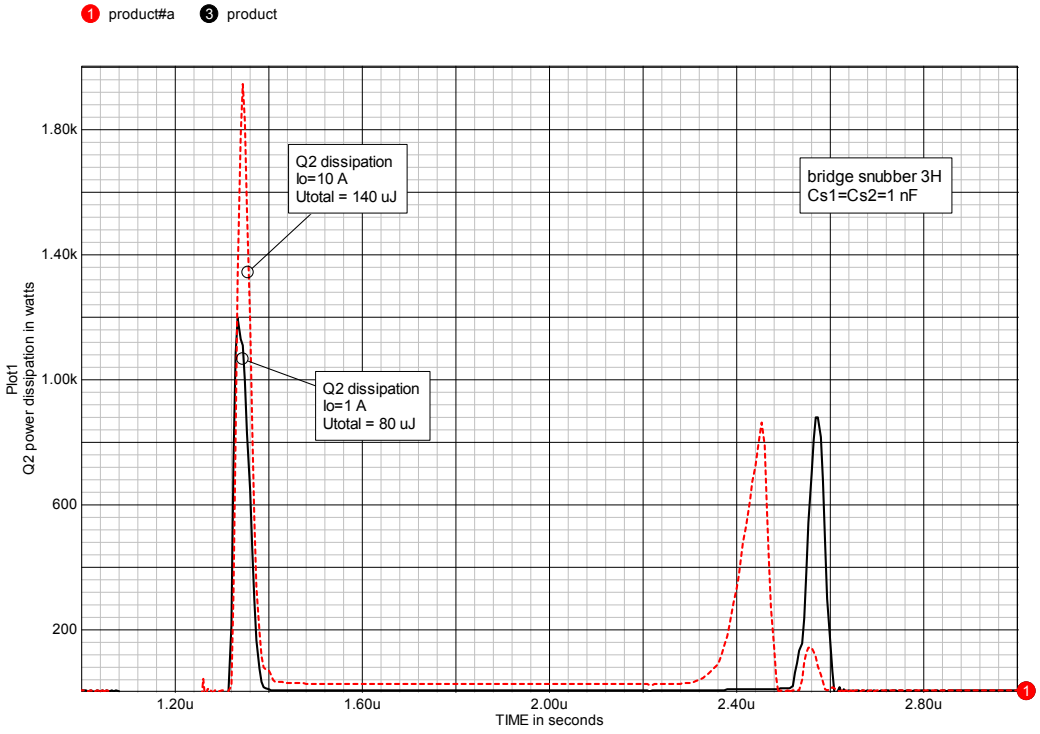


Figure 4-68, power dissipation and total energy loss per cycle for Q2 as Io varies from 1 to 10 A.

Figure 4-68 shows the power dissipation and total power loss per switching cycle (Utotal) as the output load current (Io) is varied from 1 to 10 A. As Io is increased the switching loss also increases as would be expected but it is not proportional to Io. At Io=1 A, Utotal = 80 µJ while at Io=10 A, Utotal = 140 µJ. An increase of less than 2:1 for a load or output power change of 10:1. This means that as Io is reduced the overall converter efficiency will almost certainly decrease substantially due to the switching loss being larger in proportion to the load power.

The effect of a varying load can also be seen in the load-lines for Q2 as we vary Io from 1 to 10 A, as shown in figure 4-69.

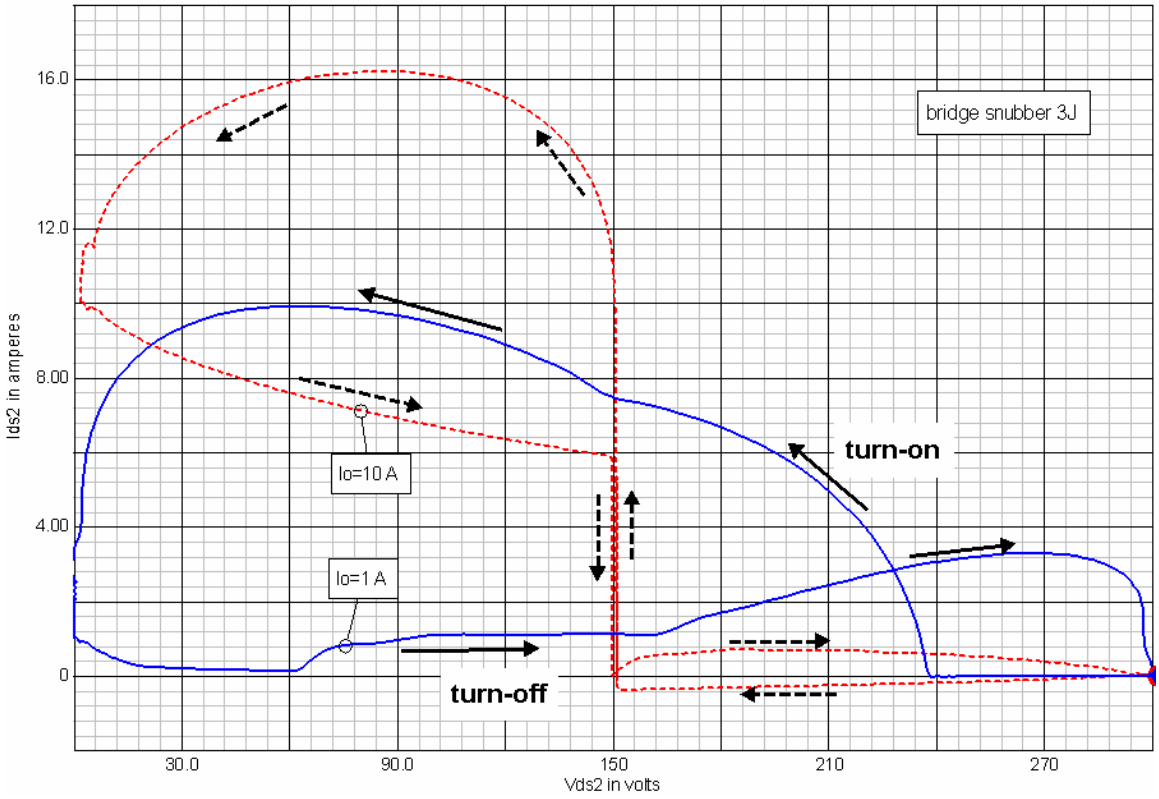


Figure 4-69, Q2 load-lines for Io=1 and 10 A.

This interaction between the two snubbers leads to a substantial increase in switch loss and peak stress which is normally undesirable. The usual solution is to incorporate an inductive turn-on snubber, as shown in figure 4-70, into the circuit. Ls1 and Ls2 are actually one inductor with two tightly coupled windings.

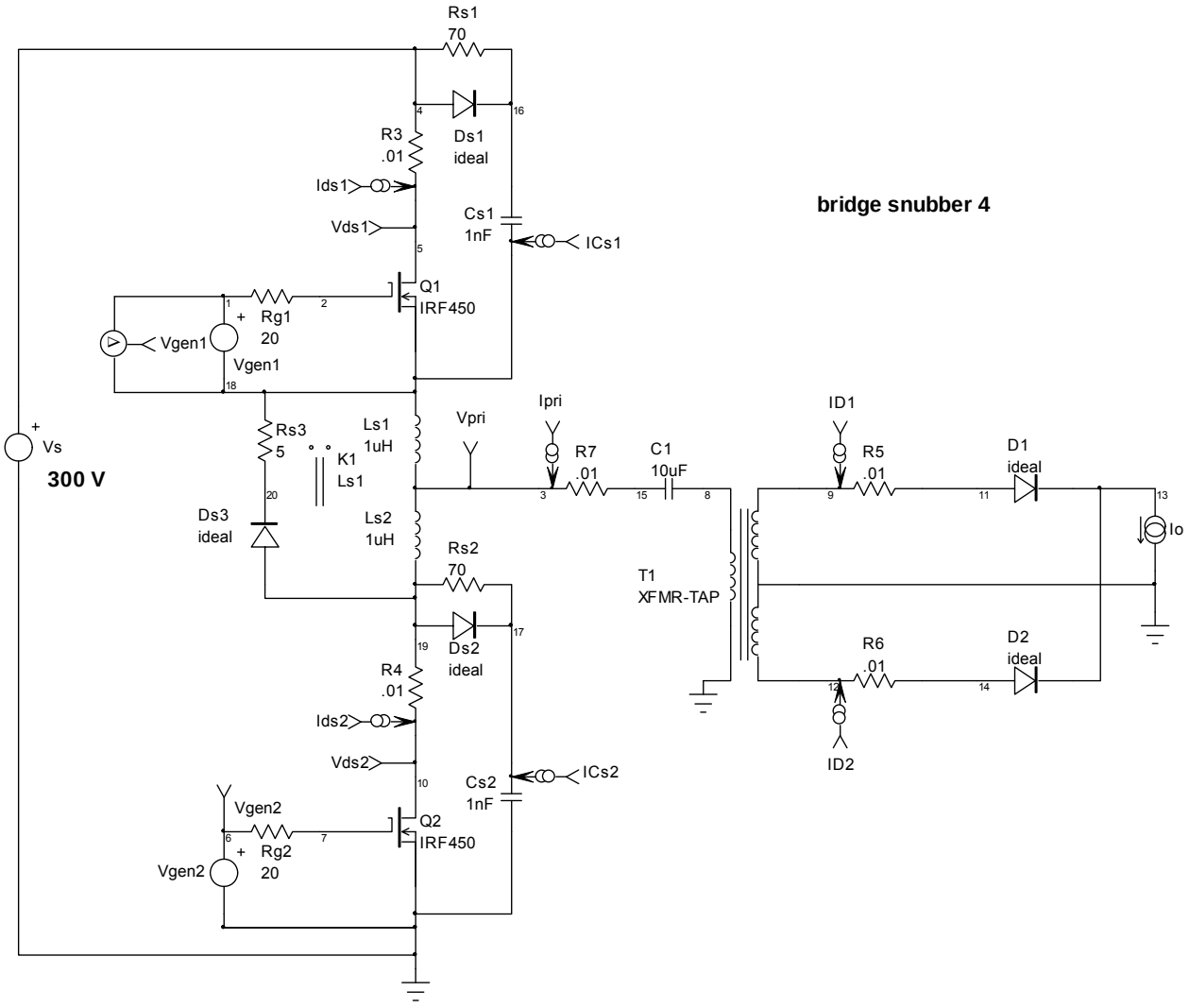


Figure 4-70, adding a two winding snubber inductor.

Ds3 and Rs3 form the discharge network for Ls1-Ls2. Q2 Ids and Vds waveforms with the Ls1-Ls2 snubber in the circuit are shown in figure 4-71 compared to Ids2 without Ls1-Ls2.

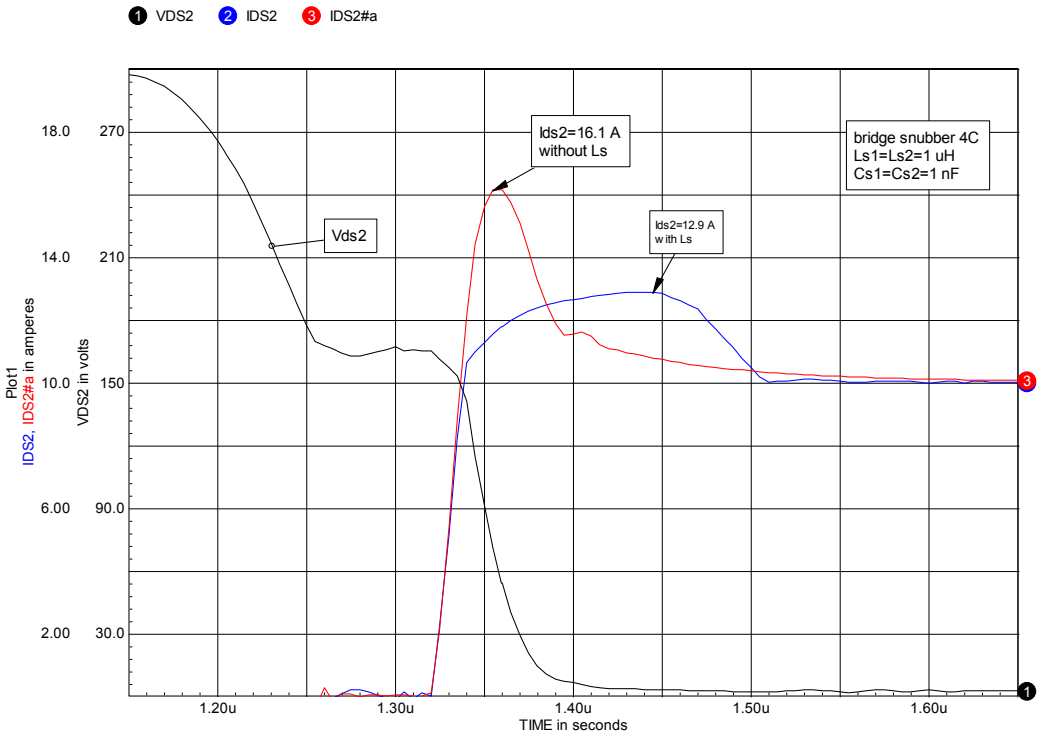


Figure 4-71, Ids2 and Vds2 waveforms with the added inductive snubber and Io=10 A.

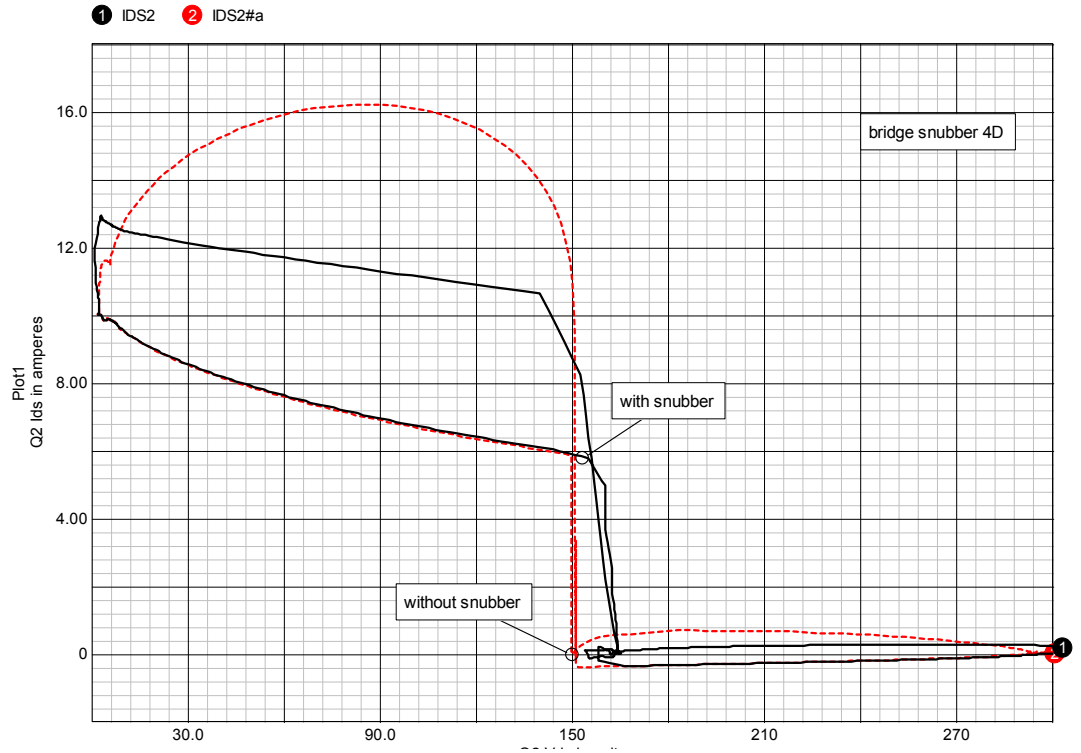


Figure 4-72, load-line with and without inductive snubber. Io=10 A.

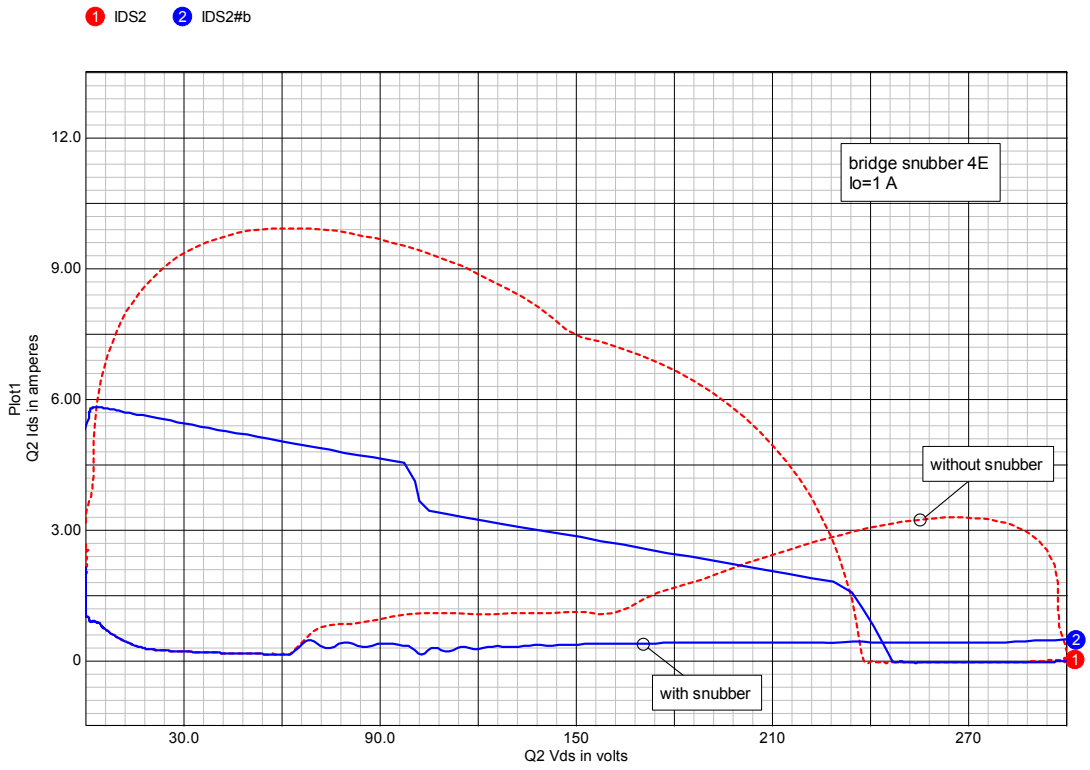


Figure 4-73, load-line with and without inductive snubber. Io=1 A.

The load-lines for Io= 1 and 10 A, with and without the inductive snubber, are compared in figures 4-72 and 4-73. The inductive snubber is very effective during the turn-on portion of the load-line.

The addition of Ls1-Ls2 will limit the peak current even if the switches switch more rapidly and will also moderate the diode reverse recovery current spike when real diodes are used on the output.

Non-linear Ls and/or Cs

The turn-on inductive snubber is very useful, particularly for reducing the effect of diode recovery current spikes. However, at turn-off the energy stored in Ls must be discharged. The larger we make Ls the more effective it is in taming diode recovery but a larger Ls generally means a larger voltage spike at turn-off and more power dissipation in Rs.

One way to retain the turn-on current limiting but reduce the turn-off voltage spike is to use a non-linear or saturable inductor for Ls as shown in figure 4-74.

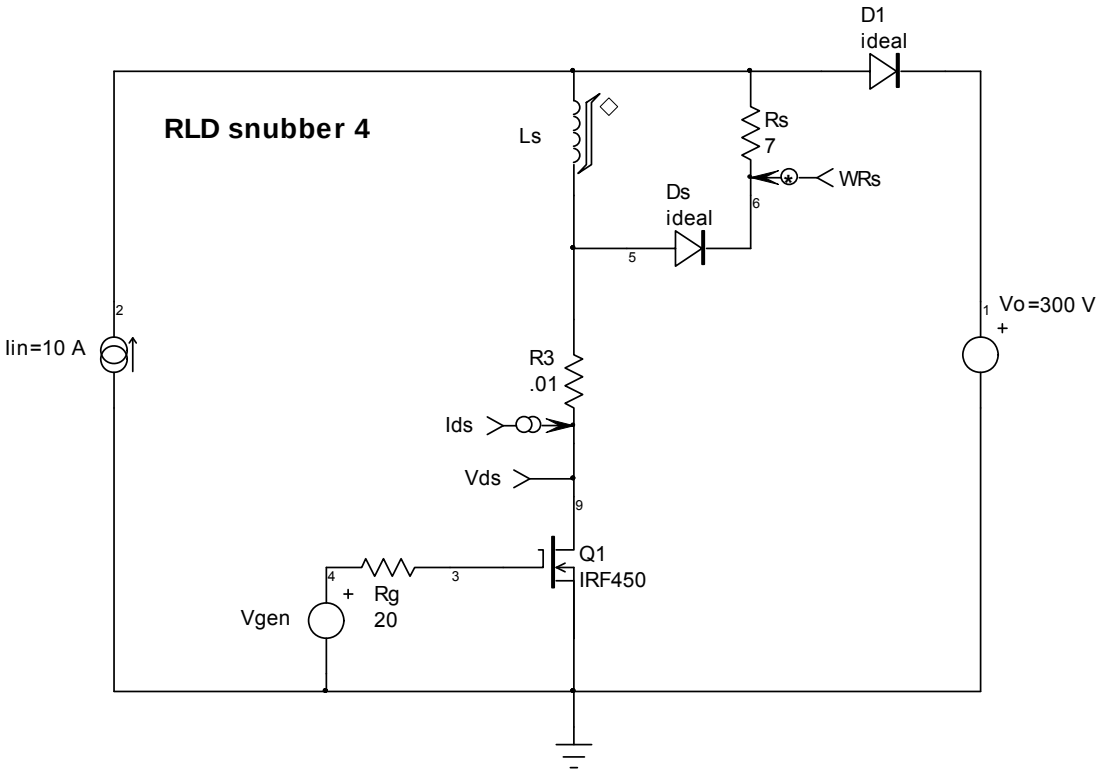


Figure 4-74, example using a saturable inductor for Ls.

At turn-on Ls has the desired inductance, say 1 uH as in previous examples, but the core flux reaches saturation shortly after Q1 is fully on and any associated diode well into reverse recovery. At this point Ls saturates and the value may drop to 0.1 uH or less. The current (Ids) flowing through Ls will keep it in saturation until turn-off and the inductance is still be small. The energy in Ls will one tenth of what it would have been with a linear inductor. The result is much lower energy dissipation at turn-off, a shorter L/R time constant or a smaller value for Rs if the same time constant is retained. Typically the voltage spike will be much smaller.

Another way to use a saturable inductor is shown in figure 4-75.

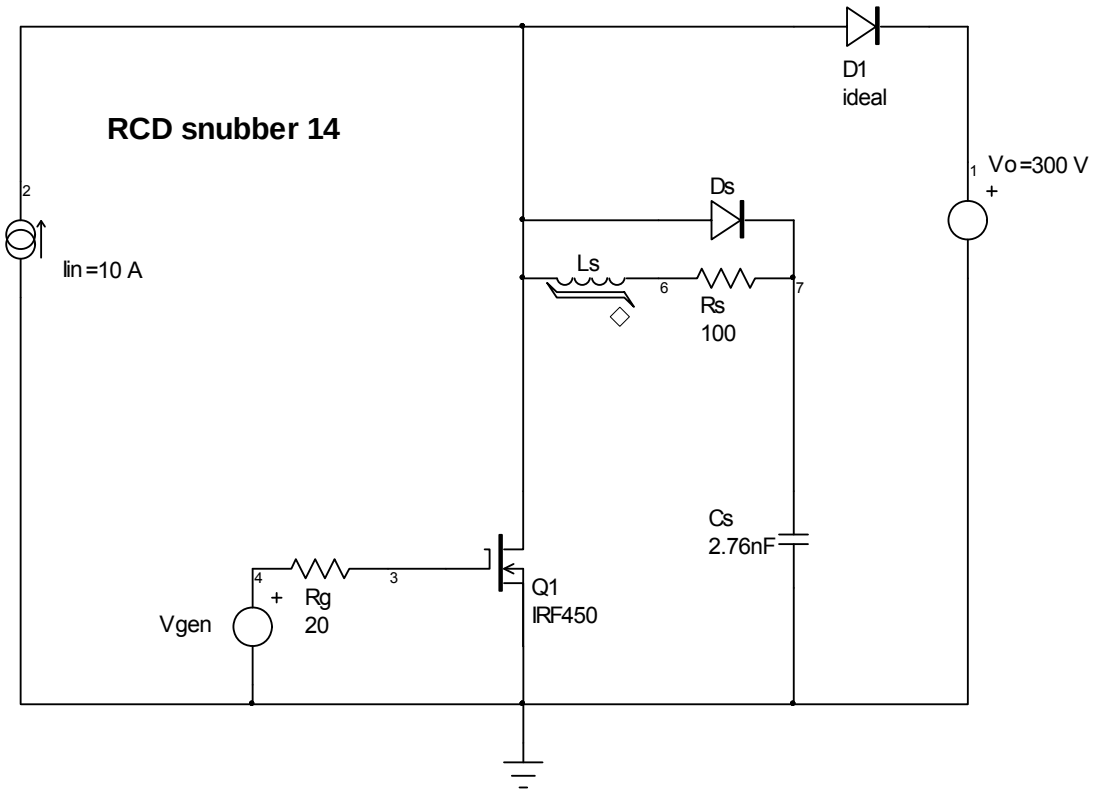


Figure 4-75, saturable inductor used to delay Cs reset current spike.

The idea here is to use the saturable inductor to delay the discharge of Cs at turn-on until Q1 is fully conducting. That should reduce stress and switching loss at Q1 turn-on.

We have the dual problem with Cs in the turn-off snubber. The larger we make Cs the more effective it is in reducing turn-off stress and loss. However, larger Cs means more dissipation at Q1 turn-on as the energy in Cs is discharged. There are non-linear capacitors in which the capacitance varies with voltage that can be used for snubbers. The idea is to have a device with large capacitance at low voltages and small capacitance at high voltages: i.e. a negative coefficient of capacitance with voltage. One example would be a semiconductor junction an example of which was given in figure 3-14 for a MOSFET. In that particular example Coss is about 4 nF at low voltages but drops to 100 pF or so at high voltages. This effect has been implemented in a turn-off snubber using a forward biased diode[469].

Some types of ceramic capacitors can also be used for this purpose. Figure 4-71 shows typical capacitance variation with voltage for different ceramic dielectrics (X7R and Z5U).

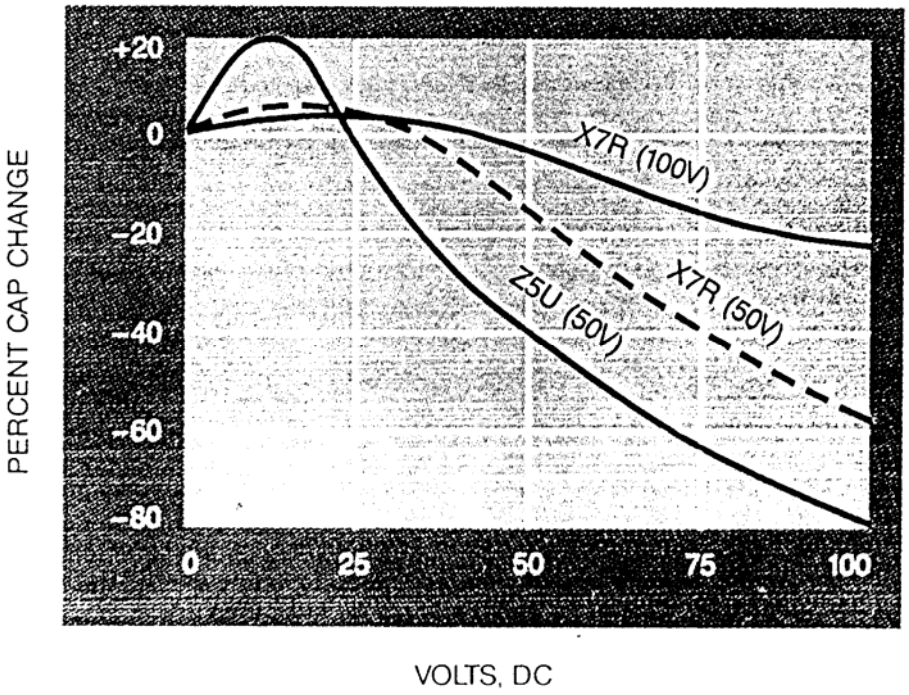


Figure 4-76, capacitance variation as a function of applied voltage.

The idea here is that at the initiation of Q1 turn-off when Vds is low, Cs is large which effectively delays the rise in Vds. When Vds rises to the off-state voltage Cs will be much smaller, perhaps 20% of the initial value. The result is much less stored energy to be dissipated at Q1 turn-on. Unfortunately there are some limitations to using this type of capacitor. Materials which display a large voltage coefficient tend to be quite lossy, have wide tolerances on initial capacitance and be very temperature sensitive. For these reasons the use of a non-linear capacitance in the turn-off snubber can be a bit tricky to implement. If you are interested in using this approach you should consult the work of Steyn, van Wyk and others[407,408,409,410,411,412,413,414,457,458].

Chapter 5

Energy recovery snubbers

The dissipative snubbers described in chapter 4 find very wide application because they are relatively simple and usually result in significant switch stress reduction and at least a small reduction in overall circuit loss. However, as converter power levels rise to the kW and multi-kW range, the power dissipated in the snubber resistors can be substantial and present a thermal management challenge. As converter power levels go above 1 kW it becomes more and more important to employ snubber circuits in which the energy trapped in the snubber reactances is recycled to either the input source or to some useful output load. This can significantly improve overall conversion efficiency and reduce thermal loading.

A wide variety of circuits have been invented to recover energy from a snubber reactive element and we will explore a few of these. By the necessity the number of examples is limited. However, many additional circuits can be found in the bibliography and in the literature on power electronics.

These snubbers can work very well, recovering much of the energy, but there is a price to pay: a larger number of components are needed to implement the snubber and the circuits are more complex in both the hardware and in their electrical behavior.

Energy recovery snubbers fall into two general classes:

1) those that use the switch being protected to implement the energy recovery and,

2) those which use an external switch or even multiple external switches for the energy recovery.

The first category is by far the most common but suffers from the problem of imposing additional turn-on and turn-off stresses on the

switch being snubbed. This is very much like what we saw in dissipative snubbers. As converter power levels rise into the tens of kW the additional complexity of using external switches becomes more attractive because it allows a reduction in primary switch stresses and may actually result in cost reductions, although that depends on the details of the particular application. At higher power levels there are examples where the energy recovery circuit is a multi-kW power converter in its own right. This discussion will be limited to the first category of snubbers

Like dissipative snubbers, energy recovery snubbers are available for turn-on, turn-off or a combination of both.

One important point needs to be made regarding energy recovery snubbers:

> *The snubbing action on the switch is exactly the same as for dissipative snubbers, i.e. inductors for turn-on and capacitors for turn-off. The difference is in how we extract energy from the snubber reactances and recycle it.*

The material in chapter 4 is directly applicable to this chapter and it will be assumed that the reader has read and understood chapter 4.

A turn-off snubber example

A popular energy recovery turn-off snubber circuit is shown in figure 5-1. Cs1 and Cs2 are the turn-off snubbing capacitors. They act in parallel at turn-off so that the effective value is their sum, 4 nF. Ds1 and Ds2 are active at Q1 turn-off. Ds3 and L1 are active during energy recovery at Q1 turn-on. Figure 5-1 is a bit cluttered with measurement points and metering resistors (R2 and R3) but these will be helpful to explain how the snubber works.

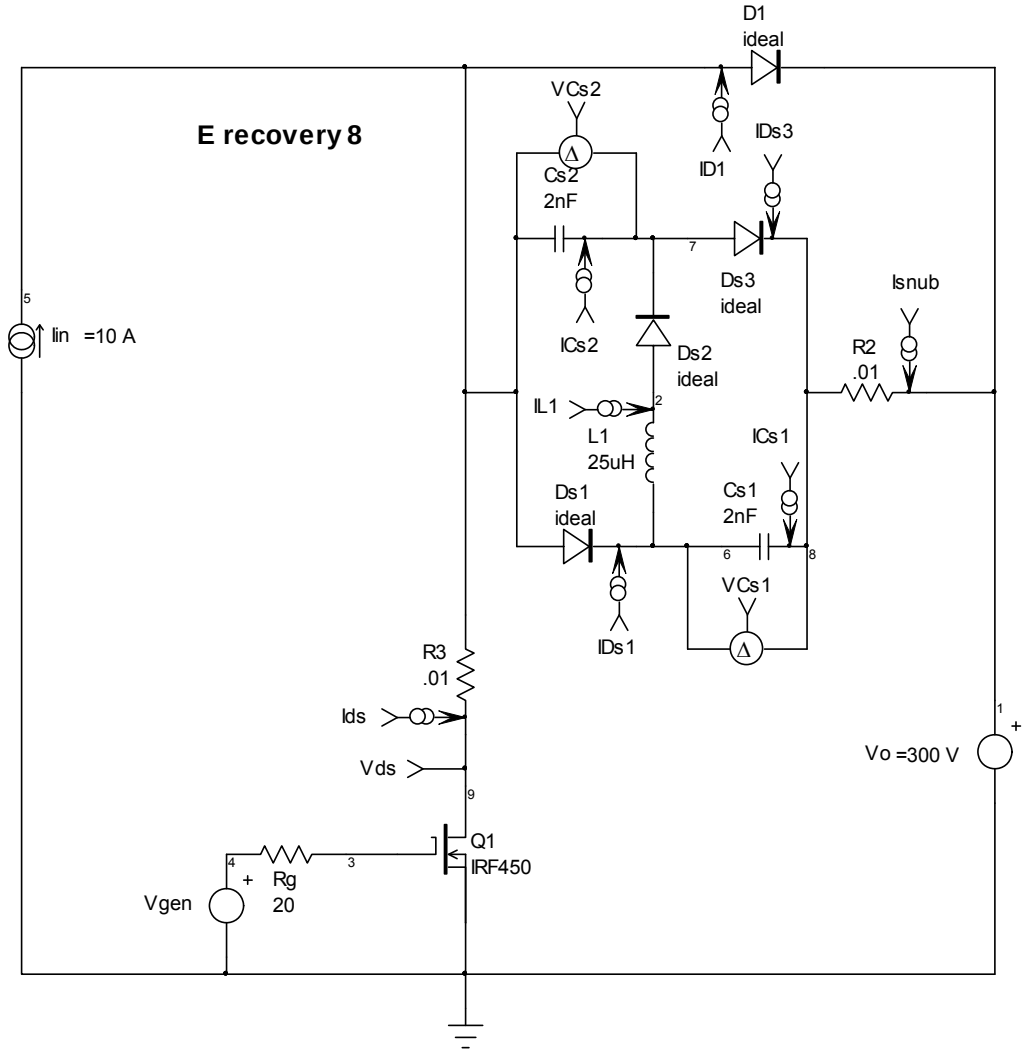


Figure 5-1, a turn-off energy recovery snubber.

We can begin the explanation of circuit operation by looking at the voltage waveforms across Cs1 and Cs2 (VCs1 and VCs2) and the total snubber current waveform (Isnub) during one complete switching cycle shown in figure 5-2. For the moment we are assuming that Cs1=Cs2. In that case VCs1=VCs2 and are represented by a single trace. Later we will see what happens when the two capacitors are not equal.

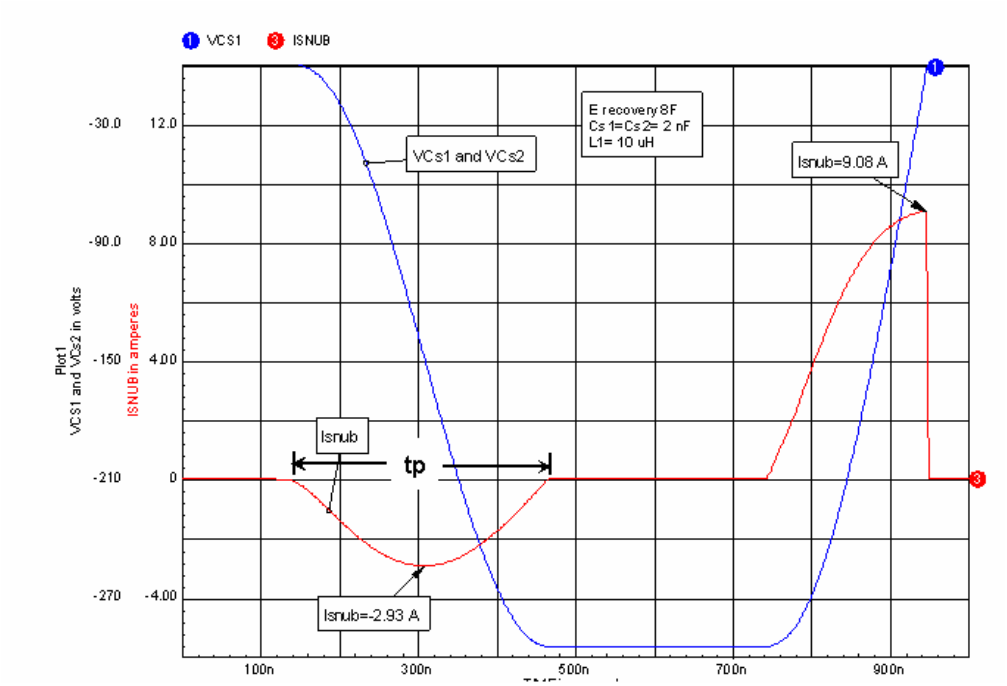


Figure 5-2, Voltage waveforms across Cs1 and Cs2 and current through the snubber (Isnub) over one switching cycle.

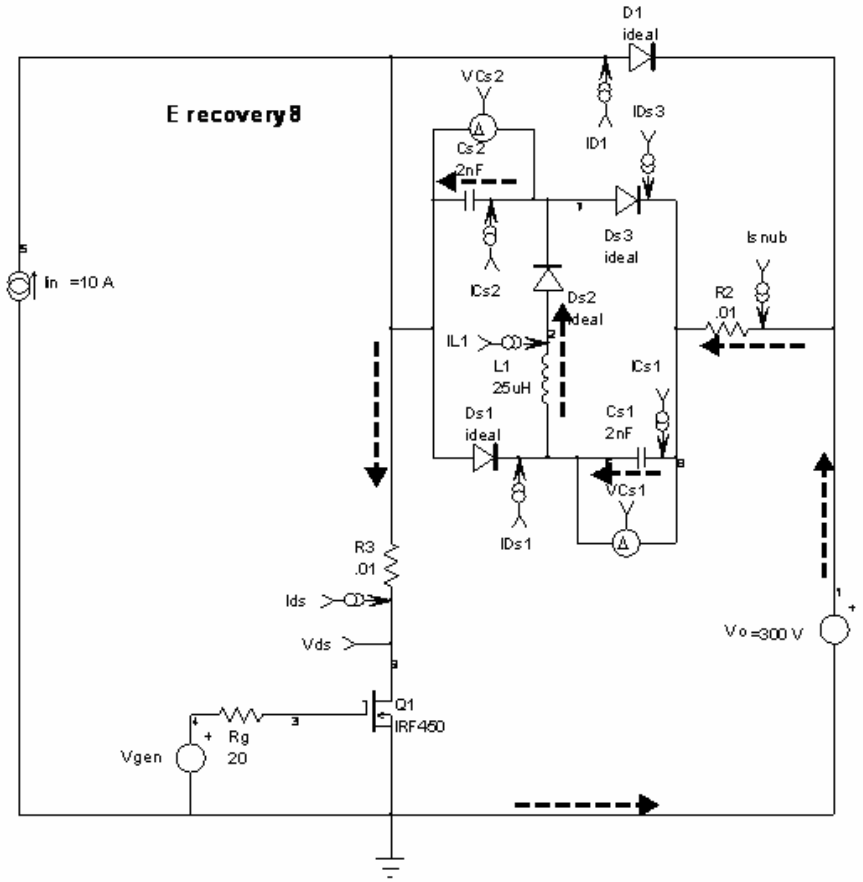


Figure 5-3, current paths in the snubber during Q1 turn-on.

Assume the switching cycle begins just before Q1 turn-on, at that point current is flowing through D1 and VCs1=VCs2=0, i.e. Cs1 and Cs2 are discharged. At turn-on, Cs1 and Cs2 are each charged through the series path that includes Vo, Cs1, Cs2, L1, Ds2 and Q1 as indicated by the dashed arrows in figure 5-3. The current flowing through this path is represented by Isnub in figure 5-2. Cs1 and Cs2 will charge until VCs1=VCs2=-Vo, which is -300 V in this example. At the point where Cs1 and Cs2 are fully charged, Isnub=0. Note that the Isnub current pulse during this interval is determined by the resonance of L1, Cs1 and Cs2 in series. Because of Ds2, this pulse can ring for only 1/2-cycle. When Isnub falls to zero, the ringing is terminated. The time interval of the pulse (t_p) can be calculated from:

$$t_p = \pi \sqrt{L1\left(\frac{Cs1Cs2}{Cs1+Cs2}\right)}$$

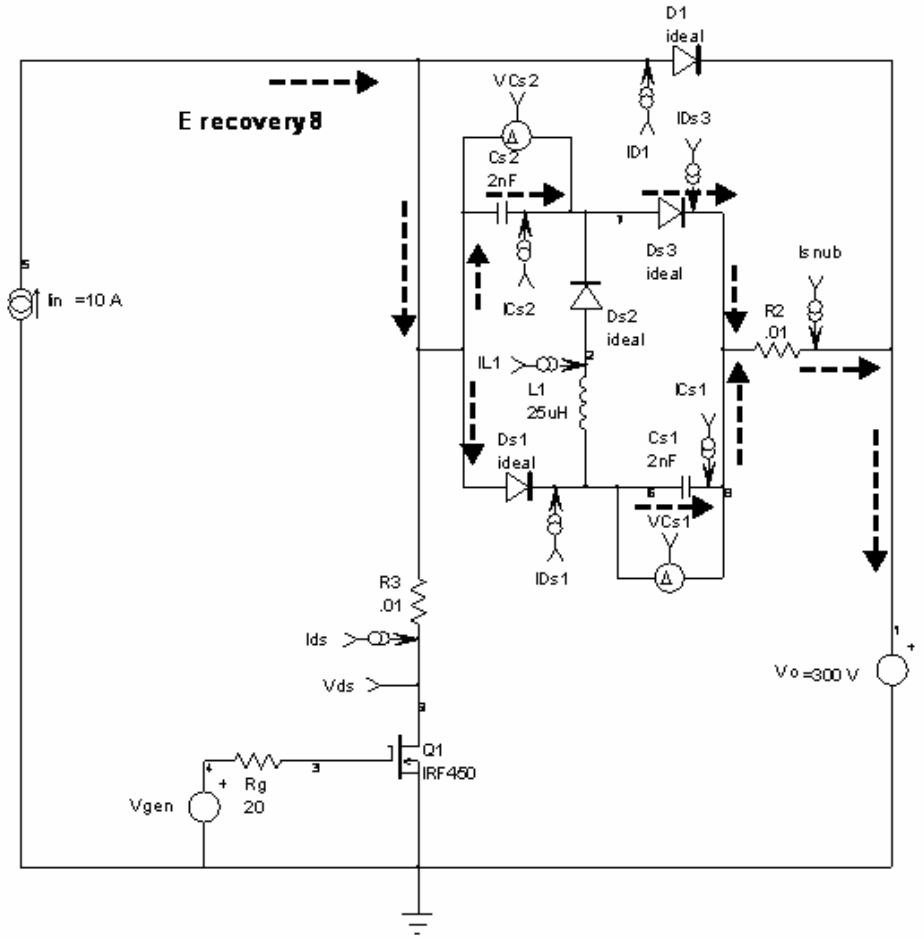


Figure 5-4, current paths in the snubber during Q1 turn-off.

At Q1 turn-off, Cs1 and Cs2 are discharged by the current commutating from the switch through Ds1 and Ds3 to the output (Vo) as shown by the dashed arrows in figure 5-4. Isnub=0 when VCs1=VCs2=0. At this point D1 is in conduction.

We can summarize the snubber energy transfer as follows:

1) Initially Cs1 and Cs2 have no stored energy (VCs1=VCs2=0).
2)At Q1 turn-on Cs1 and Cs2 are charged via L1.
3)At Q1 turn-off the energy stored in Cs1 and Cs2 is returned to the output.

Ids and Vds waveforms for Q1 with the energy recovery turn-off snubber are shown in figure 5-5.

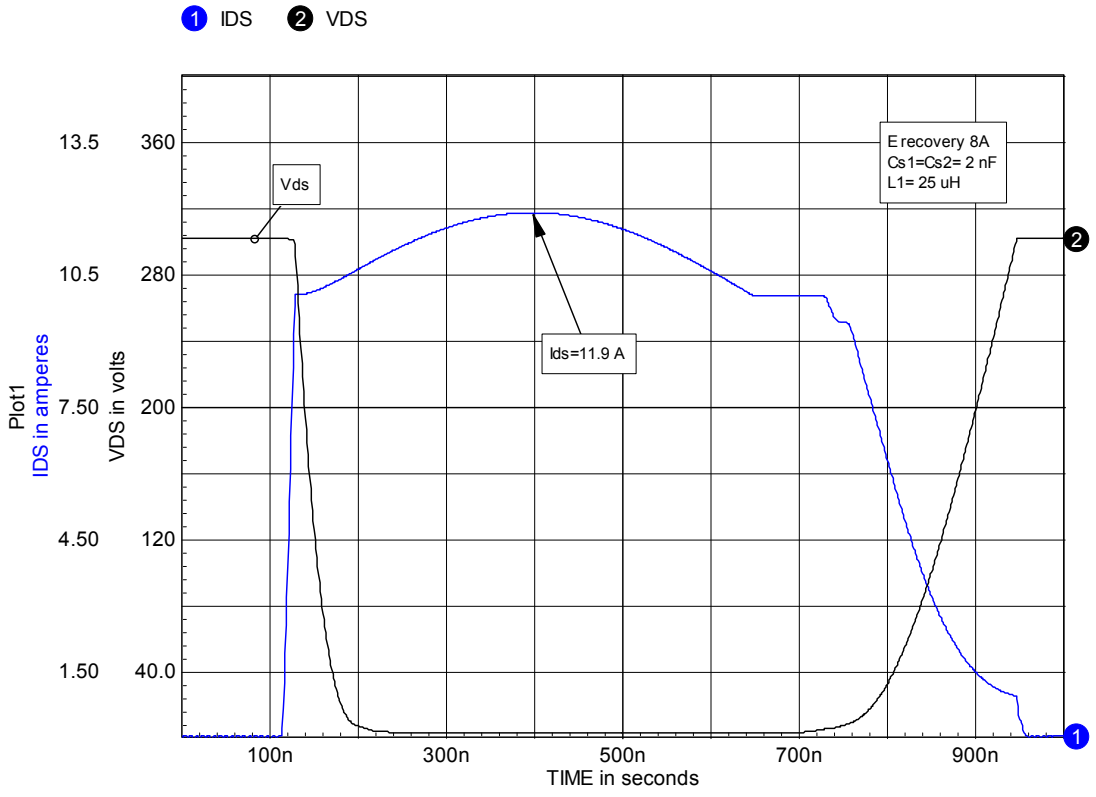


Figure 5-5, Q1 Ids and Vds waveforms.

Q1 turn-on is the normal hard switching and turn-off is a normal capacitive snubber waveform. The 1/2-cycle resonant current pulse

(Isnub) at Q1 turn-on is added to the normal Ids current. However, Isnub does not begin to rise until after Q1 is on so it affects the conduction losses but not the turn-on switching loss.

The load-line associated with figure 5-5 is shown in figure 5-6.

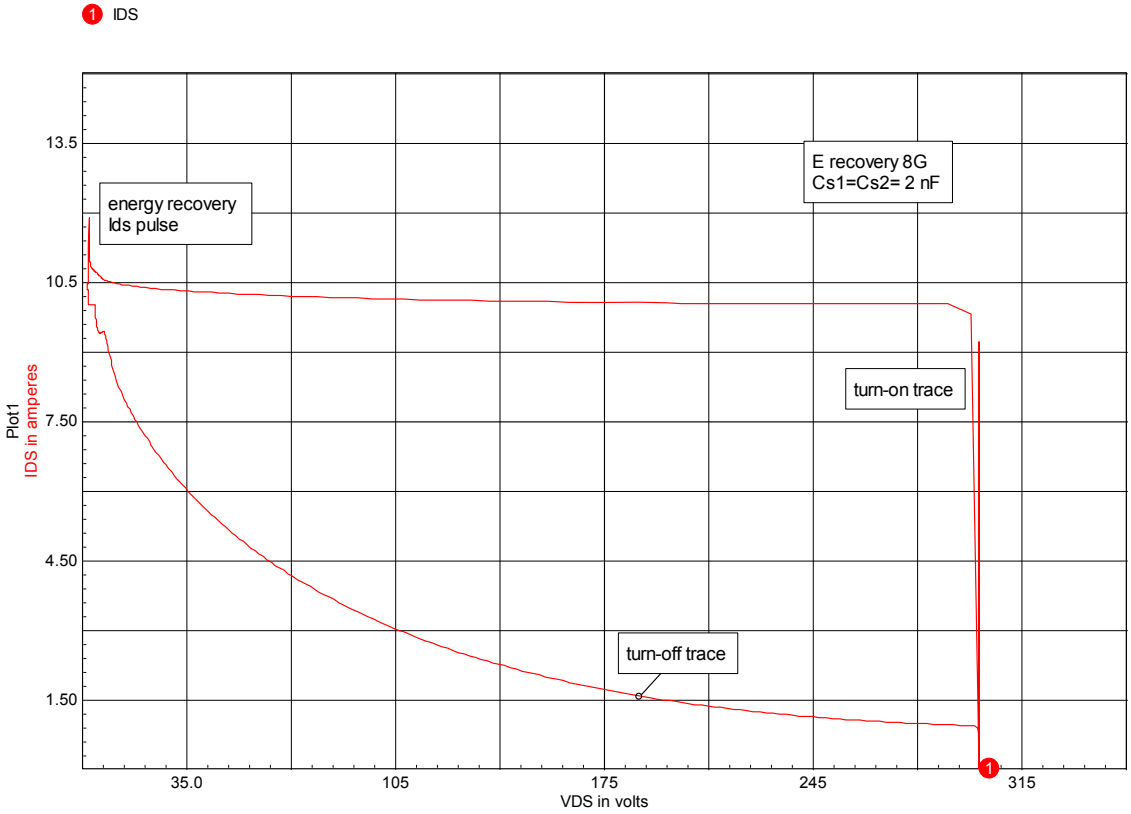


Figure 5-6, Q1 load-line with the turn-off snubber.

This is a perfectly normal capacitive turn-off snubber load-line like those shown in chapter 4. The energy recovery aspect of circuit operation shows up as the current pulse at the end of the Q1 turn-on transition.

t_p and the peak amplitude of the current pulse, for given values of Cs1, Cs2 and Vo, will depend on the value for L1. An example comparing two values of L1 (10 and 25 uH) is given in figure 5-7.

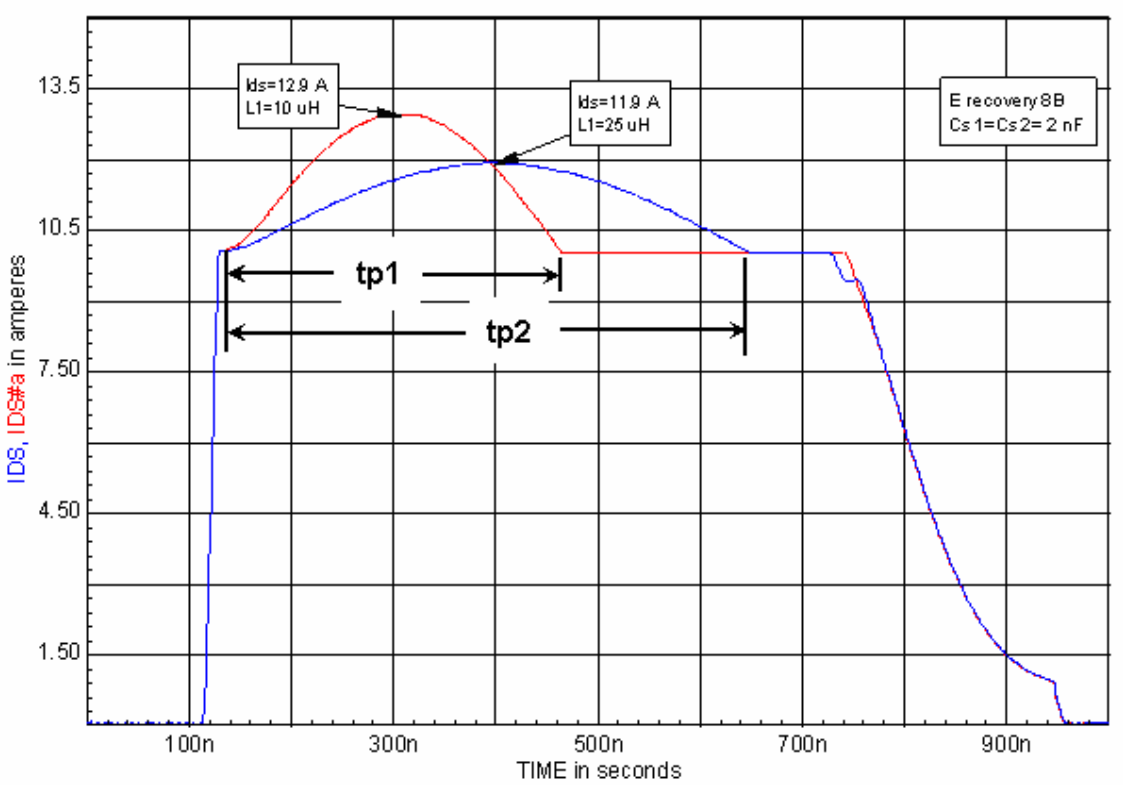


Figure 5-7, effect of different values of L1 on t_p and peak pulse amplitude.

We can reduce t_p by using a small value for L1 but that will increase the peak current.

> *Normally t_p must be less than the minimum on-time of the switch to allow Cs1 and Cs2 charging to reach completion.*

For a given value of t_p, L1 can be calculated from:

$$L1 = \left(\frac{t_p}{\pi} \right)^2 \left(\frac{Cs1 + Cs2}{Cs1 Cs2} \right)$$

As shown in figure 5-8, t_p and pulse amplitude are not affected by variations in the load current. The turn-off Vds waveform is of course

affected by the load current as shown. Again this is normal capacitive turn-off snubber behavior.

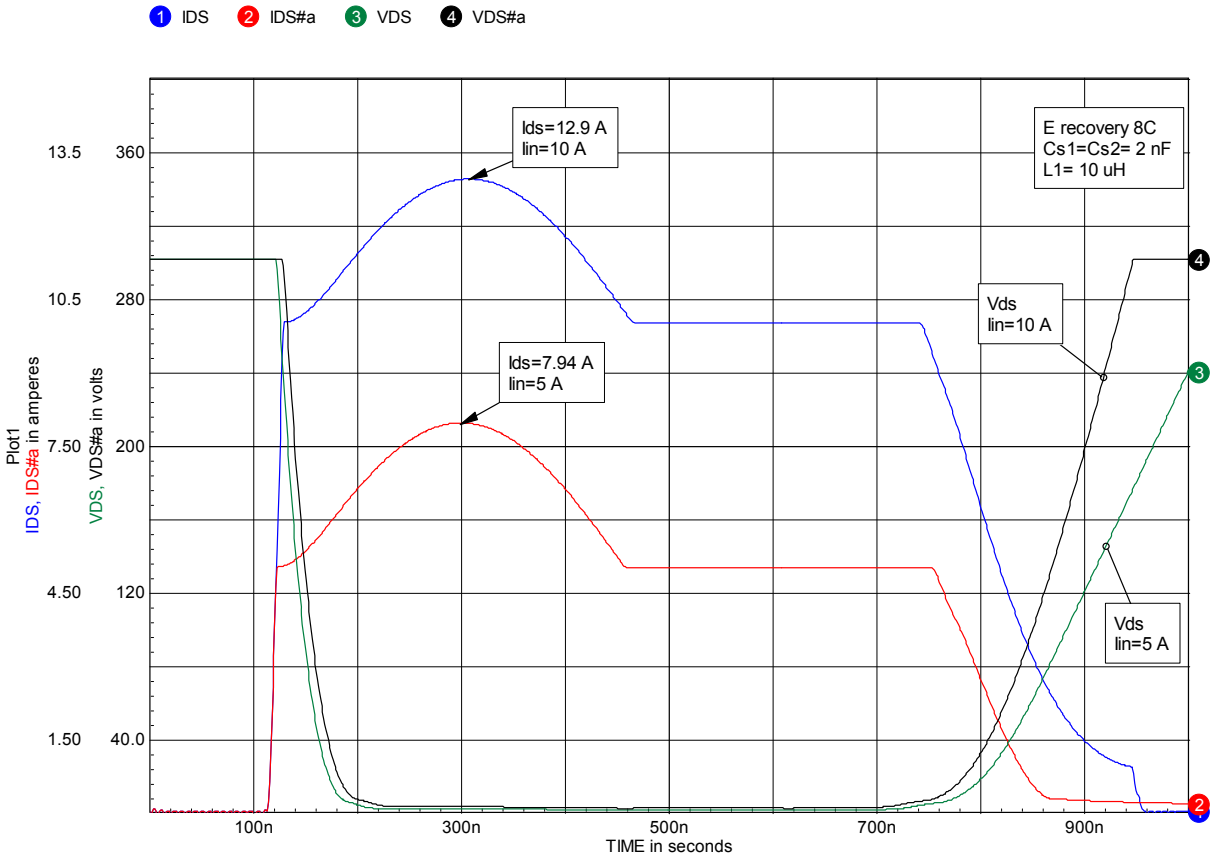


Figure 5-8, Q1 waveforms for different values of load current.

In a practical circuit Cs1 and Cs2 will not be exactly equal and this will have an effect on the waveforms. To illustrate the effect of non-equality in the snubber capacitors we will change the values in figure 5-1 to: Cs1= 1.5 nF and Cs2=2.5 nF. Note that the sum of the two is still 4 nF.

The Ids and Vds waveforms associated with this change are shown in figure 5-9.

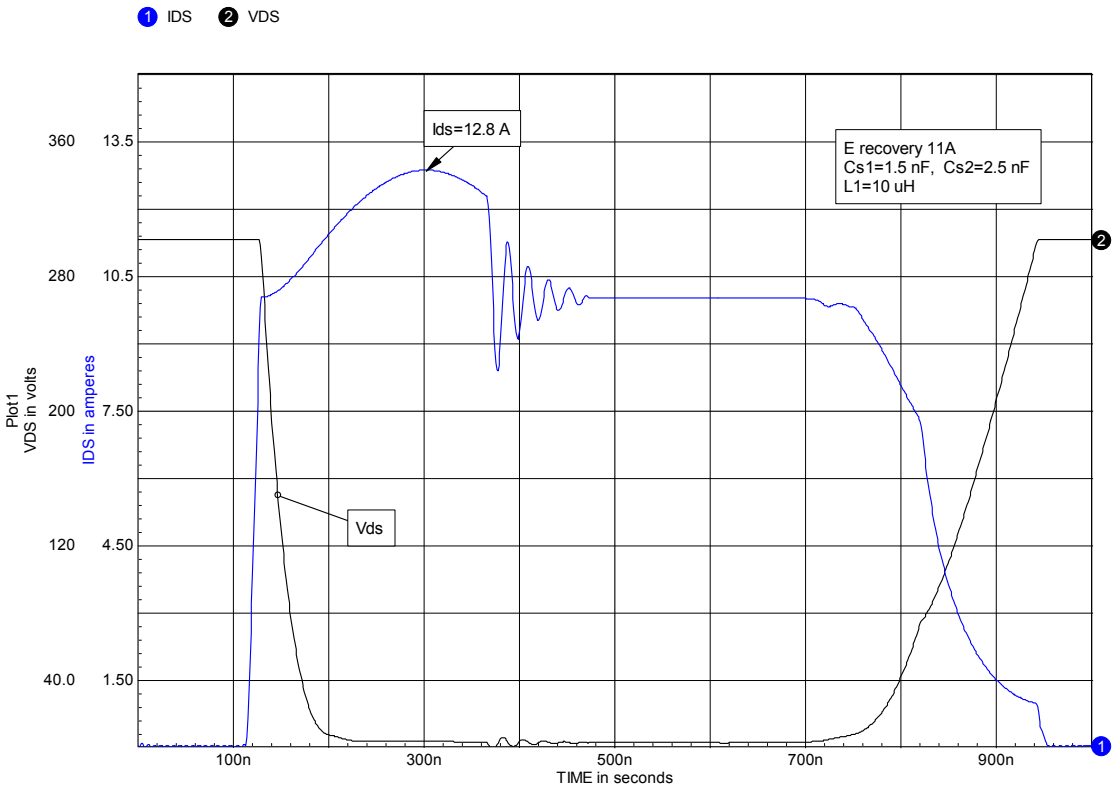


Figure 5-9, Q1 waveforms, Cs1=1.5 nF, Cs2=2.5 nF and L1=10 uH.

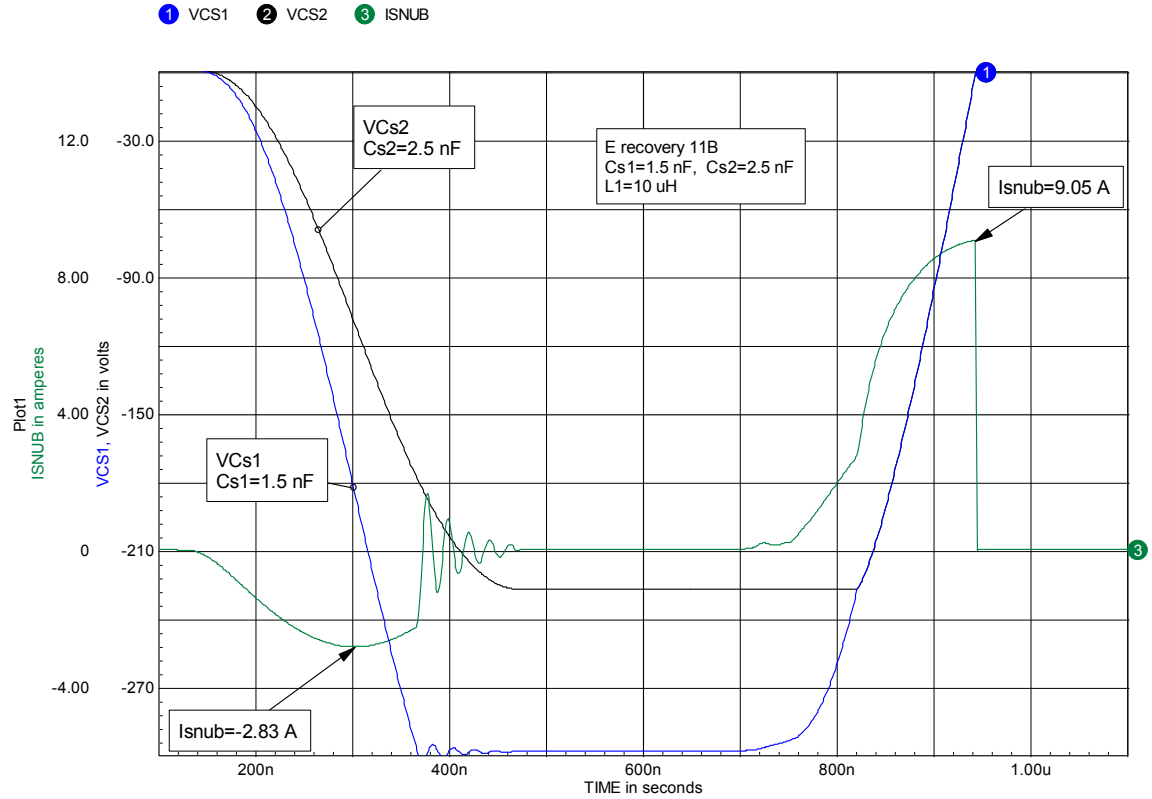


Figure 5-10, VCs1, VCs2 and Isnub for un-equal capacitor values.

Clearly the waveforms have changed! The most obvious change is the termination of the resonant current pulse at Q1 turn-on at less than 1/2-cycle and some associated poorly damped ringing of Ids.

An understanding of what's happening here can be reached by looking at the waveforms for VCs1, VCs2 and Isnub as shown in figure 5-10. It can be seen from the waveforms that the voltages on each snubber capacitor are now different. This is to be expected because the capacitors are charged in series by the same current. The voltage across the smaller capacitor (Cs1) will rise more quickly than the larger one (Cs2). The charging pulse (Isnub) will terminate when one of the capacitors reaches -Vo. The subsequent ringing is due to the resonance of the snubber capacitance with the Q1 package inductance. In a practical circuit there will be other parasitic inductances and the ringing may be even more pronounced.

Fortunately the ringing is easy to damp. If we make R2 in figure 5-1 a real resistor rather than for metering and change the value to 2 Ohms, the ringing will be nicely damped as shown in figure 5-11. The additional loss introduced by this small a value of resistance is usually small, about 16 µJ in this example.

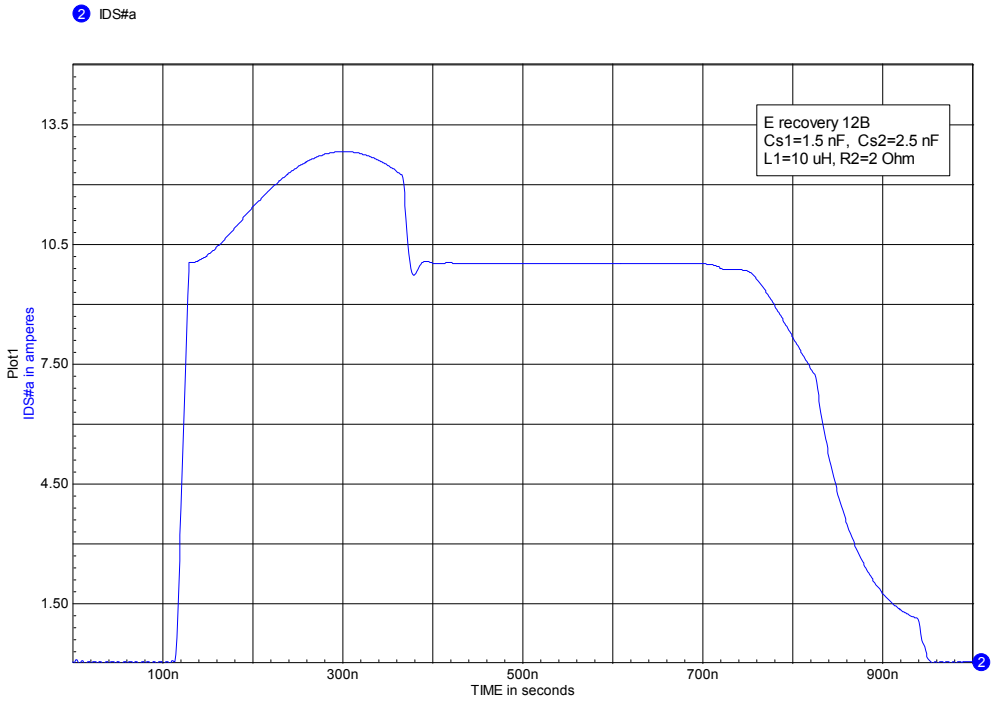


Figure 5-11, Q1 Ids waveform with R2=2 Ohm.

What effect does non-equal values for Cs1 and Cs2 have on the switch energy loss? It turns out, not much. The loss with equal capacitors is 164 µJ per switching cycle and 173 µJ for the non-equal case. In the non-equal case there is another 16 µJ lost in R2 which is needed for damping.

The degree of mismatch between capacitor values used in the above example is quite large. In a real circuit the capacitors will usually be matched more closely than this and the loss due to the mismatch very small. However, some ringing may still appear and have to be damped. It doesn't matter which capacitor is the larger, the waveforms will still be the same.

In the literature there are many variations of the circuit arrangement shown in figure 5-1. One common variation is shown in figure 5-12.

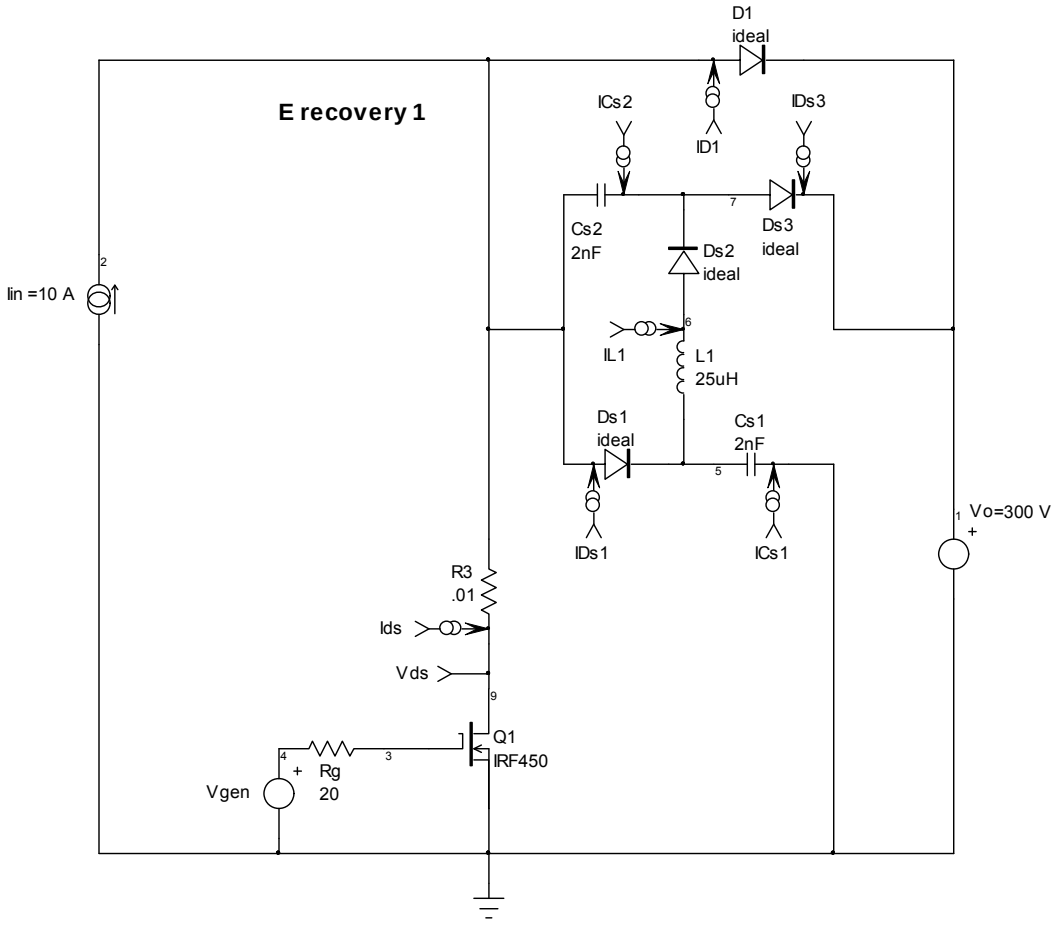


Figure 5-12, a common variation of the snubber circuit in figure 5-1.

The only difference between figures 5-1 and 5-12 is that the connection to one end of Cs1 has been moved from Vo to ground. This change has no effect on Q1 Ids and Vds waveforms. The snubber performs the same. This variation does have one advantage which is useful in practice. As shown in chapter 4, parasitic inductance in series with the snubber capacitors reduces the snubber effectiveness. In the variation shown in figure 5-1, the path through Vo will, in a real circuit, be through the output filter capacitors and their ESL and connection parasitic inductance. The variation in figure 5-10 allows this problem to be minimized because the path including Q1, Ds1 and Cs1 can have much less parasitic inductance if careful layout is employed. This point is discussed in chapter 6 under layout issues and recommendations.

When this type of snubber is used in other topologies it may appear to be different when in fact it is same. Variations of this snubber applied to a buck converter are shown in figure 5-13.

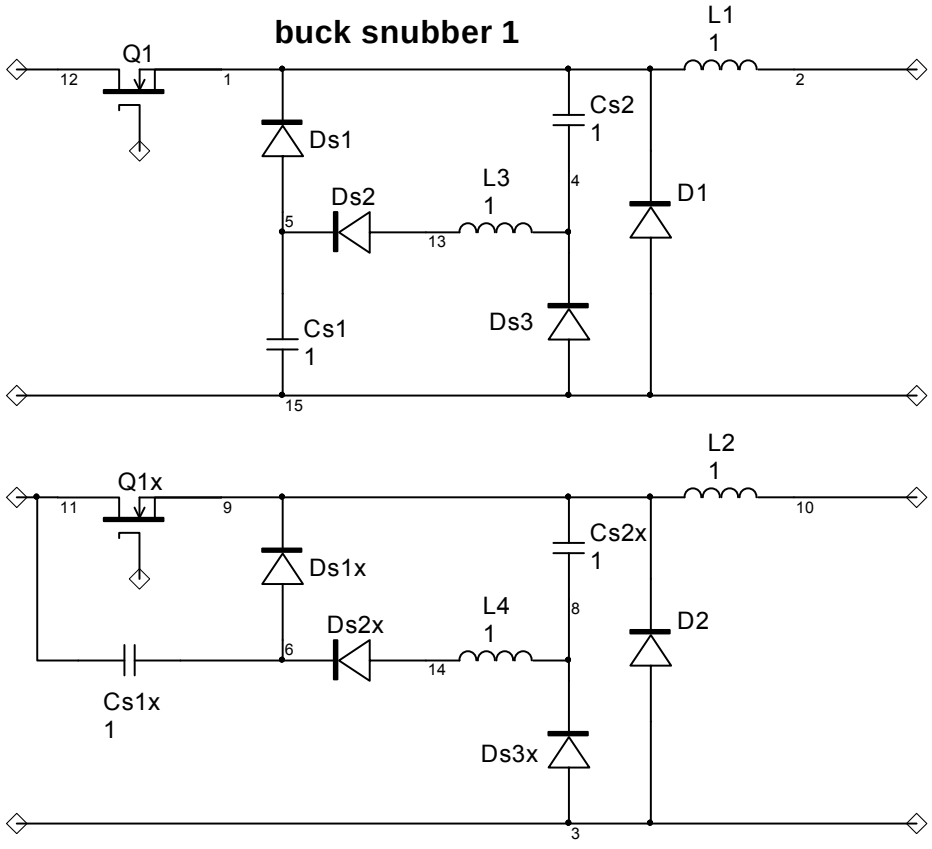


Figure 5-13, turn-off energy recovery snubbers in a buck converter.

Turn-on snubber example 1

As shown in chapter 4, an inductive turn-on snubber can be very helpful in mitigating the effects of diode reverse recovery on switch losses. Figure 5-14 gives an example of an energy recovery turn-on snubber in a circuit with real diodes.

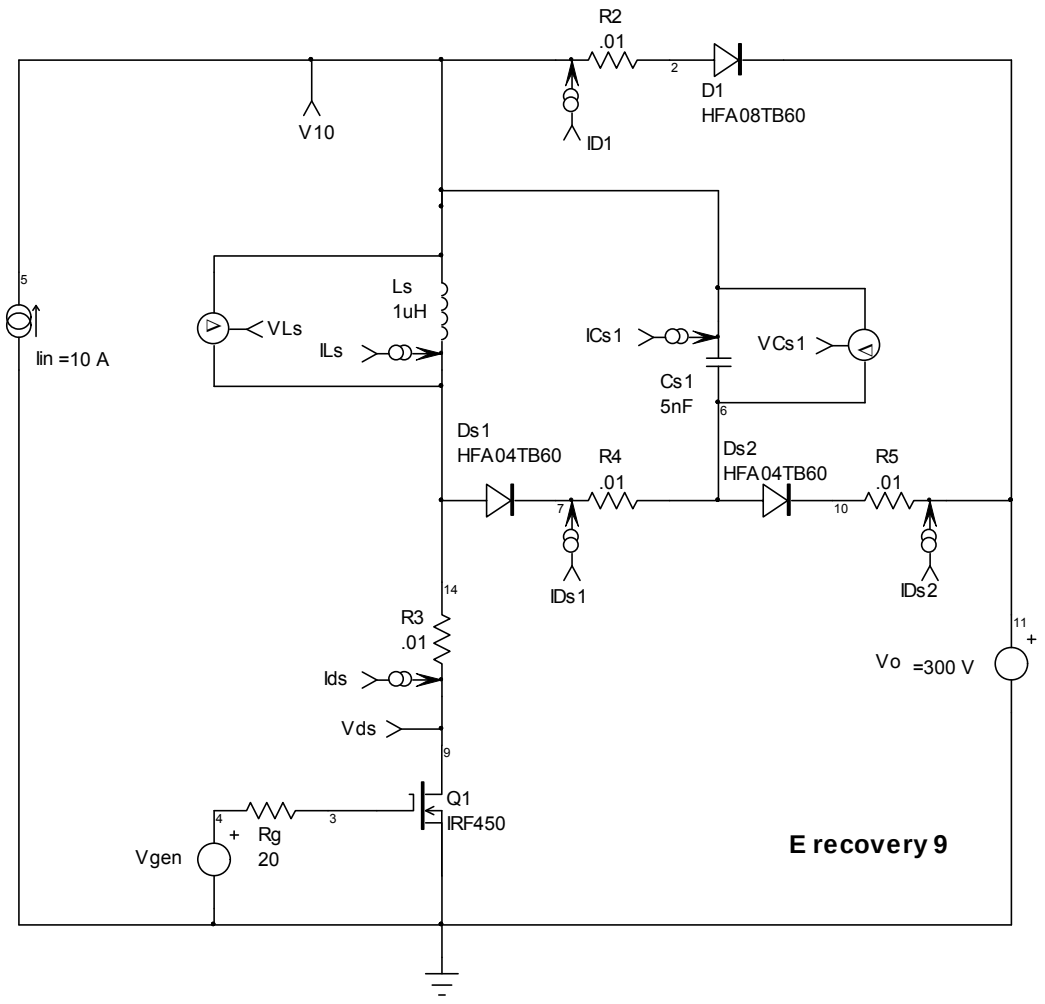


Figure 5-14, example of an energy recovery turn-on snubber.

The snubber components are Ls, Cs1, Ds1 and Ds2. Q1 waveforms with this snubber are shown in figure 5-15 (to see these waveforms without the snubber see figure 4-33). It should be noted that the value for Ls is chosen in exactly the same way as for the dissipative inductive turn-on snubber. Also, Cs1 is not part of the snubbing

action, it is part of the energy recovery mechanism and its value is chosen by a different criterion than would be the case in a capacitive turn-off snubber.

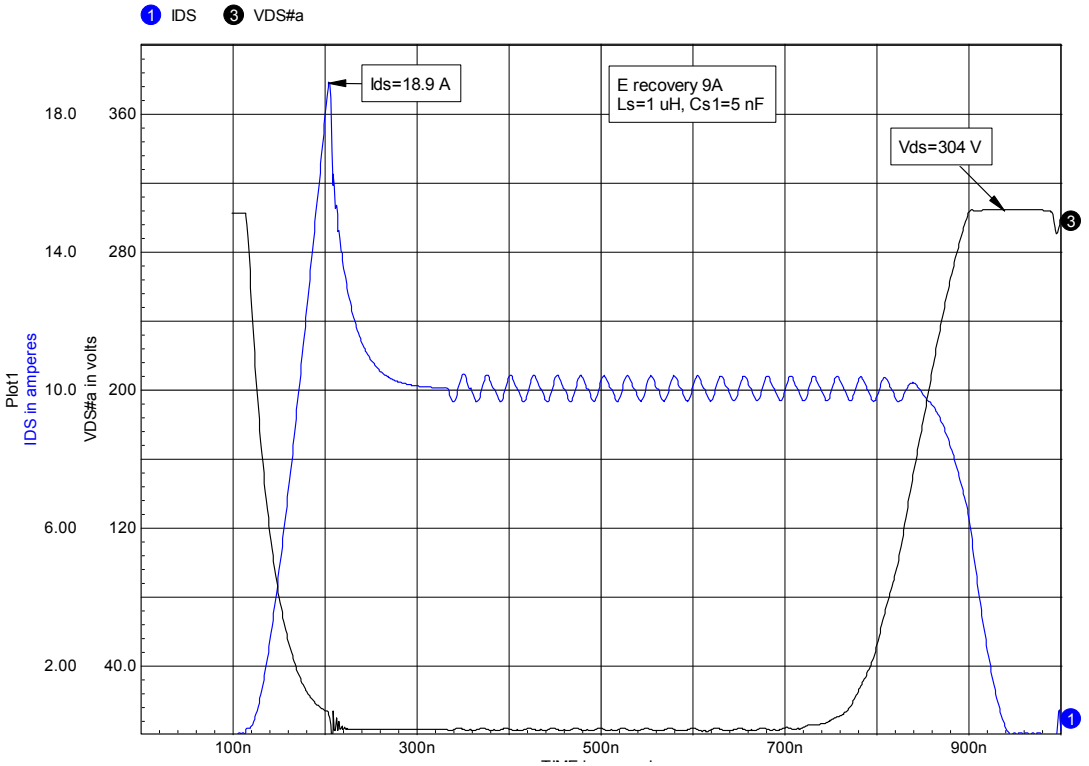


Figure 5-15, Q1 waveforms using the turn-on snubber in figure 5-14.

Turn-on and turn-off are normal waveforms for an inductive turn-on snubber. However, there is substantial ringing on the Ids waveform but on the plus side the Vds voltage spike at turn-off seems to be clamped to a low level (the Vds voltage spike at turn-off with a dissipative snubber is shown in figure 4-35).

Before going into the details of how this snubber works we need to get rid of the ringing. Figure 5-16 shows the voltage waveform at node 5 (the junction of D1, Ls and Iin).

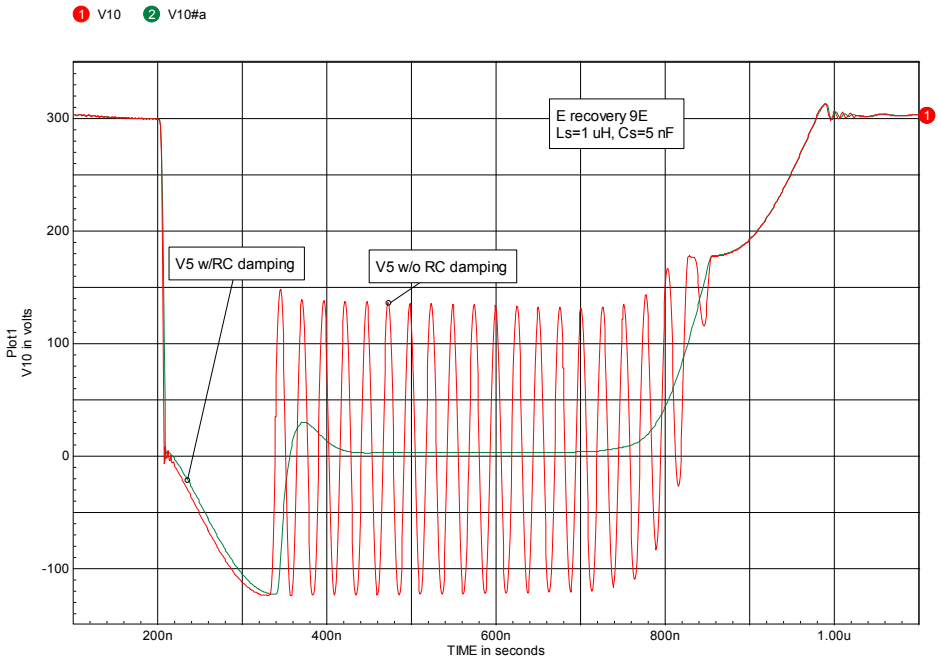


Figure 5-16, voltage ringing at node 5, with and without an RC damping network.

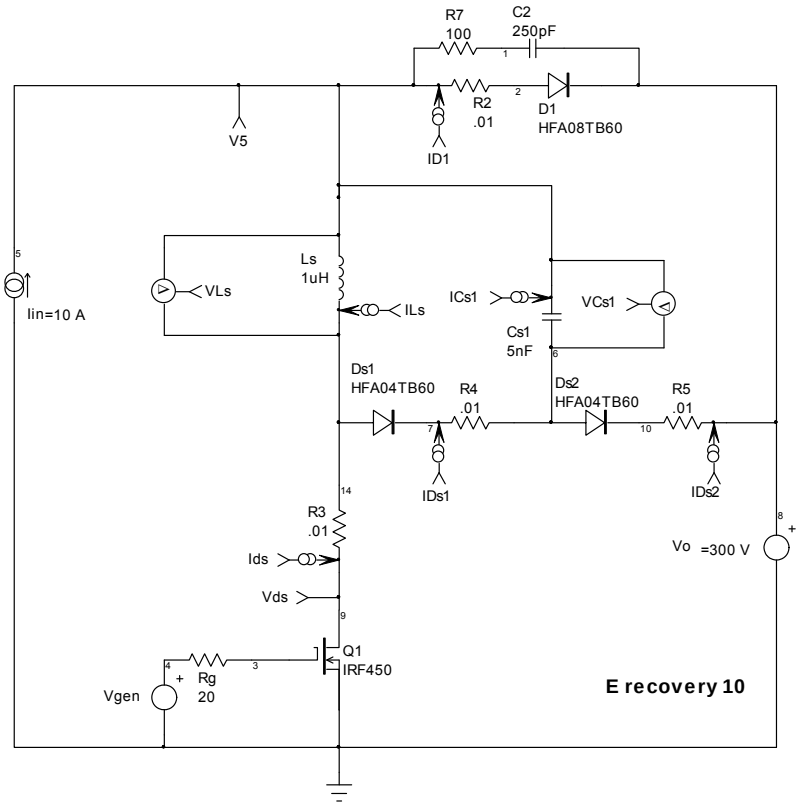


Figure 5-17, adding an RC-snubber (R7 & C2) across D1.

Without some damping, the voltage ringing can be very large. The problem stems from Ls ringing with the reverse capacitance of D1. We can suppress this ringing by adding an RC snubber across D1 as shown in figure 5-17.

The effect of the RC damping network on the voltage at node 10 is also shown in figure 5-16. The RC damping is very effective. When using this energy recovery turn-on snubber, it should be taken for granted that an additional RC snubber will be required across D1and is an integral part of the snubber circuit. This is a very good example of the type of ringing which frequently accompanies energy recovery snubbers because this type of snubber, in the ideal case, has no internal damping. As we will see in further examples, the need for RC-damping networks is quite common in energy recovery snubbers and is a limiting factor on the achievable energy savings.

We can now proceed to explain the operation of this snubber. With the addition of the damping network the Q1 waveforms will be as shown in figure 5-18.

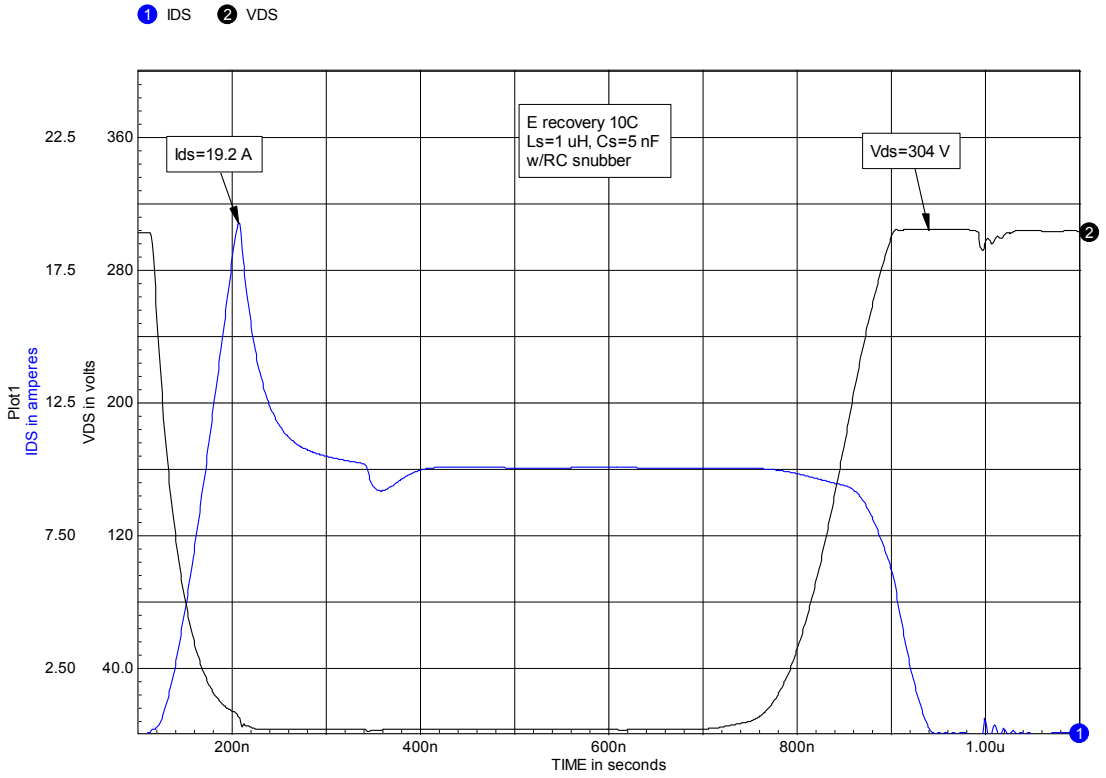


Figure 5-18, Ids and Vds with RC damping network added.

Note that unlike the dissipative inductive turn-on snubber (figure 4-35), there is no voltage spike on Vds at turn-off. This is because the drain of Q1 is clamped to Vo by Ds1 and Ds2 in series.

A comparison of the power dissipation and energy loss with and without the snubber is given in figure 5-19.

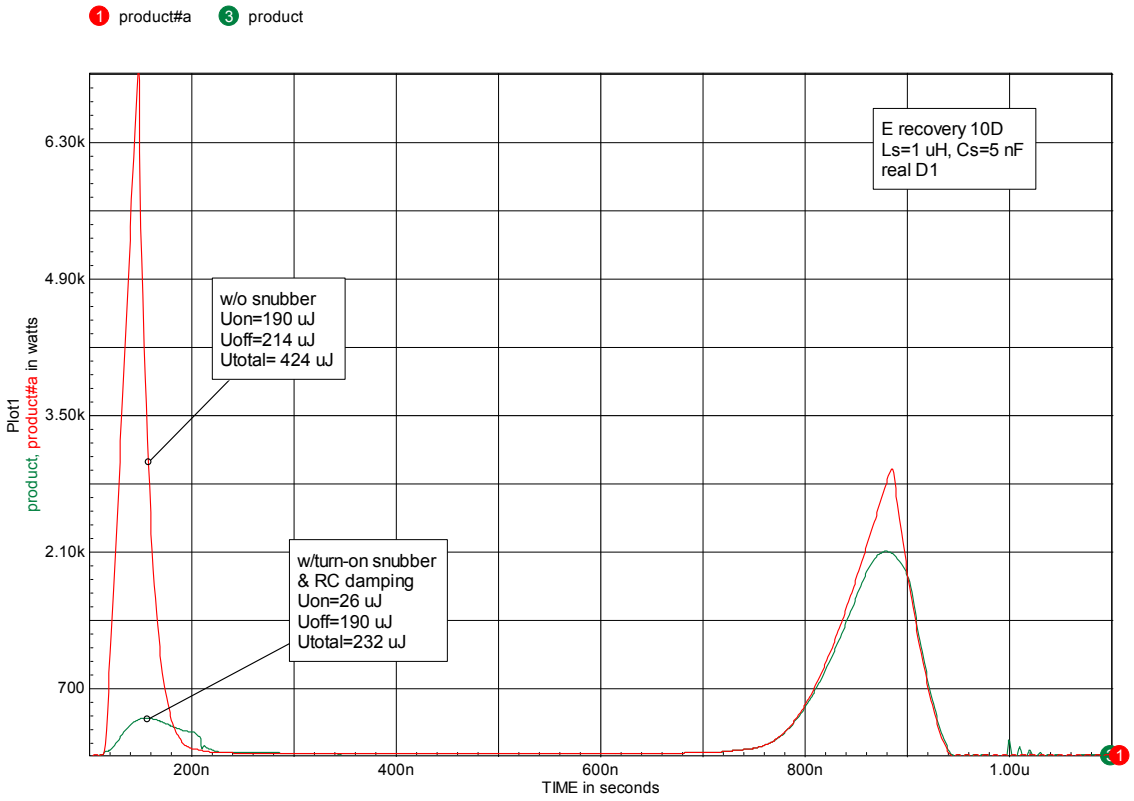


Figure 5-19, comparison of power dissipation and energy loss per switching cycle with and without the snubber.

It can be seen that the snubber is very effective at reducing the turn-on loss and even the turn-off loss is reduced somewhat. The loss reduction at turn-off is due to the elimination of the Vds voltage spike and to a small extent by the turn-off snubbing action of the RC-damping network. The load-line for Q1 with this snubber is shown in figure 5-20. Overall, this can be very effective snubber.

We have just gone through a brief overview of the performance of this particular snubber. As is frequently the case with energy recovery snubbers, the detailed circuit operation is fairly complex.

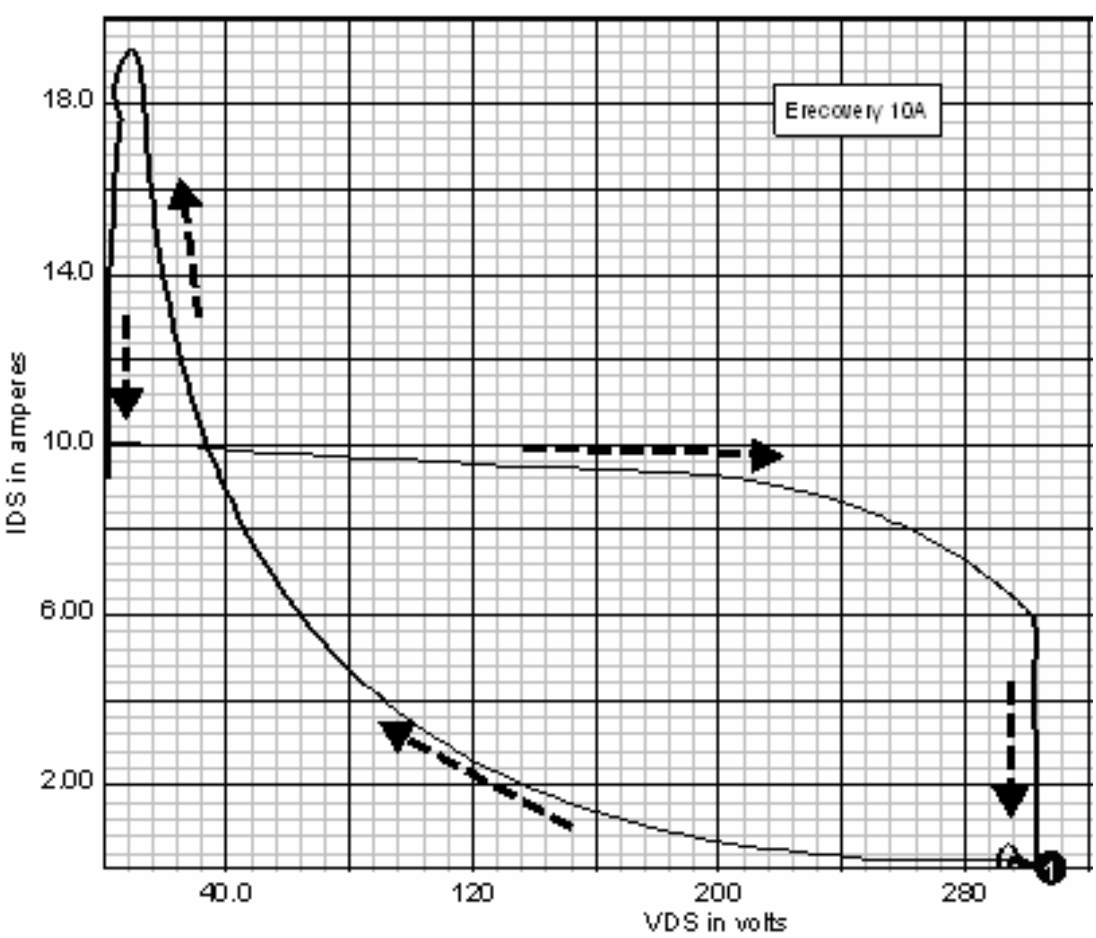


Figure 5-20, Q1 load-line with the energy recovery snubber.

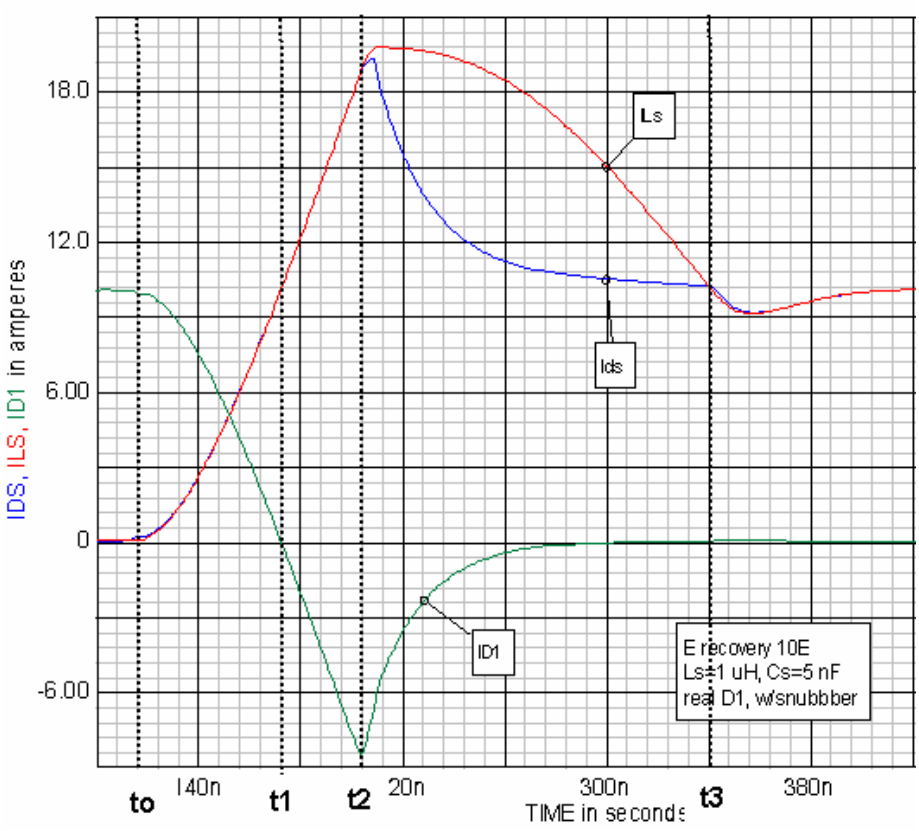


Figure 5-21, Ids, ILs and ID1 at Q1 turn-on.

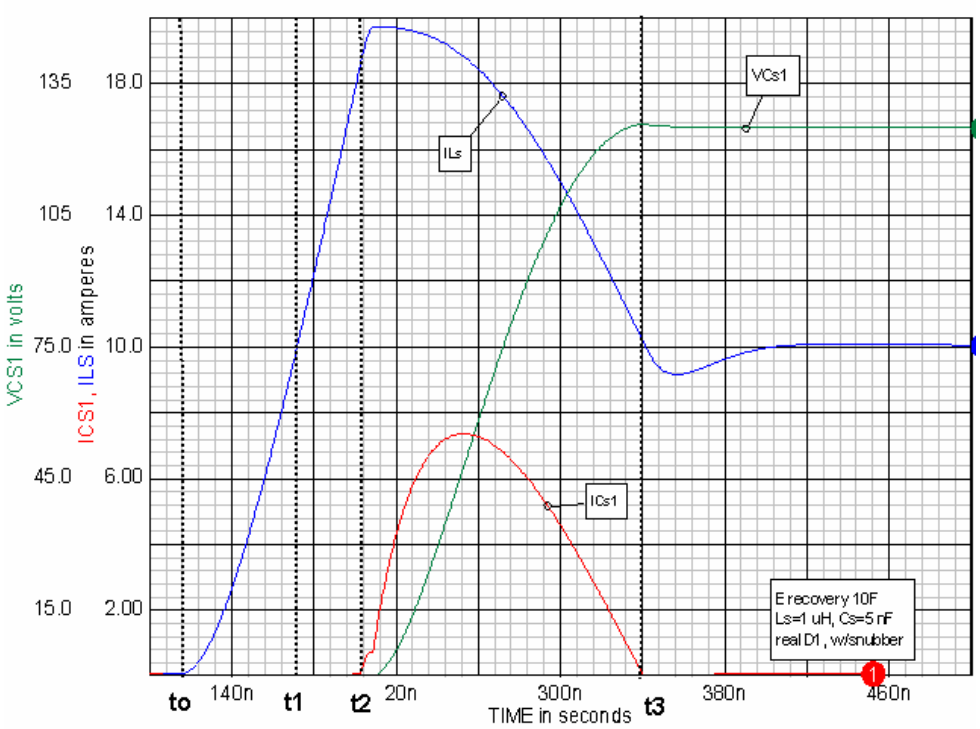


Figure 5-22, ILs, ICs1 and VCs1 at Q1 turn-on.

To better understand the detailed behavior of the snubber and to select values for the snubber components we will need to examine the waveforms and the current flow during a complete switching cycle.

Figures 5-21 and 5-22 show the voltage and current waveforms associated with Q1 turn-on. Three time intervals are defined with vertical dashed lines: to-t1, t1-t2 and t2-t3. Figures 5-23 through 5-25 show the current flow within the circuit during each of these time intervals.

During interval to-t1 (figure 5-23), right after the turn-on of Q1, the forward current in D1 (ID1) is falling and the input current is commutated to Ls and Q1. Both Ids and the current in Ls (ILs) are increasing and ILs=Ids.

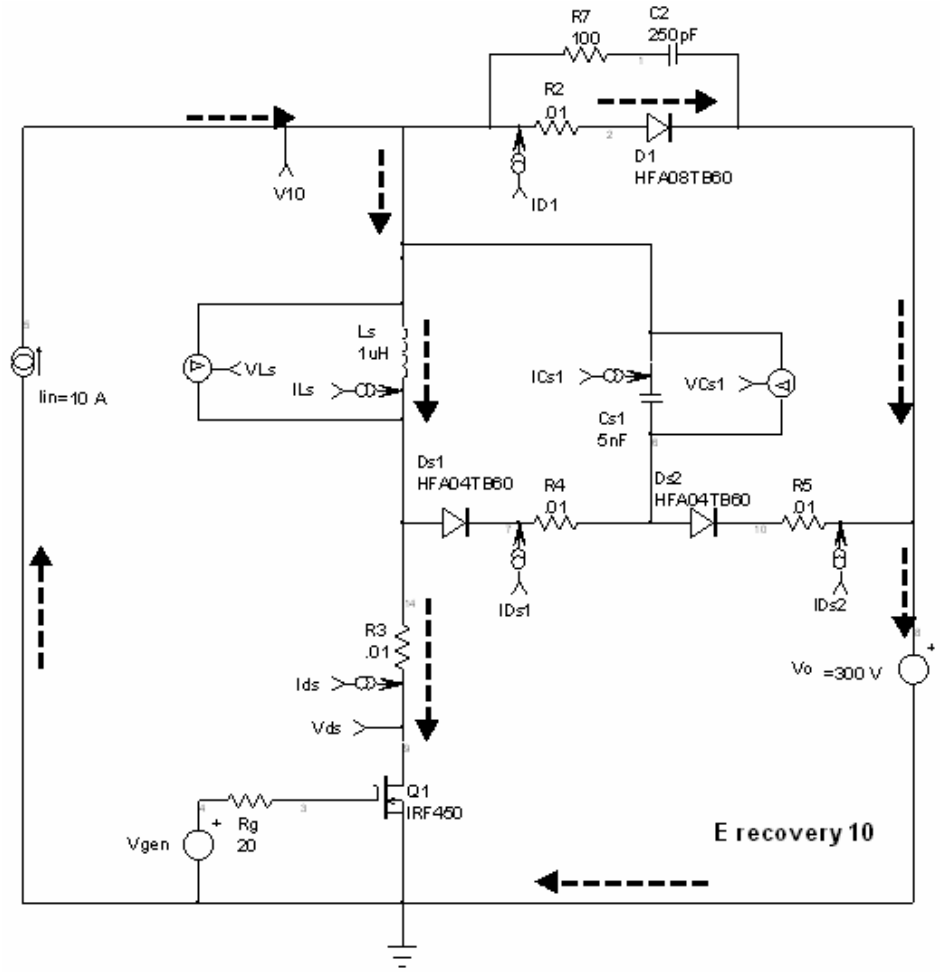


Figure 5-23, current flow during interval to-t1.

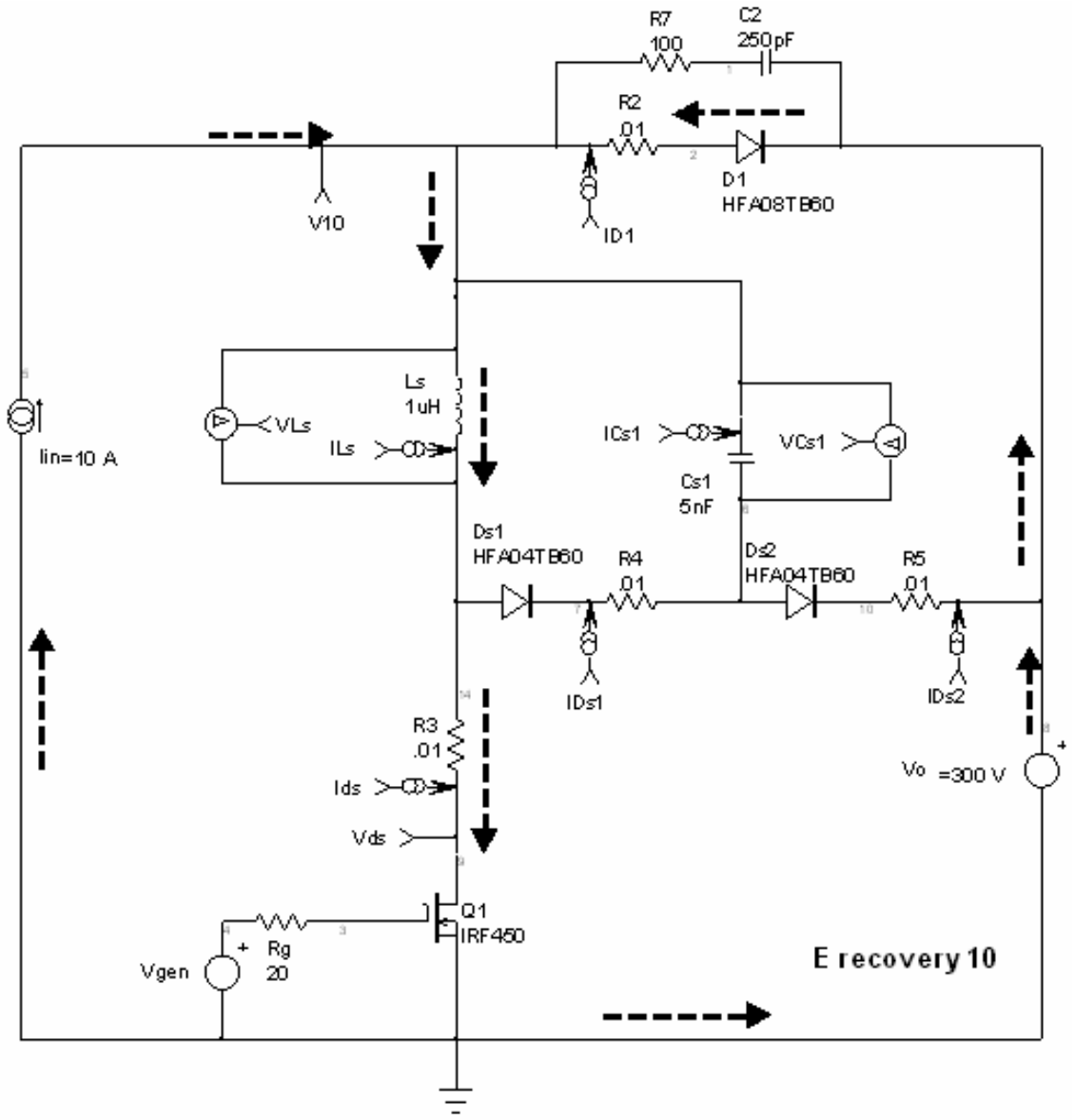


Figure 5-24, current flow during interval t1-t2.

At t=t1, ID1=0 and D1 enters the first phase of reverse recovery during interval t1-t2. As shown in figures 5-20 and 5-24, ID1 has reversed. ILs and Ids continue to increase. During the interval to-t2, there is no current flow in Ds1, Ds1 or Cs1 and ILs=Ids.

At t=t2, the initial phase of D1 reverse recovery is complete and ID1 starts to decrease. At this point ILs no longer remains equal to Ids. During the interval t2-t3 (figure 5-25) the difference between Ids and

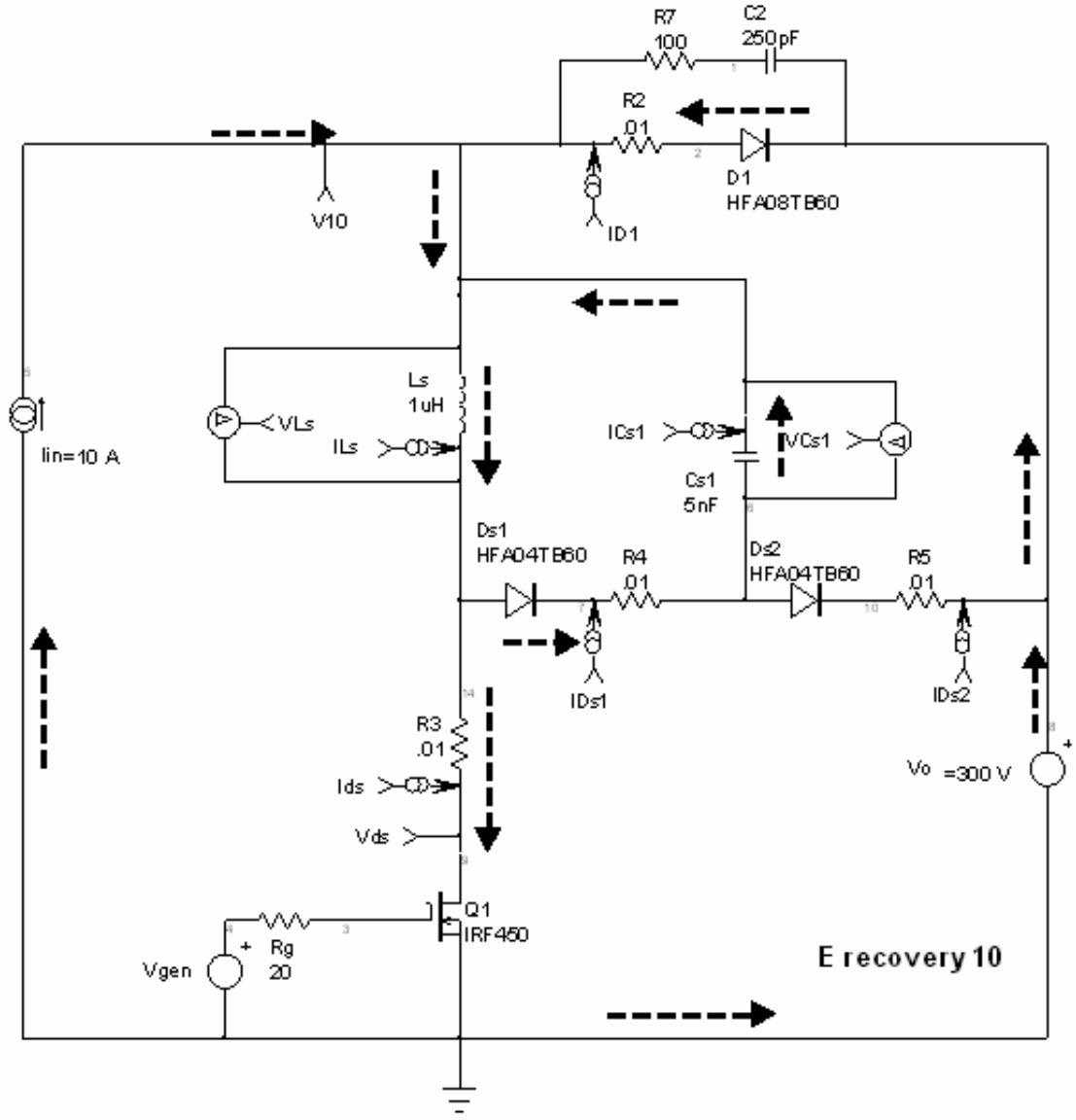


Figure 5-25, current flow during interval t2-t3.

ILs forces Ds1 into conduction and current flows into Cs1 (which has discharged before Q1 turn-on). As can be seen in figure 5-21, during this interval a pulse of current is flowing through Cs2 which charges it. Also during this interval ILs is falling. Some of the energy in Ls is being transferred to Cs1.

At t=t3, the energy transfer from Ls to Cs1 is complete and once again ILs=Ids. Ds1 stops conducting and the voltage across Cs1 (VCs1) is constant at 126 V (for this example). At this point Q1 is on and in it's normal conduction state which continues until Q1 begins to turn off at t=t4.

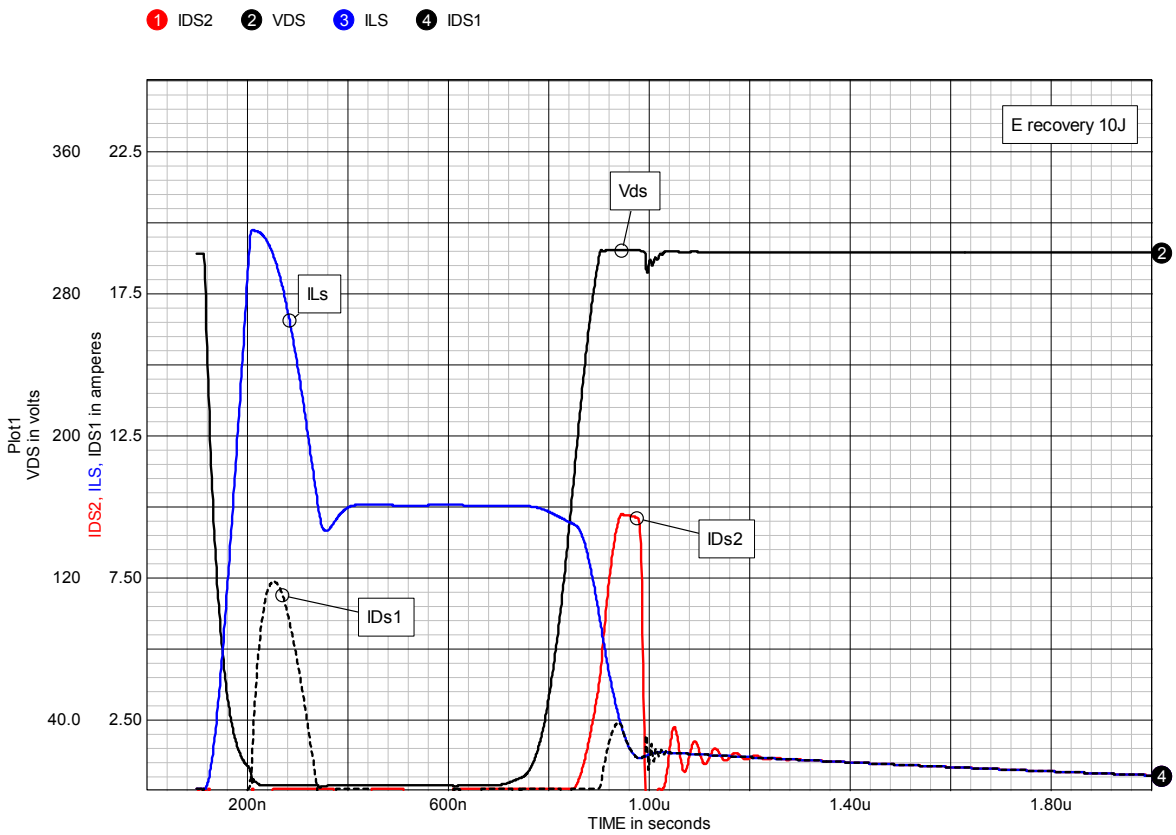


Figure 5-26, waveforms over a complete cycle

Figure 5-26 gives the waveforms for ILs, IDs1, IDs2 and Vds over one switching cycle. ILs shows us that Ls has two intervals during which it discharges stored energy. The first is associated with Q1 turn-on (t2-t3) and the second is associated with Q1 turn-off. Referring to the schematic in figure 5-25, it is clear that the only times that energy is delivered to the output (Vo) are when D1 and/or Ds2 are conducting in a forward direction. From figure 5-26 we see that the only time Ds2 is conducting is after Q1 has begun turn-off. The current pulse through Ds2 (IDs2) represents a combination of the discharge of energy from Cs1 and the second discharge of Ls. Note also in figure 5-26 that there is a long current tail on ILs. This represents the final energy discharge of Ls but the length of it presents a problem which we will address shortly.

To better understand the circuit operation we will expand the time scale on the turn-off portion of the waveforms in figure 5-26, as shown in figure 5-27, and add a few more waveforms shown in figure 5-28. Current flows during

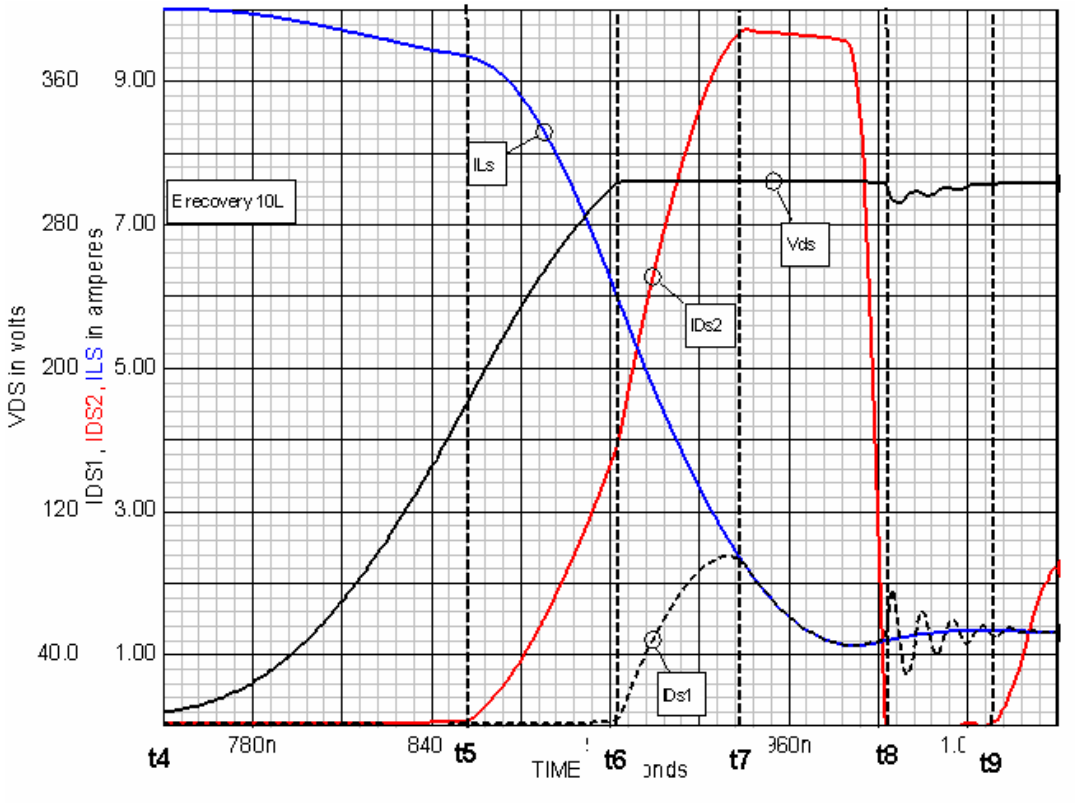


Figure 5-27, Q1 turn-off waveforms

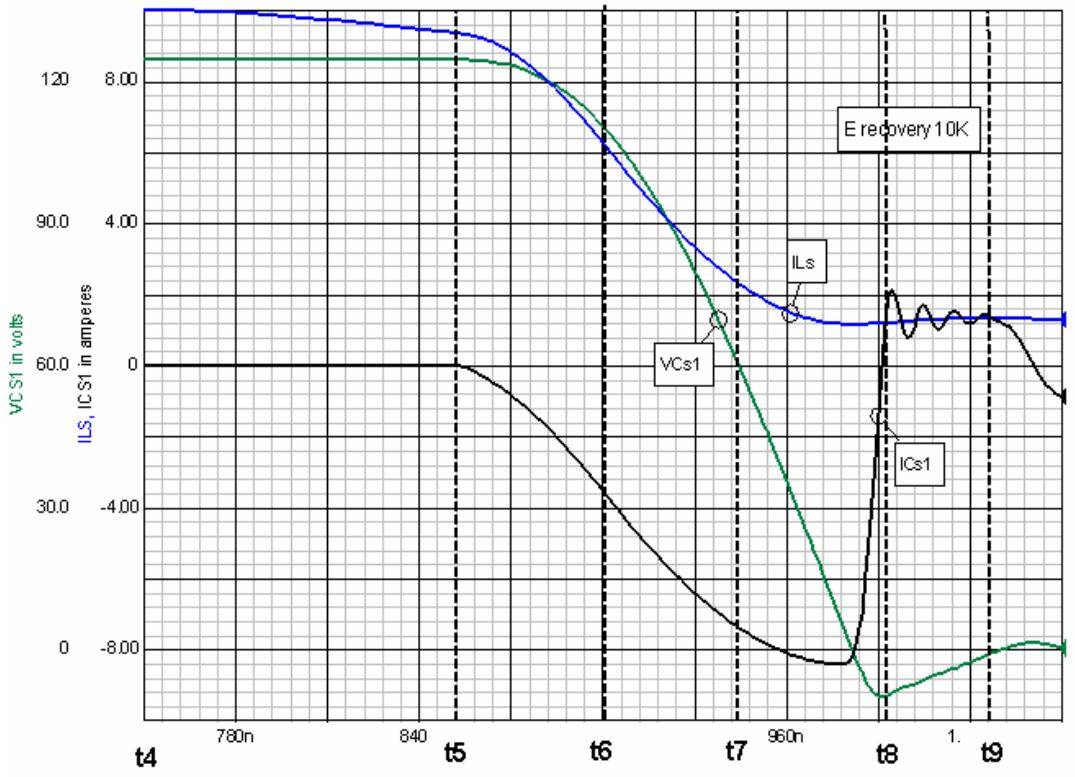


Figure 5-28, Q1 turn-off waveforms

the remaining time intervals, t4-t5, t5-t6, t6-t7, t7-t8 and t8-t9 (defined in figure 5-27). These are shown in figure 5-29 through 5-32.

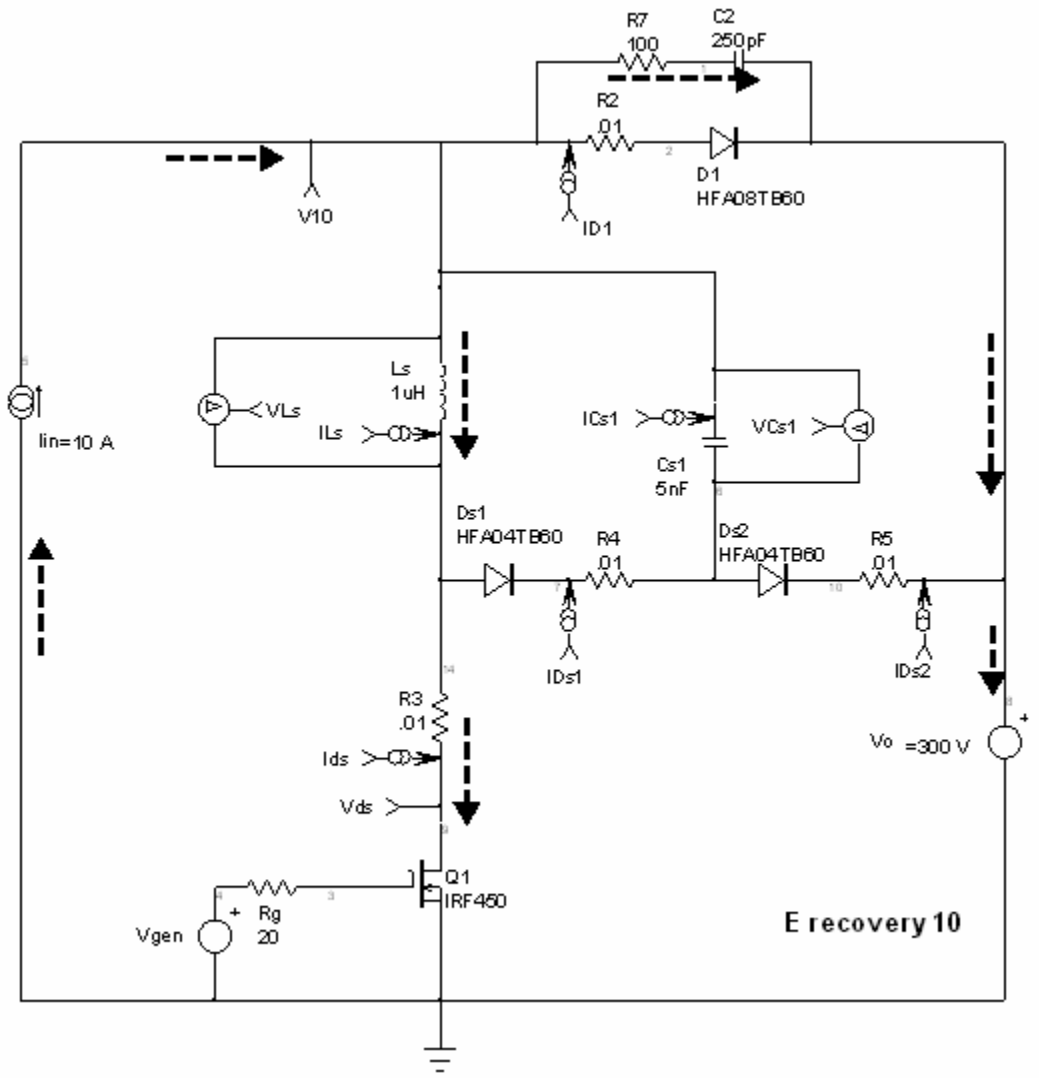


Figure 5-29, current flow during interval t4-t5.

At t=t4, Q1 begins turn-off. The current flow is shown in figure 5-29. During this interval ILs = Ids and is decreasing. Vds will be rising. The small current difference between Iin (10 A, constant) and ILs represents the current flowing through the RC-snubber into the output.

During the interval t4-t5, VCs1 = 126 V. At t=t5, Vds = 174 V. At this time the sum of Vds and VCs1 will be 300 V = Vo so that current can now be

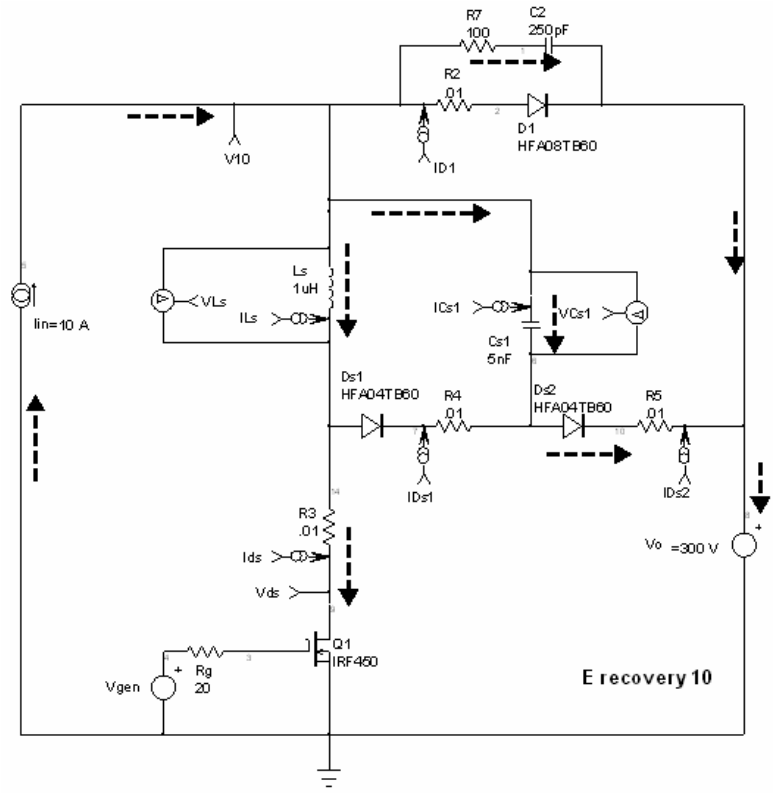


Figure 5-30, current flow during interval t5-t6.

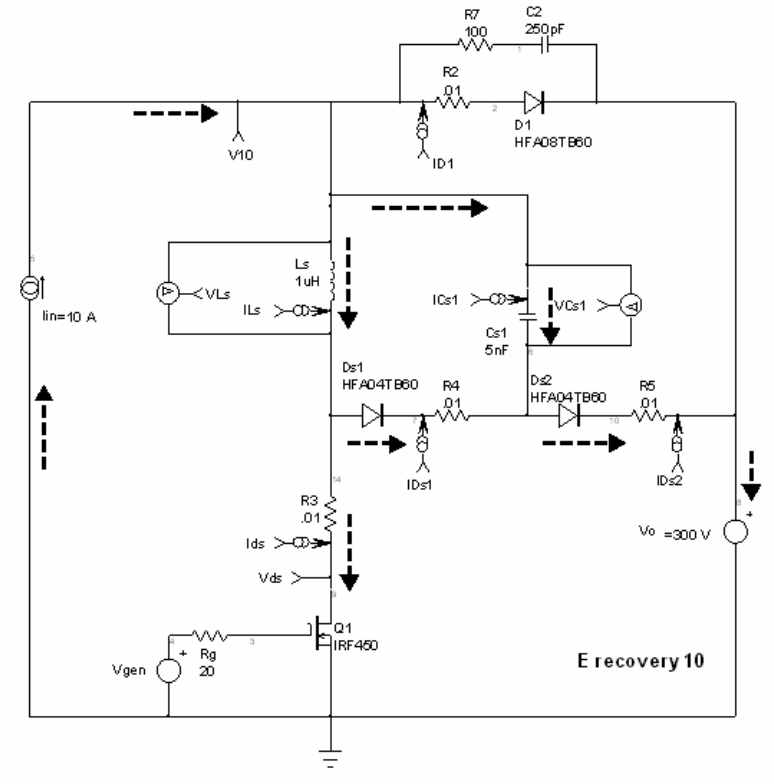


Figure 5-31, current flow during interval t6-t7.

diverted through Cs1, discharging its energy into the output through Ds2 as indicated in figure 5-30.

At t=t6, Vds reaches Vo (300 V) and is clamped to Vo by conduction through Ds1 and Ds2 as shown in figure 5-31. During the interval t6-t7 both Ls and Cs1 are discharging energy into the output.

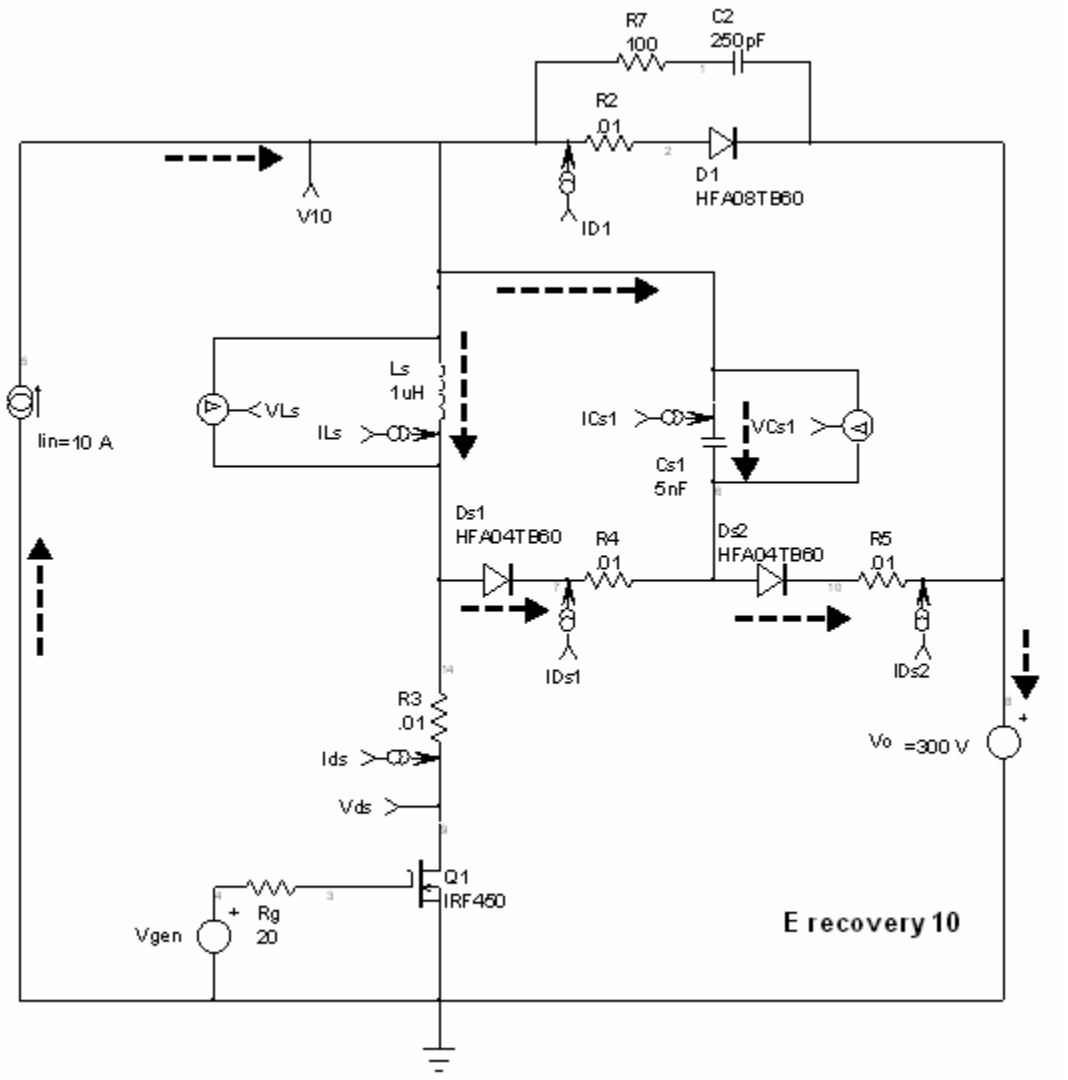


Figure 5-32, current flow during time interval t7-t8.

At t=t7, the current in Q1 (Ids) reaches zero and Q1 is now off. During the interval t7-t8, both Ls and Cs1 continue to discharge their energy into the output as indicated in figure 5-32.

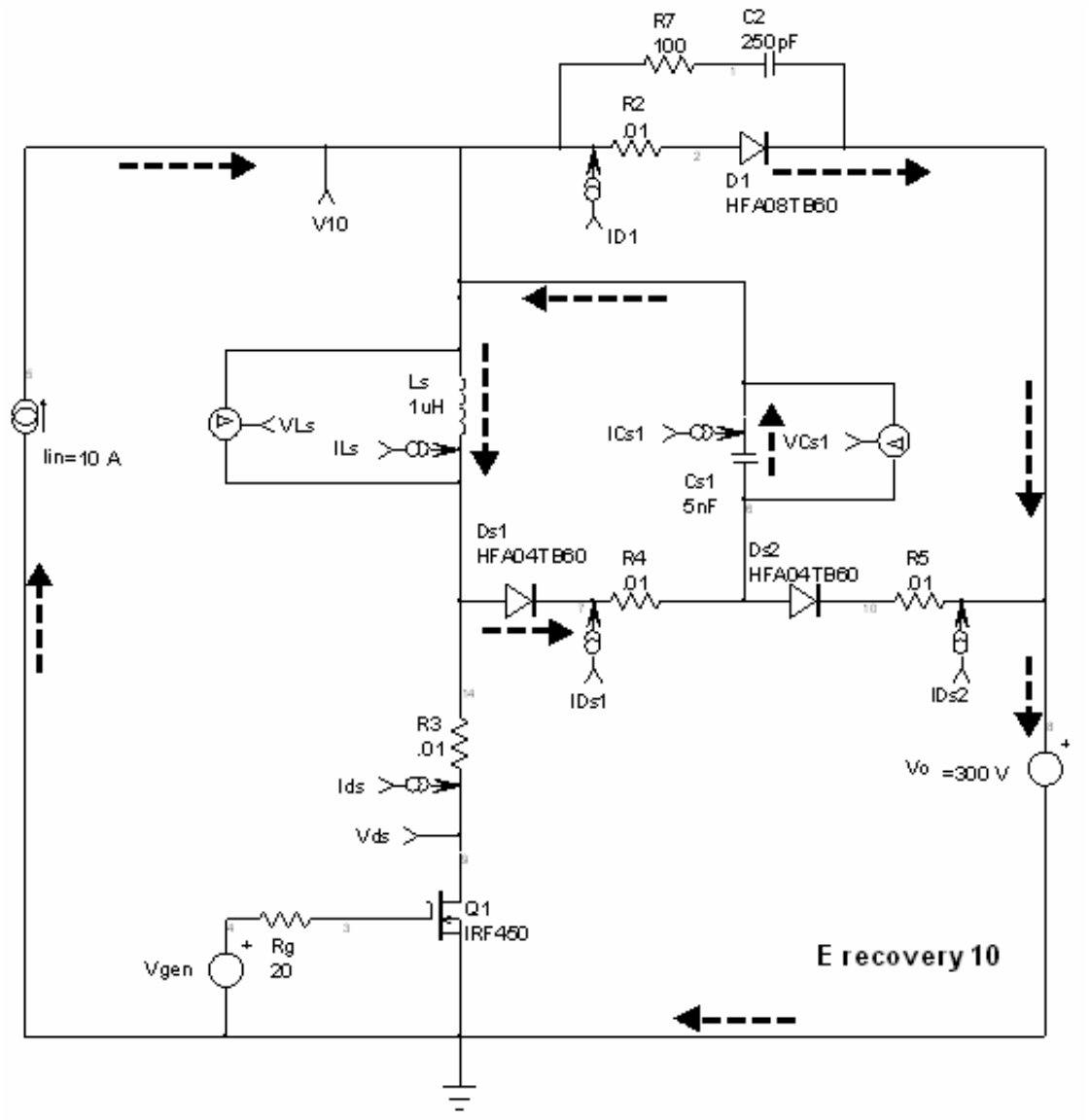


Figure 5-33, current flow during interval t8-t9.

At t=t8, Cs1 has been fully discharged and D1 begins to conduct. In fact there is some reverse charging of Cs1 which leaves some energy on that capacitor. This energy is discharged back into Ls during interval t8-t9 as indicated in figure 5-33. During this interval Ds2 is not conducting.

At t=t9, Cs1 is now fully discharged and Ds2 resumes conduction allowing Ls to discharge into the output along with Iin through D1, as indicted in figure 5-34.

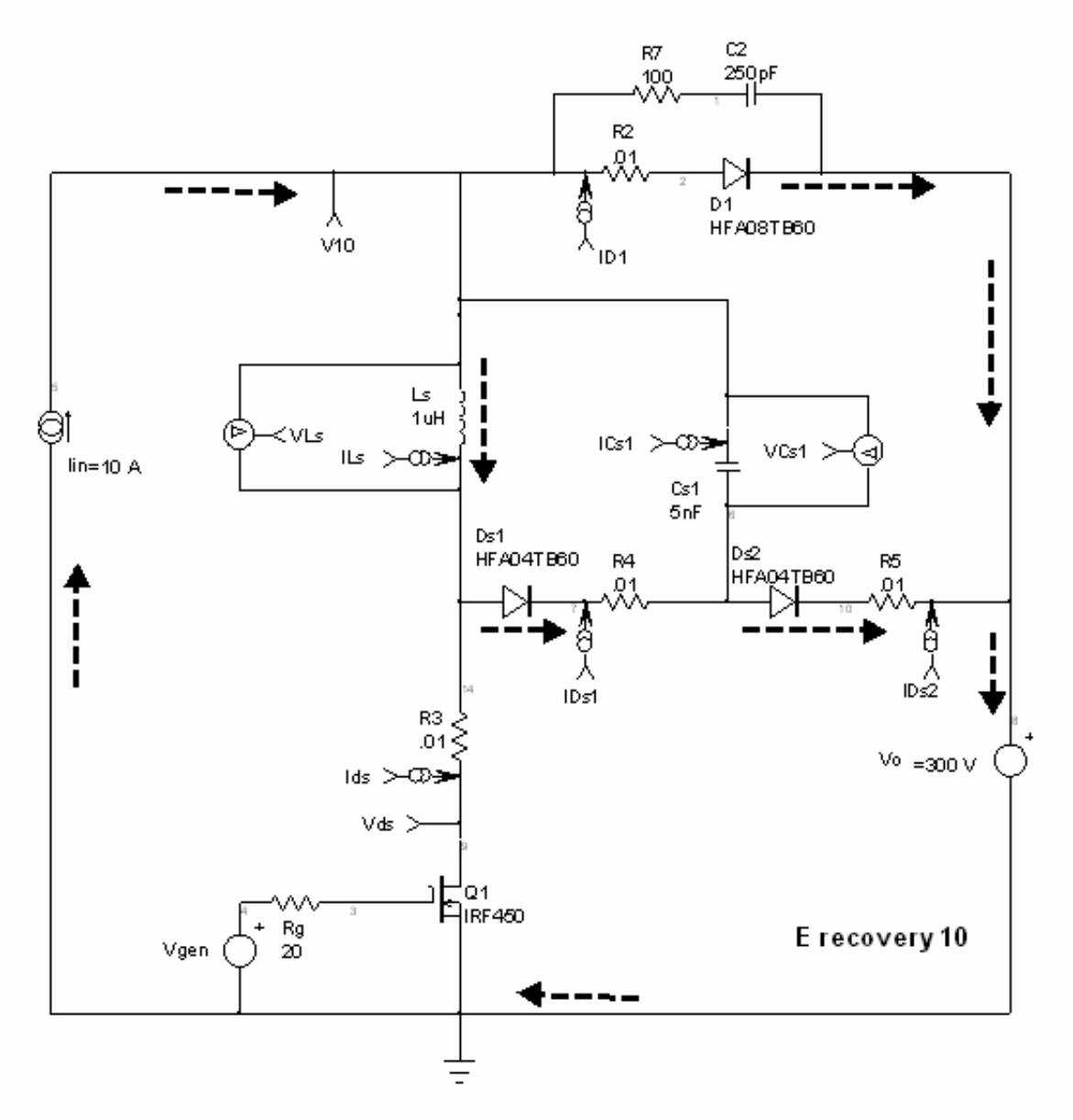


Figure 5-34, current flow during the interval t9-on.

Referring back to figure 5-26, we see that there is a long current tail associated with the discharge of Ls beginning at t=t9. The reason for the current tail is that, with D1, Ds1 and Ds2 conducting (figure 5-34), the reset voltage across Ls is only one diode drop, so it takes a long time for the energy to discharge. The amount of energy left in Ls at t=t9 will depend on the value of Cs1.

As pointed out earlier, Cs1 is used to recycle the energy in Ls. The value for Cs1 involves a tradeoff.

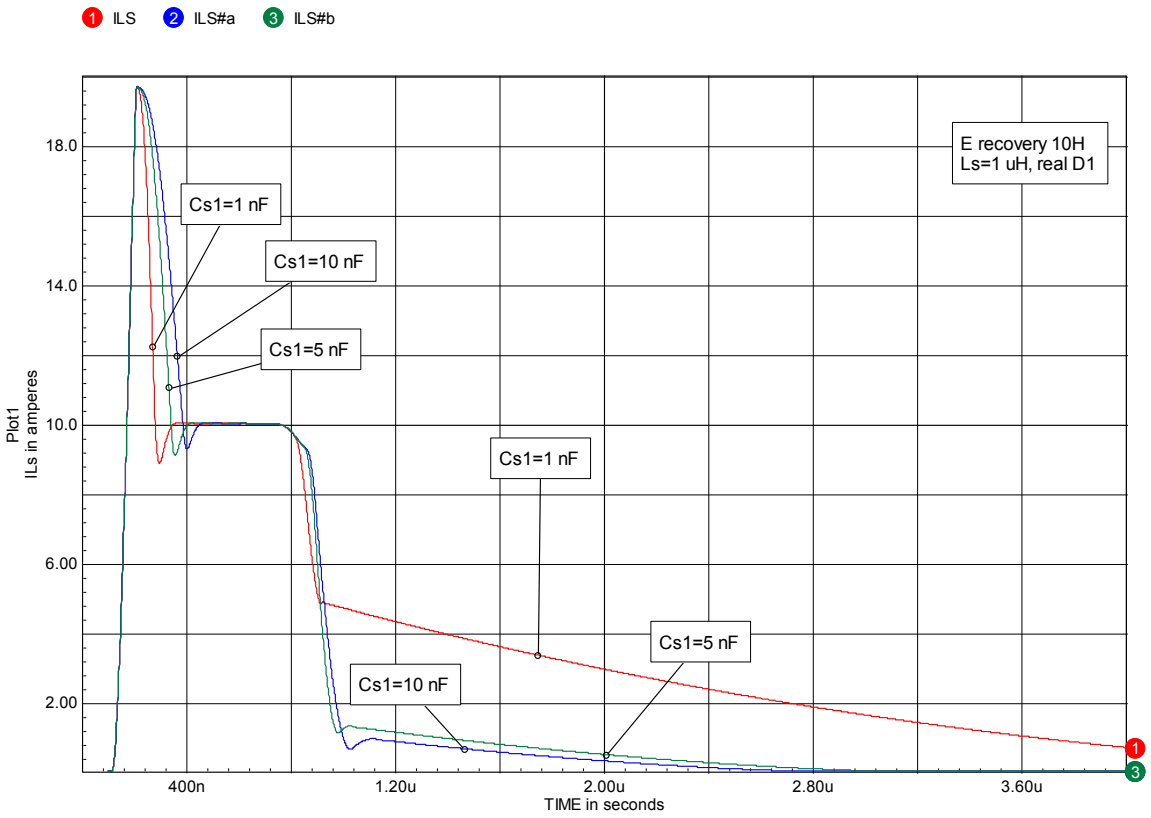


Figure 5-35, ILs for three different values of Cs1, 1, 5 and 10 nF.

Figure 5-35 shows the Ls waveforms three different values of Cs1. As the value for Cs1 is increased the current in Ls (ILs) is altered in two ways: first, the initial discharge time for Ls after Q1 turn-on is prolonged and second, the length of current tail after Q1 turn-off is significantly reduced. The first effect is undesirable in that it increases the minimum acceptable switch on-time but the second is very desirable in that it reduces the minimum acceptable switch off-time. However, as can be seen from the ILs waveforms, the point of vanishing returns sets in quickly. Going form 1 to 5 nF makes a useful difference but doubling the capacitance from 5 to 10 nF doesn't make a lot of difference, there is still a current tail. The value for Cs1 will be determined by the minimum on and off times for Q1 and must be balanced to satisfy both if possible.

There is another way to reduce the current tail. You can add a small series resistance in series with Ds2 (R5 in figure 5-15). The effect of varying the value of R5 on the ILs current tail is shown in figure 5-36.

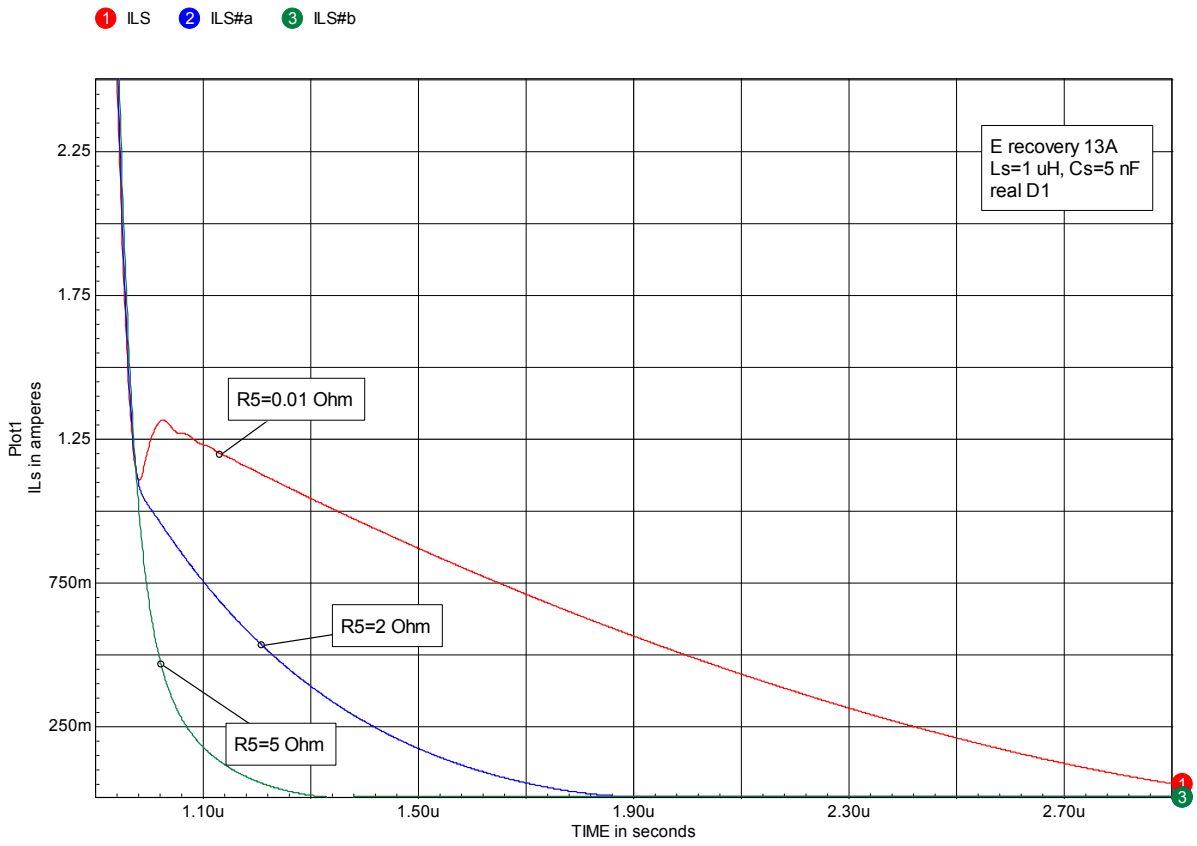


Figure 5-36, ILs current tail waveforms for different values of R5.

Adding a bit of resistance in series with Ds2 yields an immediate reduction in the ILs current tail. In this example, for R5=5 Ohm, there will be an additional 21 µJ of energy loss at each turn-off transition but that should be acceptable. There is however, another downside to adding R5. The absence of a turn-off voltage spike on Vds in figure 5-18 is due to the clamping of Q1 drain to Vo through Ds1 and Ds2. When we add R5 in series there will now be a 49 V spike on Vds at turn-off, as shown in figure 5-37. If R5 were 2 Ohm, then the voltage spike would be about 20 V.

The trade-off in selecting values for Cs1 and R5 requires that the minimum on-time be balanced against the minimum off-time in the particular application.

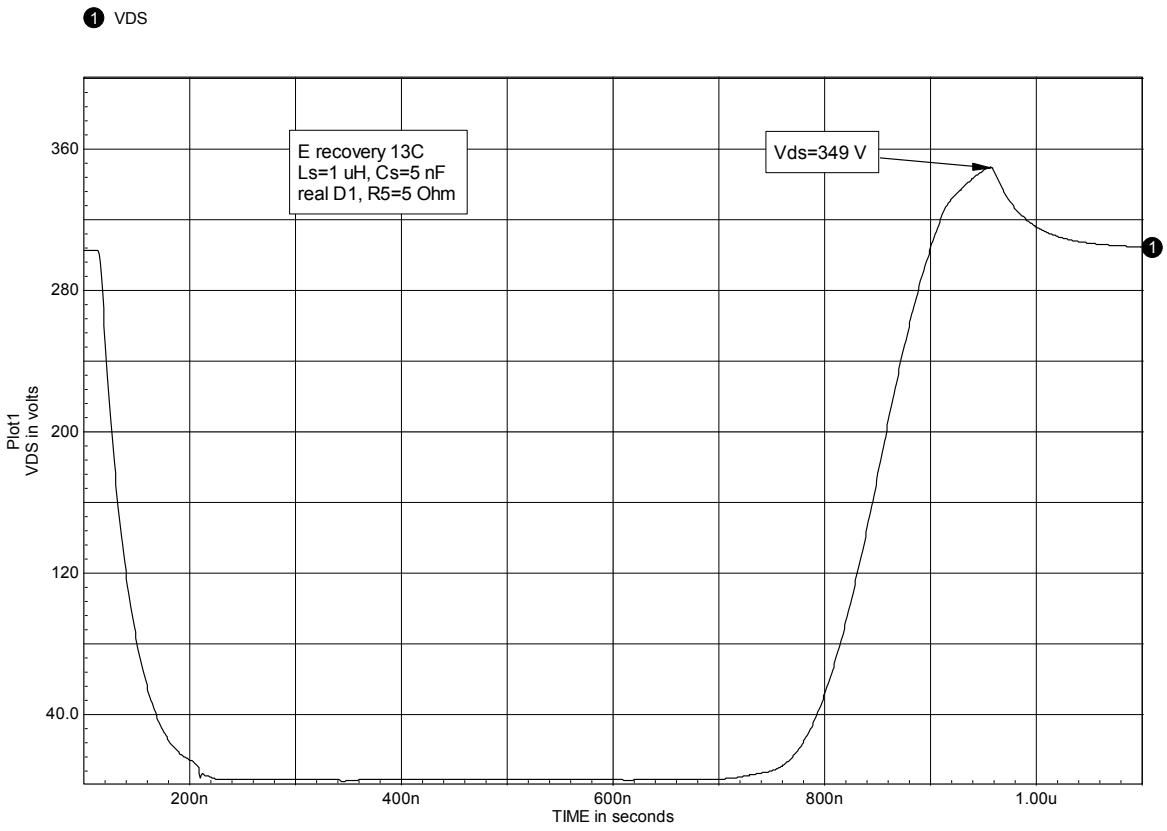


Figure 5-37, voltage spike at Q1 turn-off due to the addition of R5.

There is one further problem associated with this snubber. When the load current is reduced there can be ringing in Q1 Vds as shown in figure 5-38, where Iin has been reduced to 2 A. Ds1 and Ds2 still provide an upper clamp voltage (Vo) but drop out of conduction during the ringing. This is due to Ls resonating with Coss of Q1. Unfortunately, R5 will not provide damping for this ringing. If it is necessary to suppress this ringing, a shunt RC damping network across Q1 is probably the best option.

This is the second example we have seen of a spurious ringing waveform introduced by the addition of an inductive turn-on energy recovery snubber to the basic converter. Because most energy recovery circuits are deliberately designed to dissipate as little energy as possible, usually little damping is present. This leads to the snubber inductor ringing with parasitic circuit capacitances and of

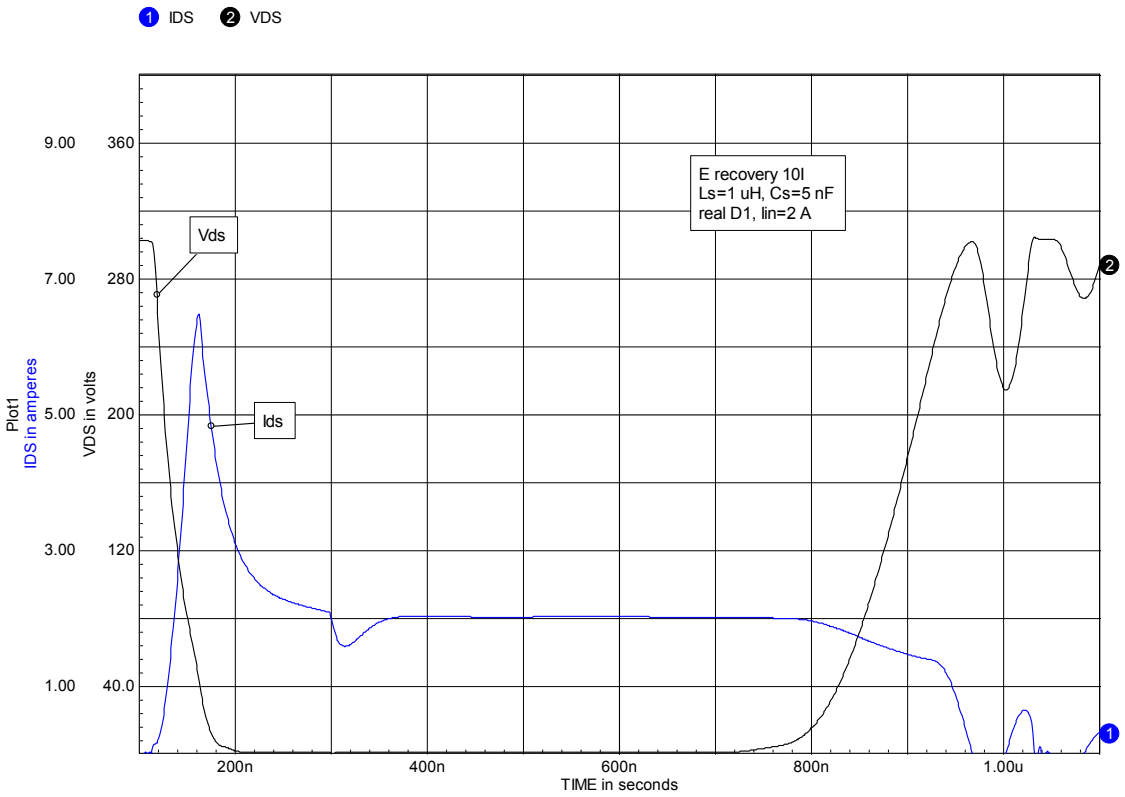


Figure 5-38, Vds ringing at Q1 turn-off at light load.

course parasitic inductances in the circuit can also create additional ringing.

> *This problem is quite common in energy recovery snubber schemes and the designer needs to be wary.*

Turn-on snubber example 2

Another popular energy recovery snubber is shown in figure 5-39.

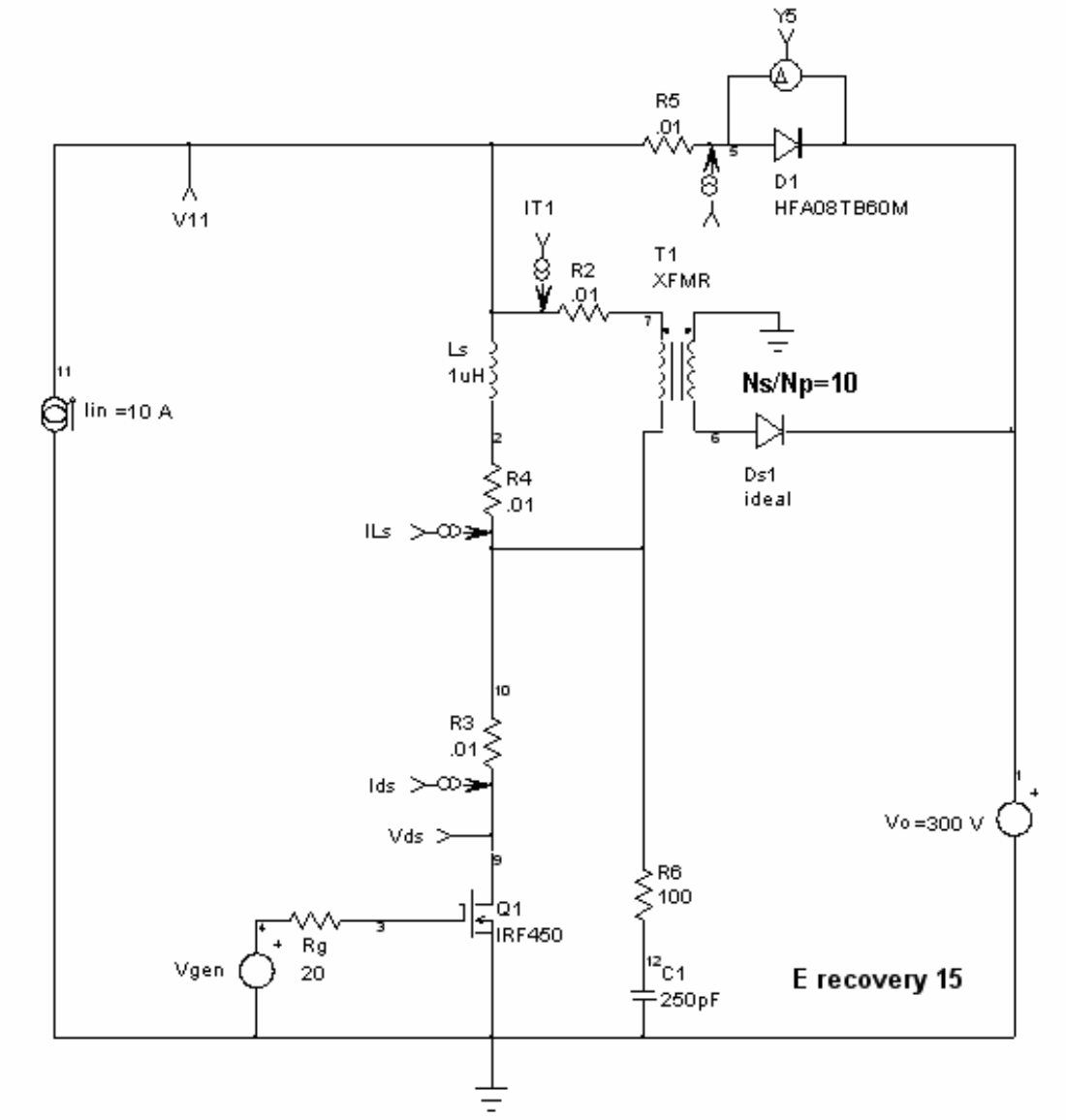


Figure 5-39, energy recovery turn-on snubber.

In an actual application, Ls and T1 would be combined into a single two-winding inductor where Ls is the magnetizing inductance but to explain the circuit behavior, I have separated Ls from the transformer windings. R2 and R4 are for current metering in the model. In this example, for T1, Ns/Np=10. Turns ratio selection will be discussed shortly. Note that an RC damping network (R6-C1) has been included.

Figure 5-40 shows the Ids and Vds waveforms for this snubber example.

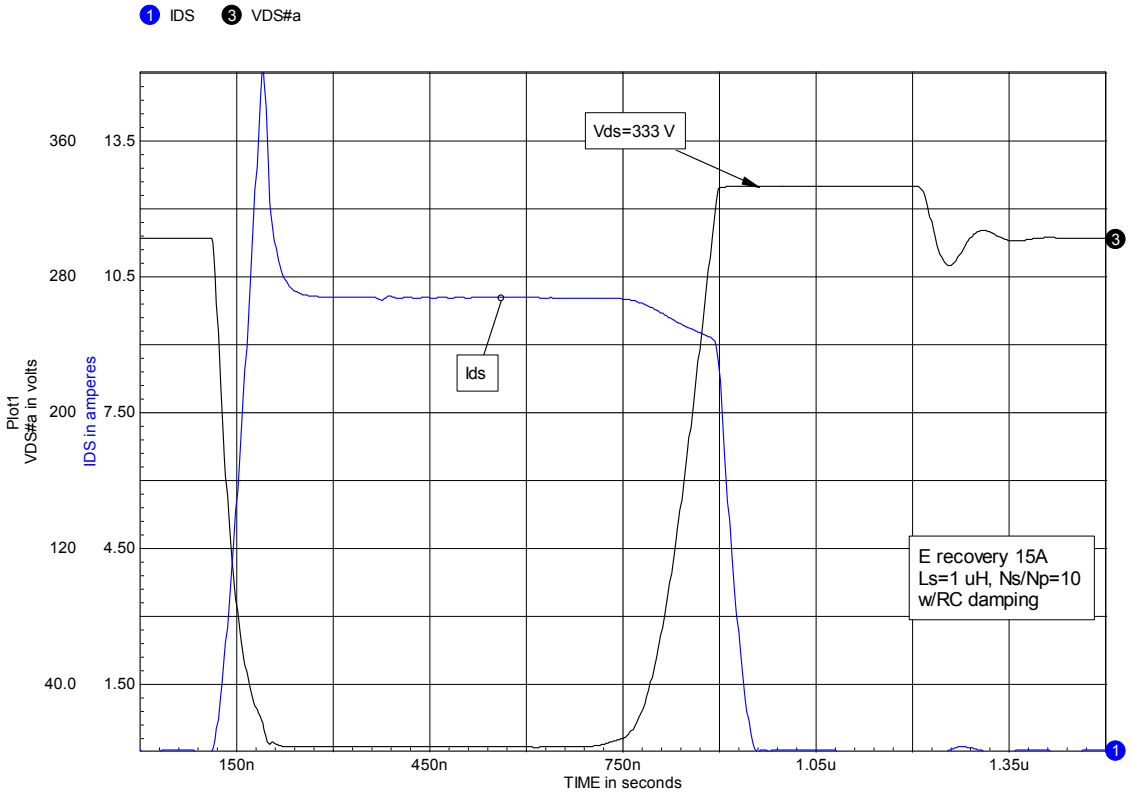


Figure 5-40, Ids and Vds waveforms.

The turn-on snubbing action is exactly as we have seen earlier for Ls=1 uH. At turn-off Ls discharges through T1 and Ds1 into Vo which forms a clamp circuit. In this example Ns/Np=10, so the clamp voltage on the primary of T1 is 30 V during the discharge interval of Ls. This adds a 30 V spike to Vds at turn-off. This spike could be made smaller by increasing Ns/Np but in exchange, the discharge time would increase. Ultimately the allowable discharge time is limited by the minimum off-time of Q1. There is another practical limitation on Ns/Np. As the value is increased it becomes more difficult to obtain good coupling between windings. The result is some residual leakage inductance on the primary which leads to another voltage spike on Vds at turn-off. Figure 5-41 shows the effect of 50 nH of leakage inductance.

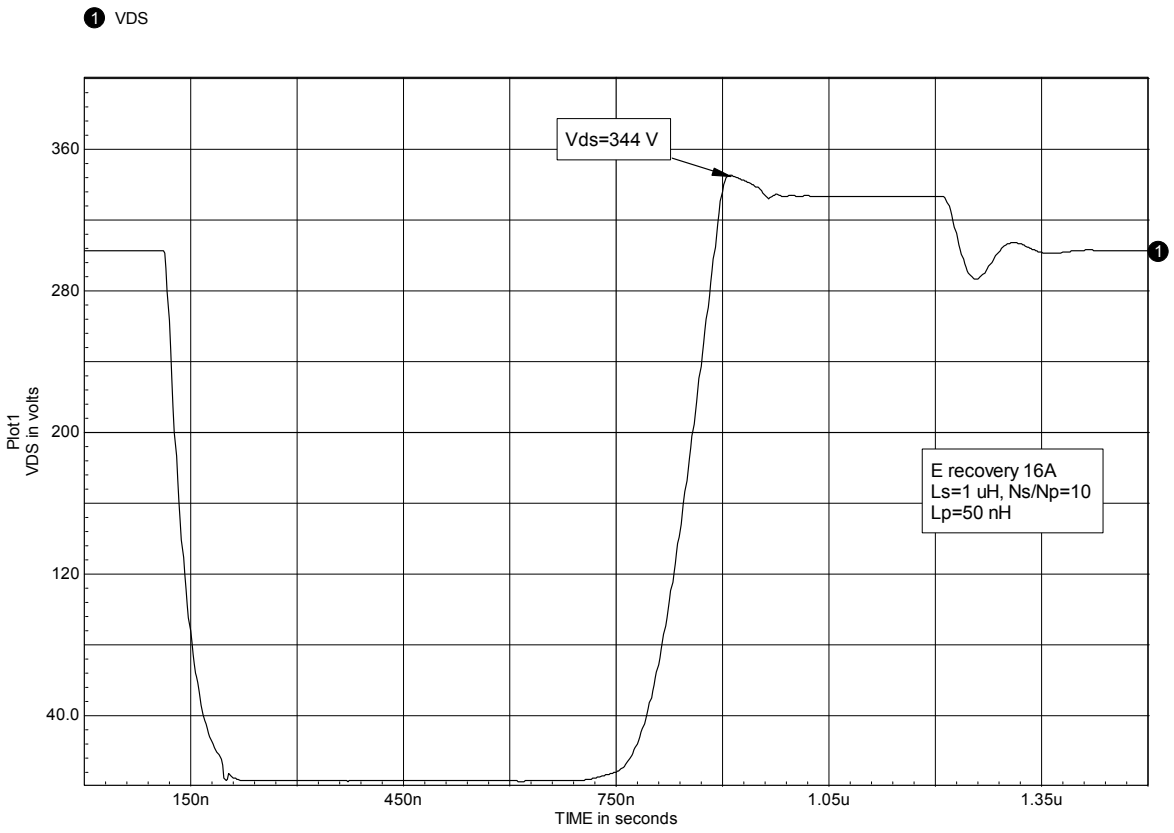


Figure 5-41, Vds spike with 50 nH of leakage inductance.

In this example, the amplitude of the additional voltage spike is reduced by the presence of the RC damping network.

At the end of the discharge interval of Ls, some ringing is present due to the resonance of Ls and Coss of Q1. RC damping network is present to suppress both this ringing and the spike associated with leakage inductance. Without damping this ringing would be much larger than shown here. If desired this ringing could be reduced further with more aggressive damping.

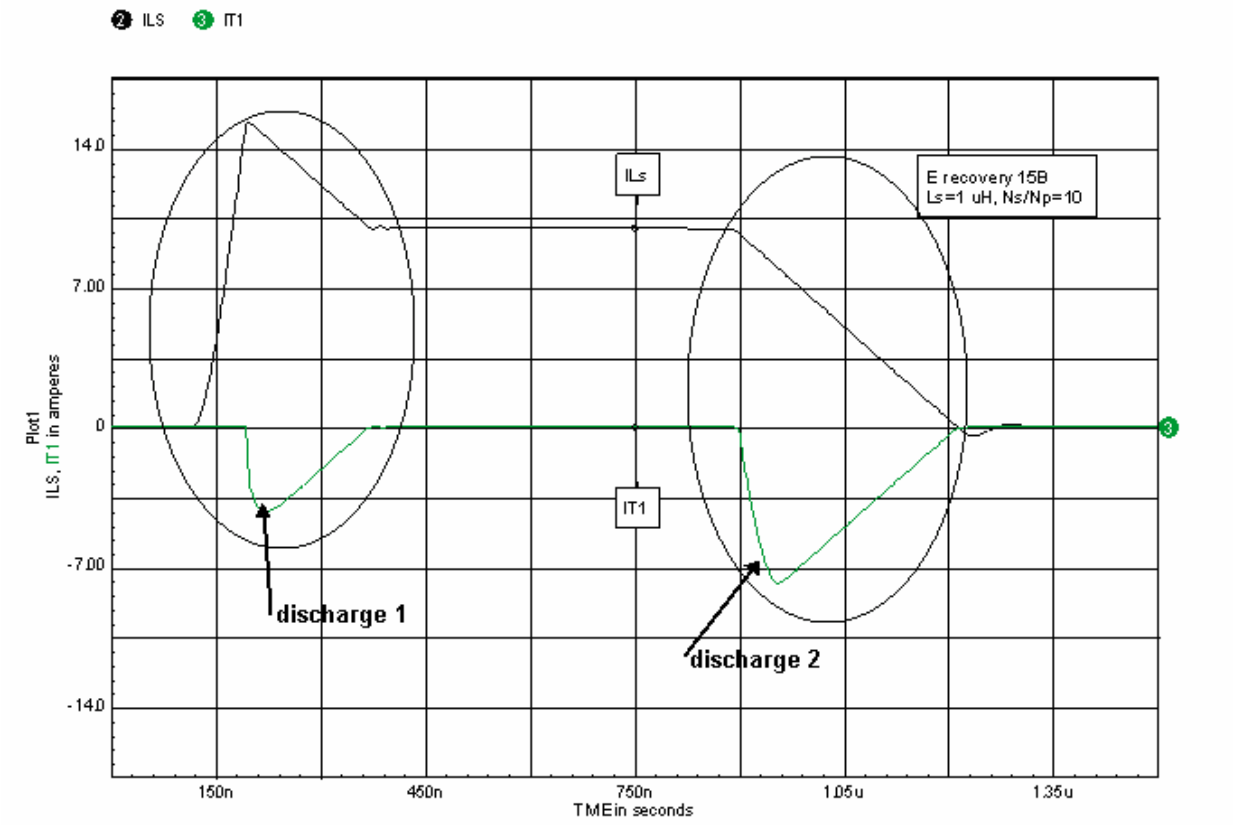


Figure 5-42, current waveforms in Ls (ILs) and T1 primary (IT1).

Figure 5-42 shows the current waveforms for ILs and IT1 (on the primary side). There are two energy discharge intervals for Ls: the first interval commences when D1 reverse recovery enters it's second phase (i.e. begins to support reverse voltage) and continues until ILs equals Iin, 10 A in this example. The second interval commences at Q1 turn-off and continues until all the energy in Ls is discharged. During both intervals, energy is dumped into Vo via the secondary winding of T1 and Ds1.

While this snubber is simple and effective it does have one drawback. As shown in figure 5-43, during the first discharge interval of Ls, there is an additional reverse voltage spike (VD1) across D1. In addition there will be some ringing between Ls and the capacitance of D1. It may be necessary to have a second RC damping network across D1.

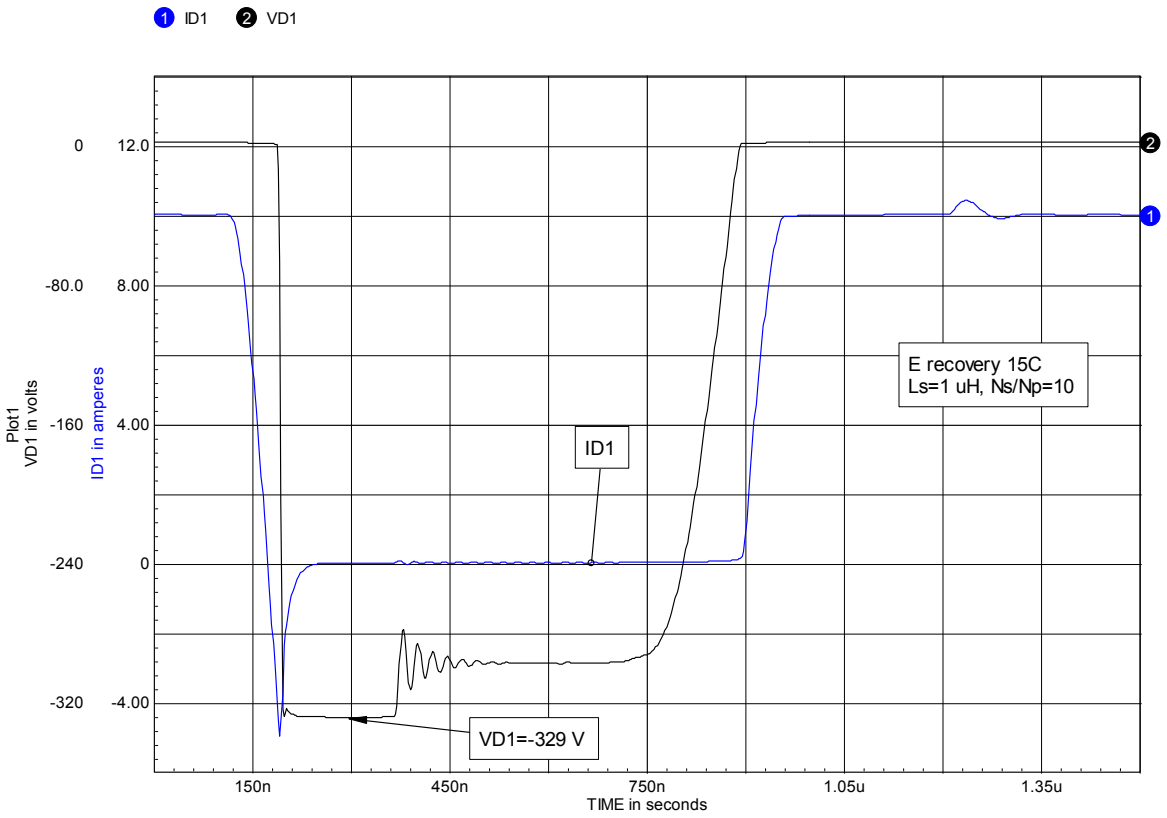


Figure 5-43, voltage (VD1) and current (ID1) waveforms for D1.

This is yet another example of the parasitic ringing which can appear in energy recovery snubbers.

In this snubber circuit Ls was chosen by the same rules as for the dissipative turn-on snubber and its turn-on action is the same. The turns ratio is determined by trading reset time versus the voltage spike amplitude on Vds at Q1 turn-off.

Combination energy recovery snubbers

There are many energy recovery snubbers which can provide snubbing at both turn-on and turn-off. However, we have to be a bit careful. In general we cannot simply combine the turn-on and turn-off examples given above. When we try that we often see interaction between the snubbers which impairs the snubbing action[291] and/or introduces large voltage and/or current ringing.

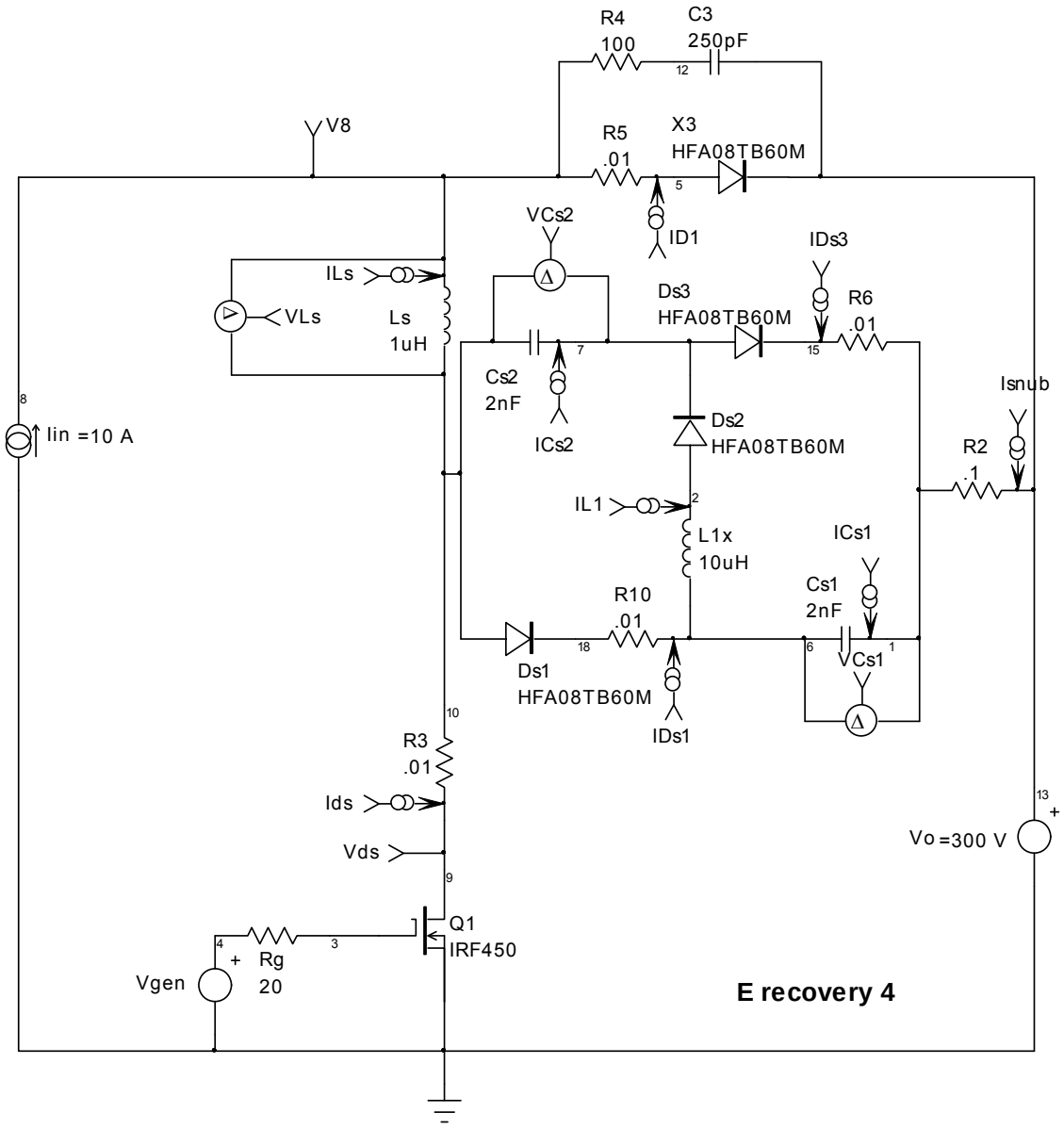


Figure 5-44, adding an inductor (Ls) to the snubber in figure 5-1.

By way of an example of what not to do, a circuit arrangement which will have severe ringing is shown in figure 5-44 where a turn-on snubber inductor (Ls) has been added to the turn-off snubber (originally shown in figure 5-1) to reduce the effect of using a real diode for D1, on Q1 turn-on current waveform.

The resulting Q1 waveforms for Ids and Vds are shown in figure 5-45.

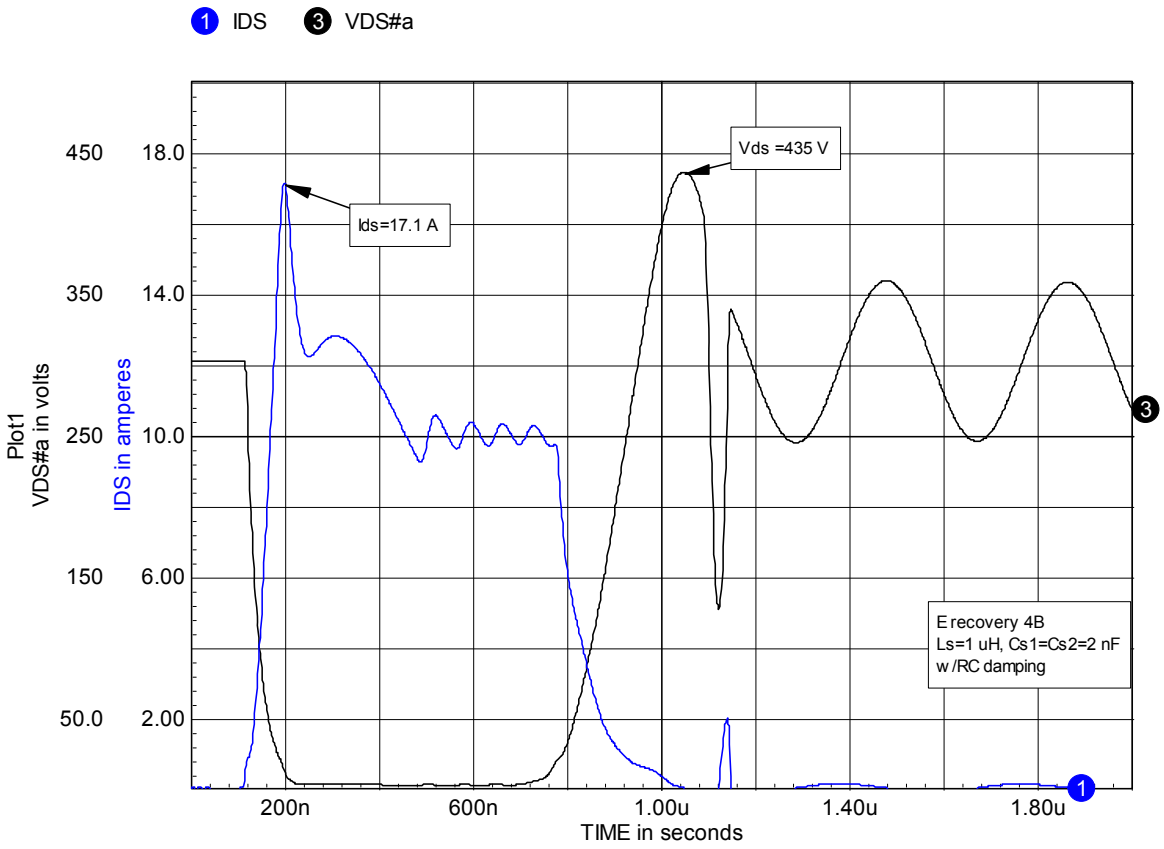


Figure 5-45, waveforms for Ids and Vds associated with figure 5-29.

While there is obviously both turn-on and turn-off snubbing, there is also a large voltage overshoot at turn-off followed by large amplitude ringing, which is only slightly damped. There are also other ringing in the circuit. This is not a satisfactory snubber. We need to do better!

Combination snubber example 1

A very simple fix for the circuit in figure 5-44, would be to add a resistor-diode network across Ls, in other words combine the energy recovery turn-off snubber with a standard dissipative turn-on snubber. This is shown in figure 5-46,where we have added Rs and Ds4 to the circuit in figure 5-44.

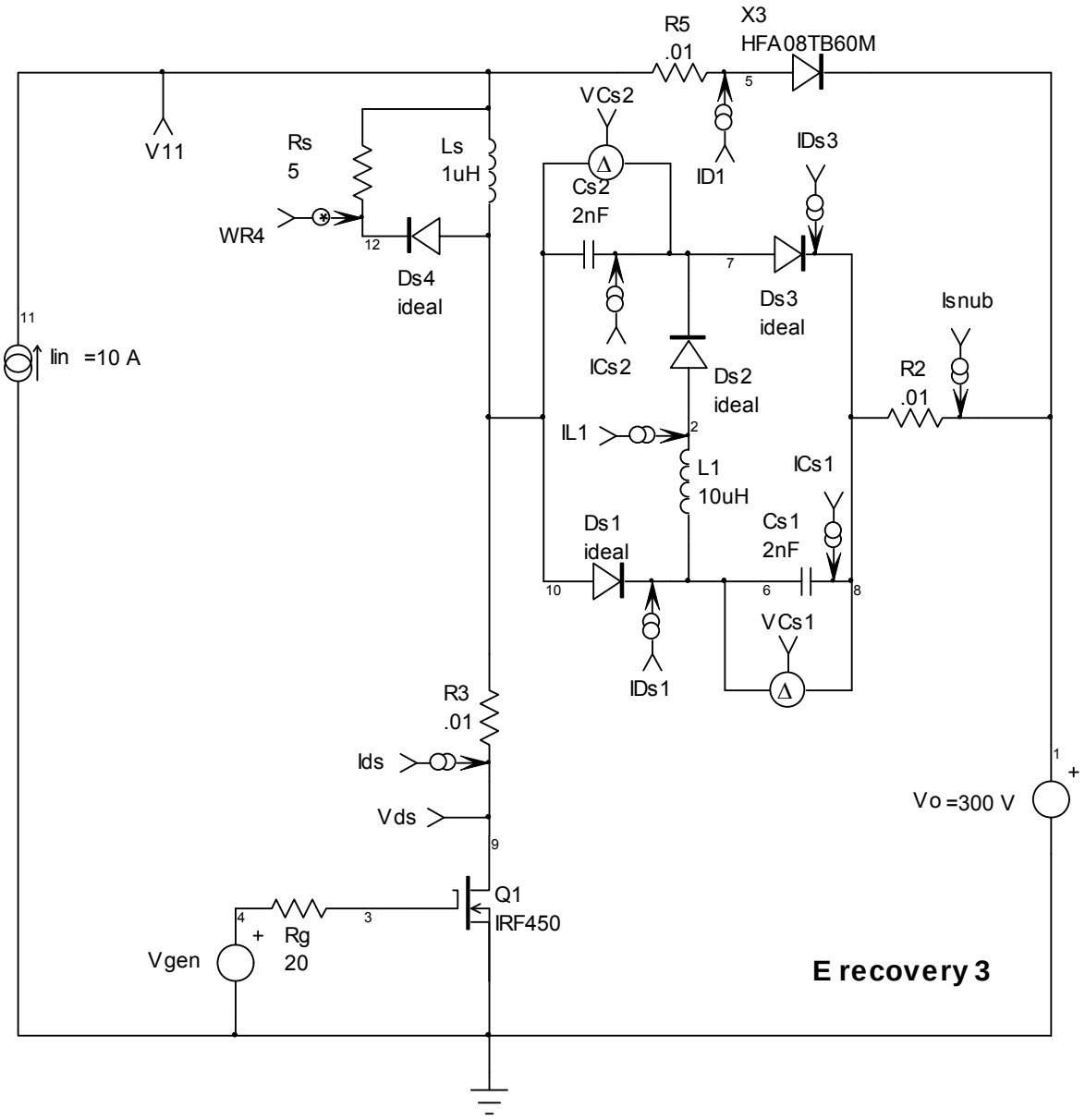


Figure 5-46, an energy recovery turn-off snubber combined with a dissipative turn-on snubber.

The new waveforms for Q1 are shown in figure 5-47. Without any snubber Utotal=424 μJ (see figure 4-33) all of which is in Q1. Using the combination dissipative snubber (see figure 4-42) the switch loss was reduced to 115 μJ but there was another 243 μJ of loss in the snubber resistors so the total circuit loss was 358 μJ.

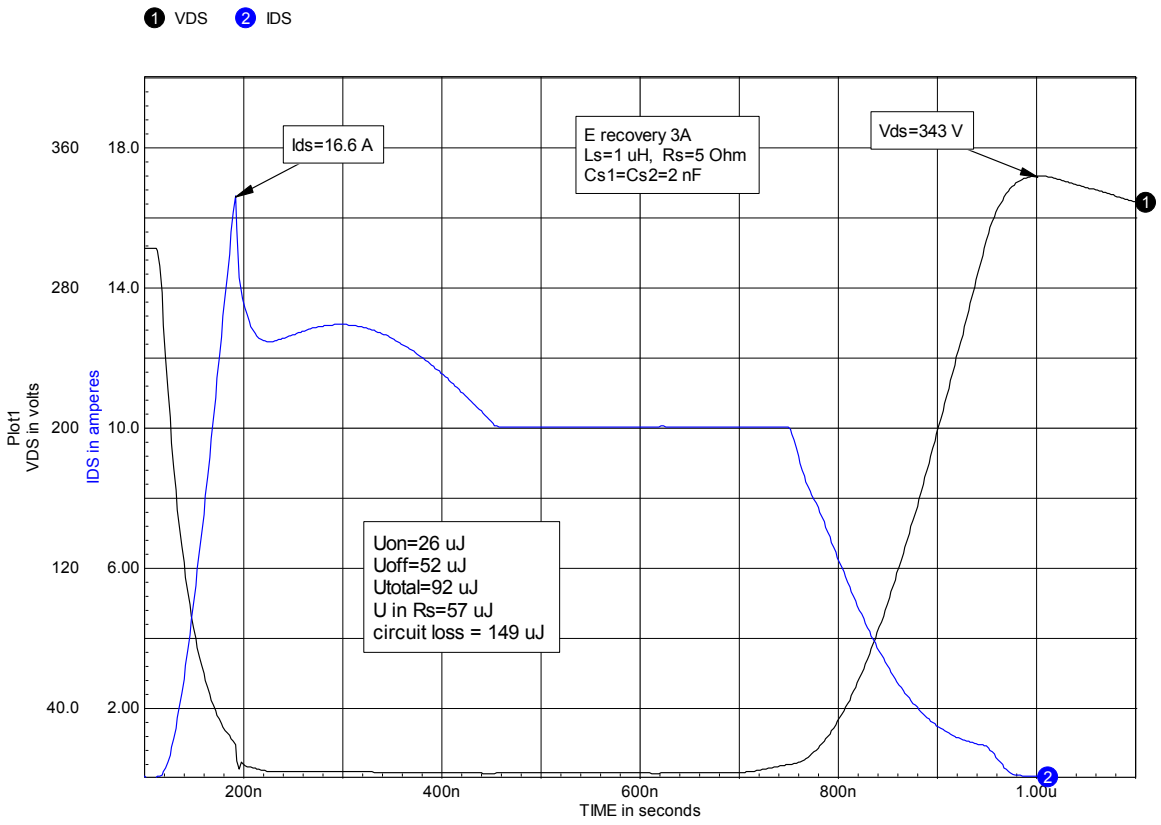


Figure 5-47, Q1 waveforms for Ids and Vds with Rs and Ds4 added.

By combining the dissipative turn-on snubber with the energy recovery turn-off snubber we have saved most of the resistive energy loss so the total circuit loss is now down to 149 µJ, with 57 µJ in Rs and rest in Q1. Note that in figure 4-42 Cs=3.5 nF but in figure 5-46, Cs=4 nF. That is why Utotal is slightly lower in figure 5-47.

Combination snubber example 2

For reference in the following, figure 5-48 shows a dissipative turn-on/off (or combination) snubber which was discussed in chapter 4. In this example, the snubber is divided into two sections: the portion which provides the turn-on and turn-off snubbing action and the resistor which dissipates the energy stored in Ls and Cs1 at switch turn-off.

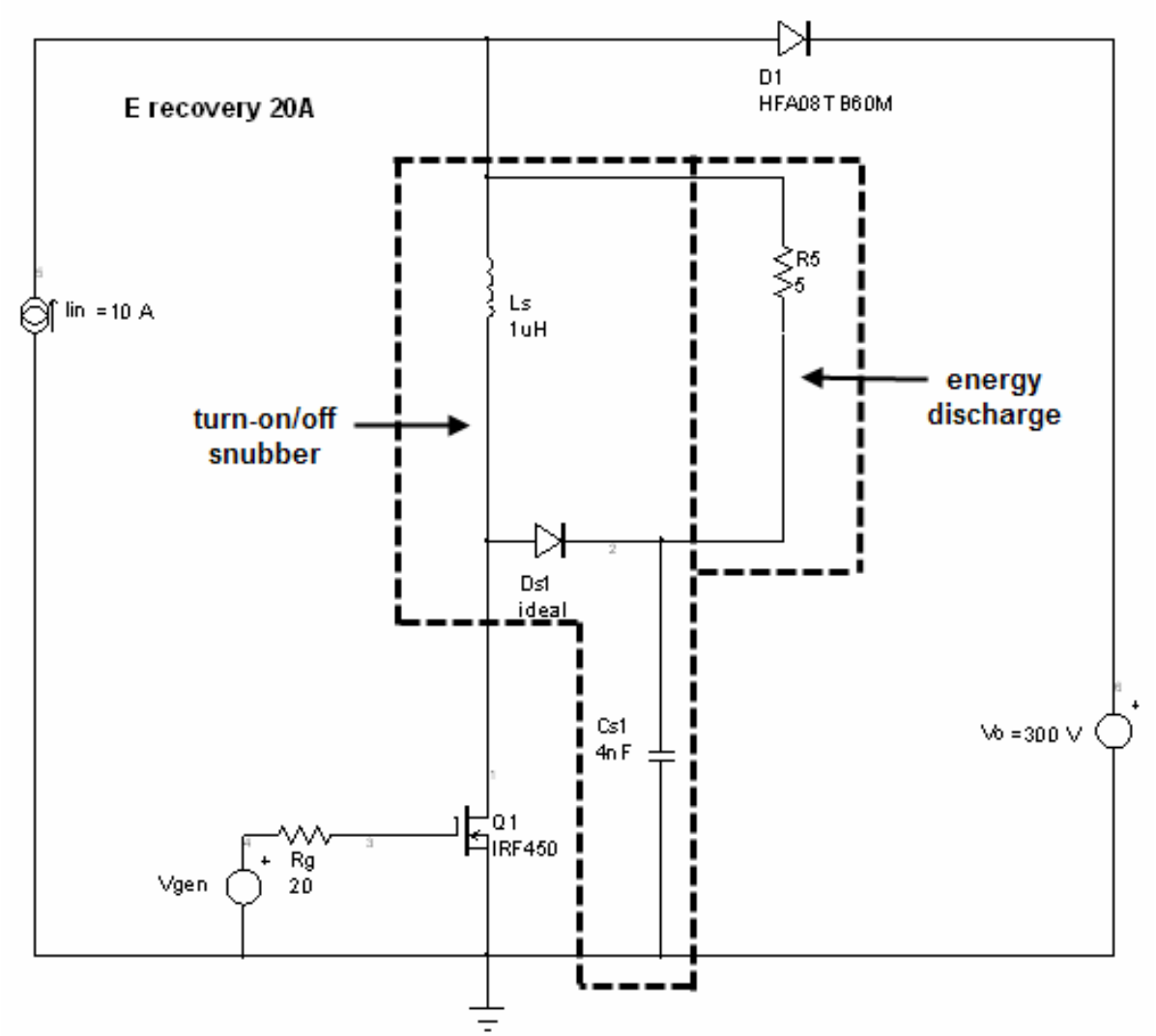


Figure 5-48, dissipative turn-on/off snubber circuit.

At high power levels the energy dissipation may be quite large and it may be desirable to recover this energy and apply it to some useful purpose.

To save this energy we can replace dissipative resistor in figure 5-48, with an energy recovery network as shown in figure 5-49.

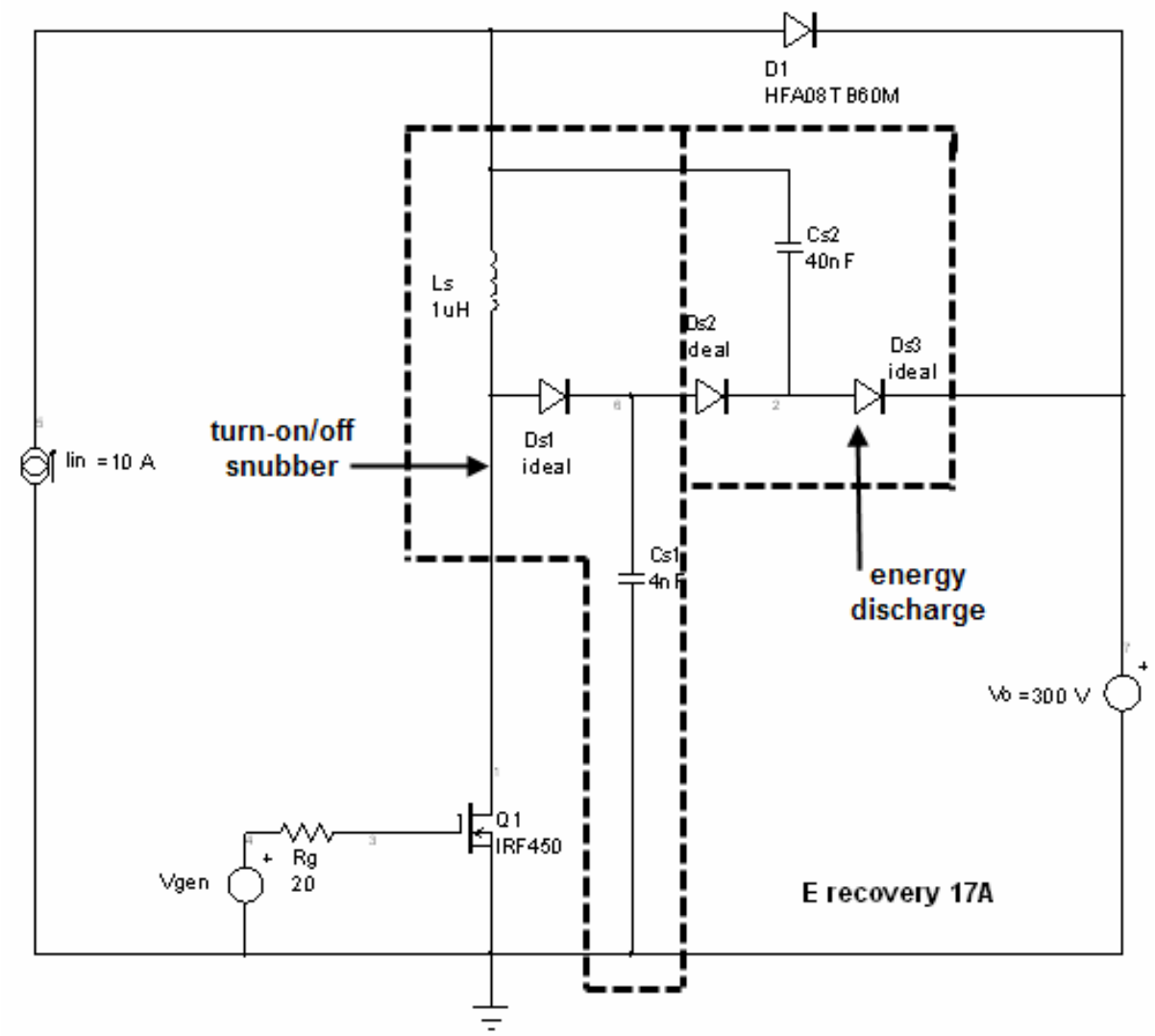


Figure 5-49, combination snubber example 2.

Ls is the turn-on snubber inductor and Cs1 is the turn-off snubber capacitor. Ds2, Ds3 and Cs2 form an energy recovery network which has replaced the dissipative resistor in figure 5-48. In this example, the recovered energy is delivered to the output (Vo). Cs2 is an energy storage capacitor used to recirculate the reactive energy and deliver it to the output. Cs2 has to store enough energy to completely reset Ls at turn-off. Cs2 is usually sized to be 10 x Cs1 although smaller values may be adequate depending on the application.

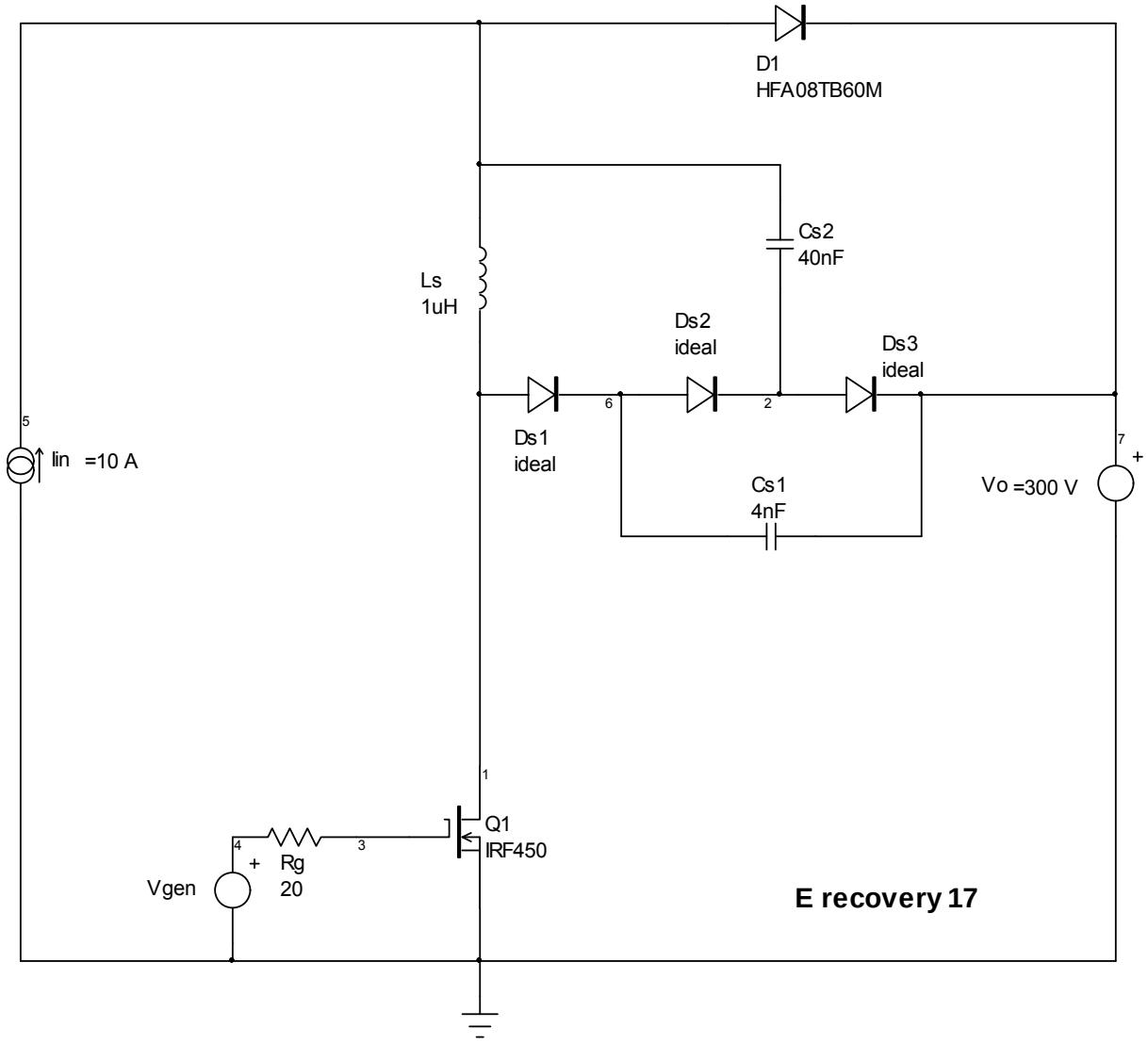


Figure 5-50, alternate version for example 2.

A common variation of this snubber is shown in figure 5-50. This variation behaves exactly the same as that in figure 5-49. All we've done is to move one terminal of Cs1 from ground to Vo which has no effect on the dynamic behavior of the circuit.

For the rest of this section we will work with the variation in figure 5-49. Typical Q1 waveforms associated with figure 5-49 are shown in figure 5-51.

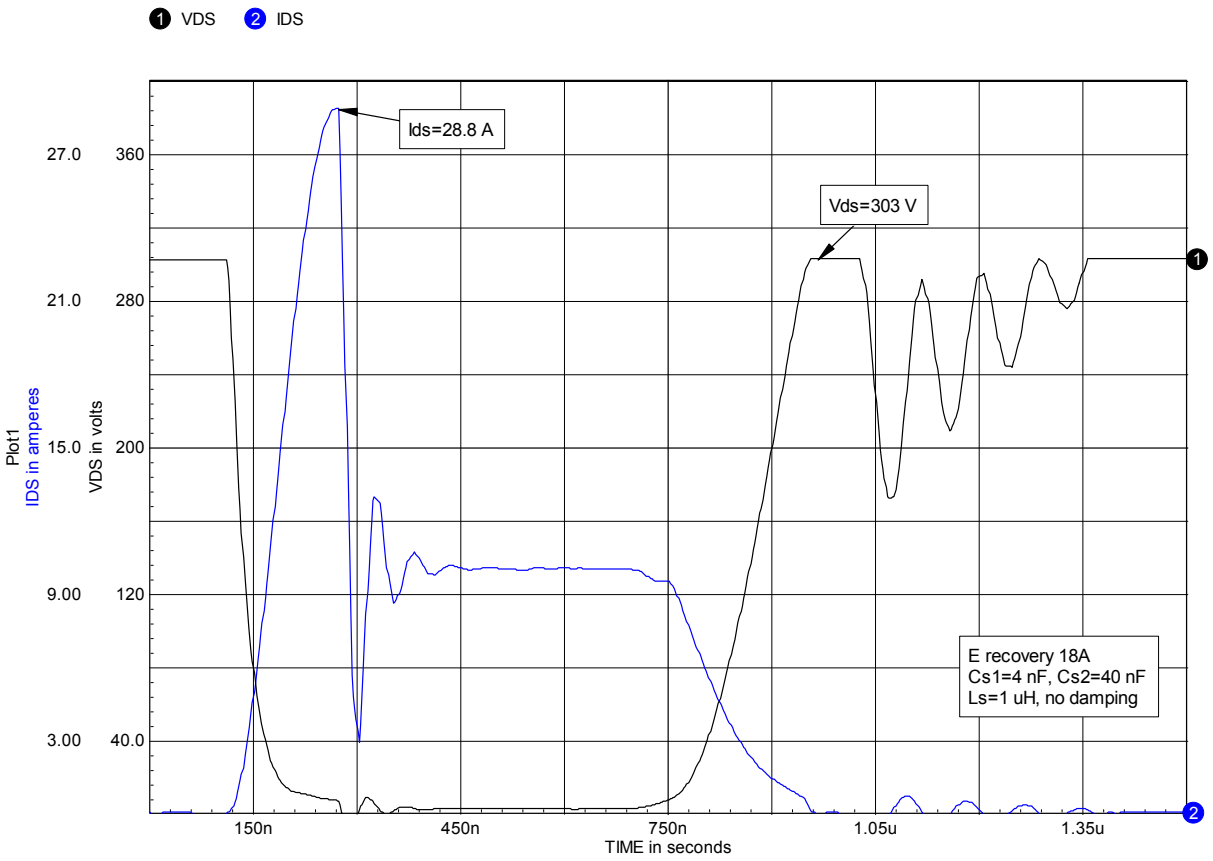


Figure 5-51, typical Q1 waveforms in the circuit in figure 5-49.

While the snubbing action is very good, these are still ugly waveforms! The ringing is severe because there is no damping in the circuit. Before proceeding with the discussion we will have to add some damping as shown in figure 5-52 (Rs1, Rs2 and Cs3).

Q1 waveforms with the added damping are shown in figure 5-53. Heavier damping could have been used but that would lead to higher losses. There is a trade-off between the degree of damping and the acceptable loss.

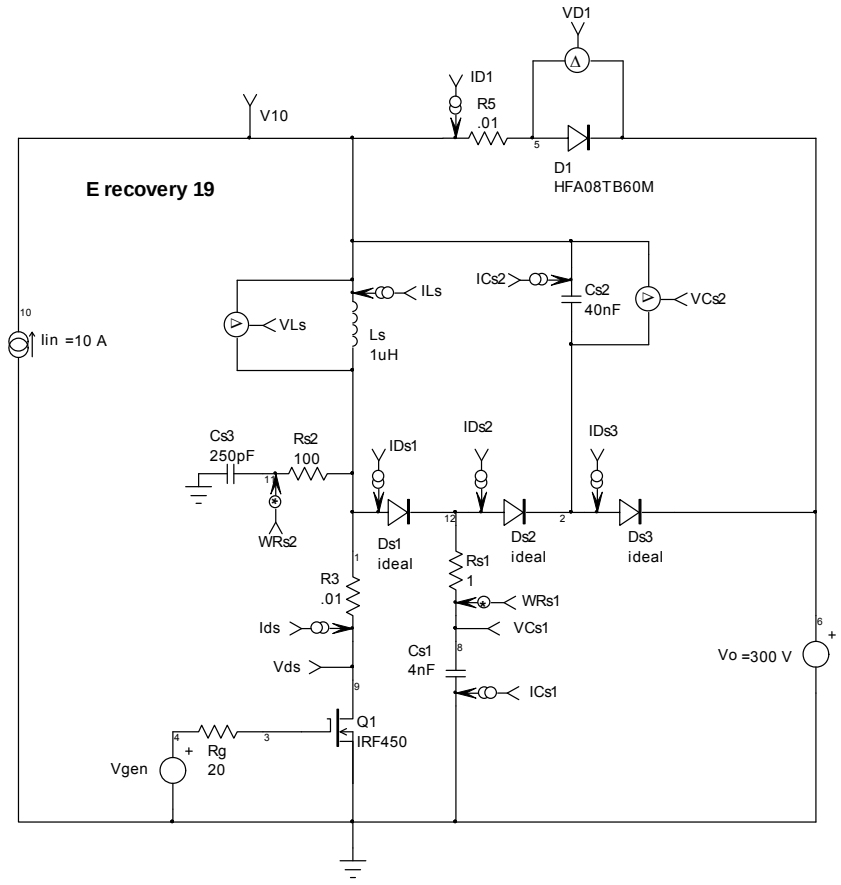


Figure 5-52, figure 5-49 with damping (Rs1, Rs2 and Cs3) added.

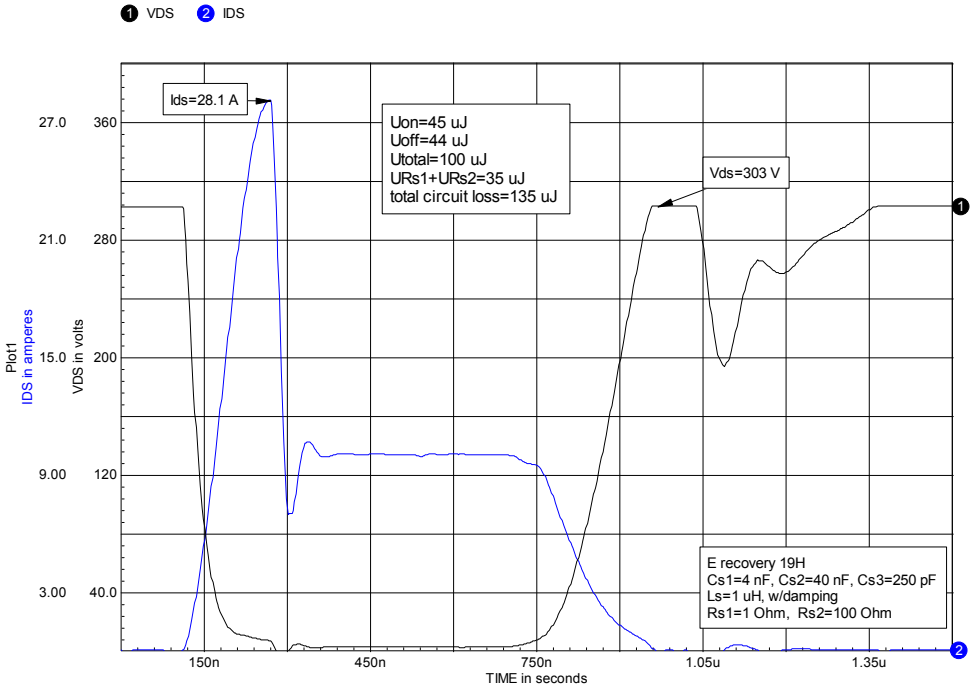


Figure 5-53, typical Q1 waveforms with damping added.

Now it is fair to ask, is example 2 any improvement over example 1? The total switch loss (Utotal) is a bit higher but the total circuit loss has dropped somewhat (149 μJ to 135 μJ). Example 2 has the advantage that Vds is clamped to within three diode drops of Vo (about 303 V in this example). This is an improvement over example 1 where Vds peak is 343 V. However, Ids peak at Q1 turn-on in example 2 is much higher (28 A versus 17 A). The component count is similar although there is one less diode and one less inductor in example 2. It could be argued that example 2 is not a great improvement over example 1. However, in some applications example 2 might be preferred.

This is a good example of the care which needs to be taken when selecting a snubber circuit. It is not always obvious which circuit is best and what trade-offs need to be made. As we saw earlier, in energy recovery snubbers the details of circuit operation during a switching cycle can be quite complex and a complete description of the action very involved. For the most part, complete discussions of every example have not been presented here but a description of one additional example can serve as a guide on how to perform such an analysis on other circuits. It will also illustrate how a apparently simple circuit can have very complex behavior.

The first step is to combine the voltage and current waveforms for the circuit elements in one graph as shown in figure 5-54, aligning the waveforms in time. At every point in time where the circuit state changes, a vertical dashed line is drawn through all the waveforms to relate changes in the waves at that time. This results in a hideous graph but, with a little patience, it serves several functions:

> First, it shows the points during one operating cycle where there is a discontinuity in one or more waveforms. These are points where, for example, diodes or other components start or stop conducting so the equivalent sub-circuit changes.

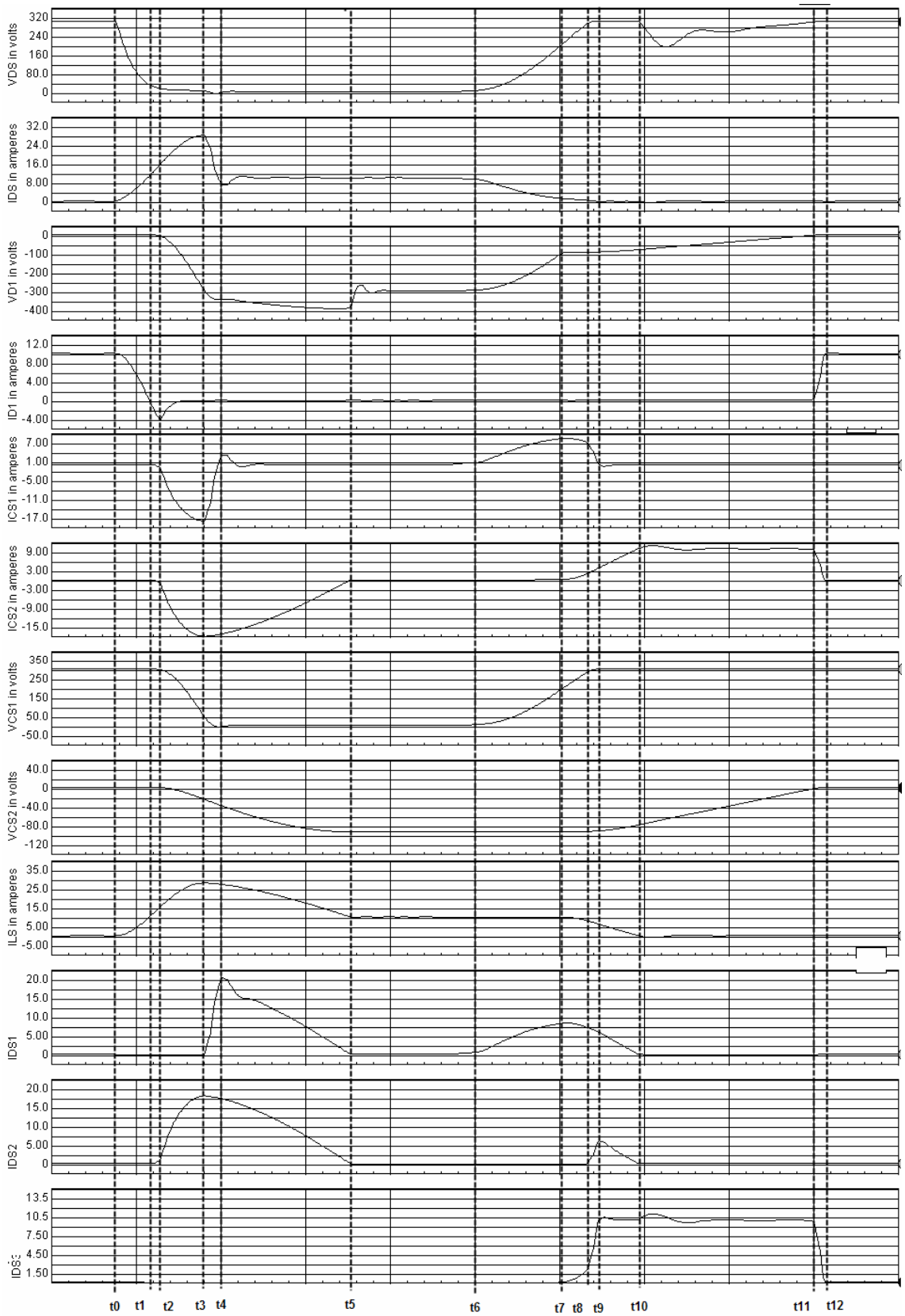


Figure 5-54, component waveforms during one switching cycle.

Second, it shows by inspection which components are conducting and which are not. This allows us to draw a series of sub-circuits, one for each state, which illustrate what is going on in the circuit during a particular time interval.

Third, it identifies the time intervals ($t0^+$-t1, t1-t2, ...,t12-$t0^-$, etc) are during which each sub-circuit is valid.

We will examine the circuit behavior during each time interval, beginning at $t0^+$ (the initiation of turn-on of Q1). The initial conditions just before Q1 turn-on ($t0^-$) are:

ILs=0,
VCs1=Vo,
VCs2=0 and
ID1=Iin.

For each time interval a sub-circuit can be drawn. Each sub-circuit will be comprised of the components that are in conduction during that time interval. Non-active components will be omitted.

$t0^+$-t1

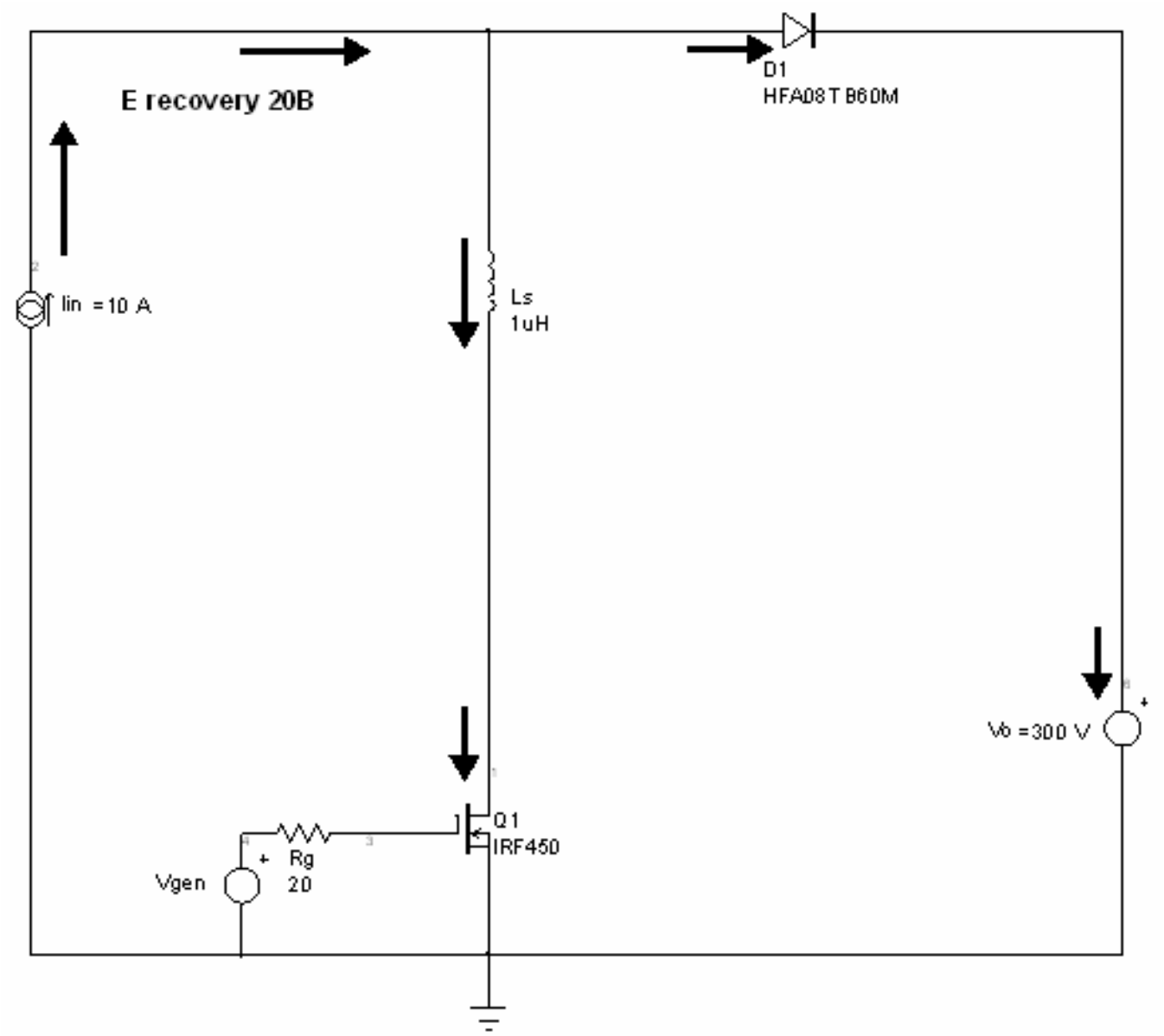


Figure 5-55, sub-circuit corresponding to $t0^+$-t1.

Figure 5-55 shows the equivalent circuit during $t0^+$-t1, the initial turn-on of Q1. D1 will have been conducting from the last switching cycle and current will begin to rise in Ls as Q1 turns on. Ls slows the rate of rise of Ids in Q1 which is desired action for a turn-on snubber.

t1-t2

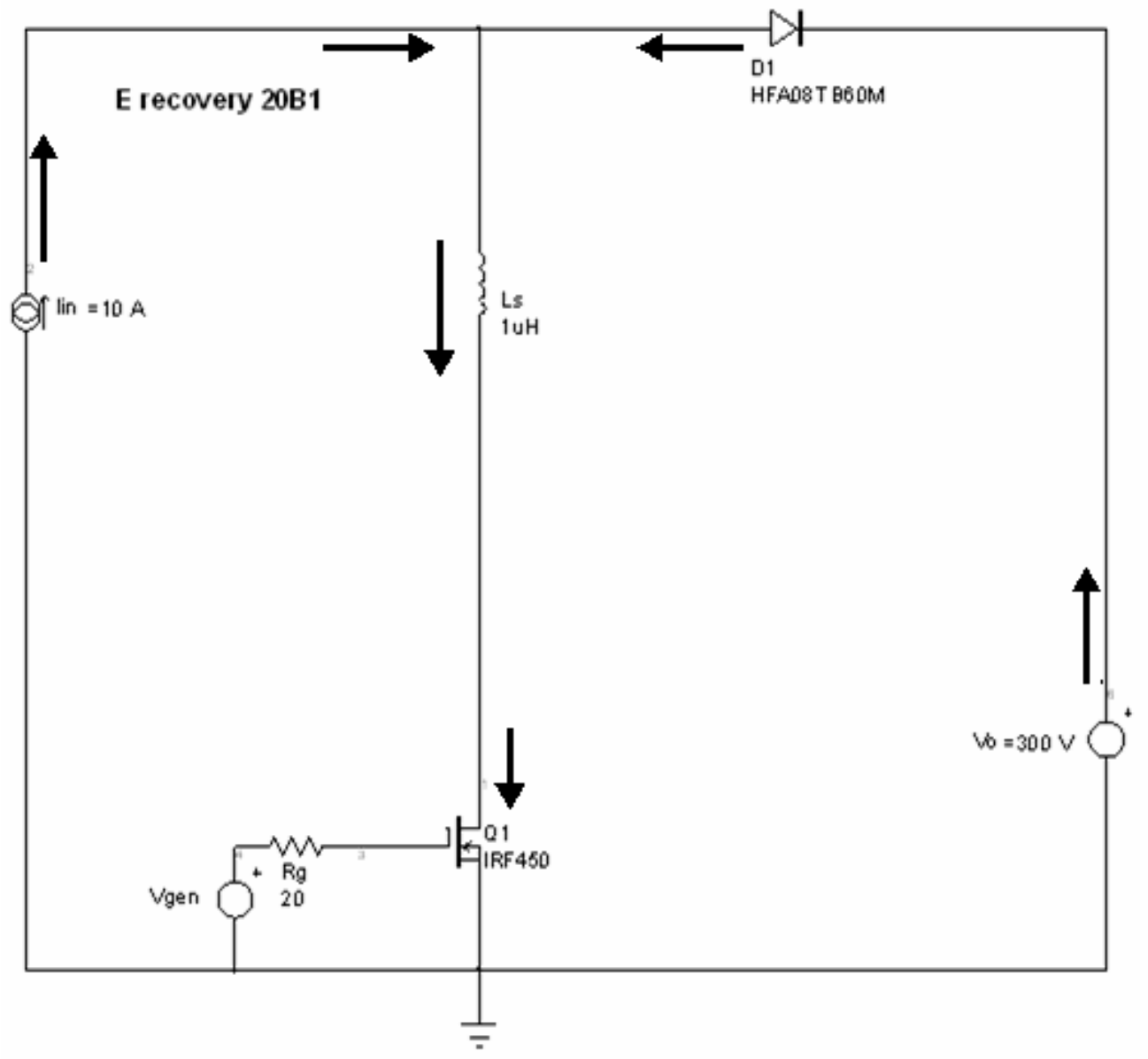


Figure 5-56, sub-circuit corresponding to t1-t2.

Figure 5-56 shows the equivalent circuit during t1-t2. At t1, ID1 reaches zero and begins to reverse. This initiates the first part of D1 reverse recovery. Ids continues to increase.

t2-t3

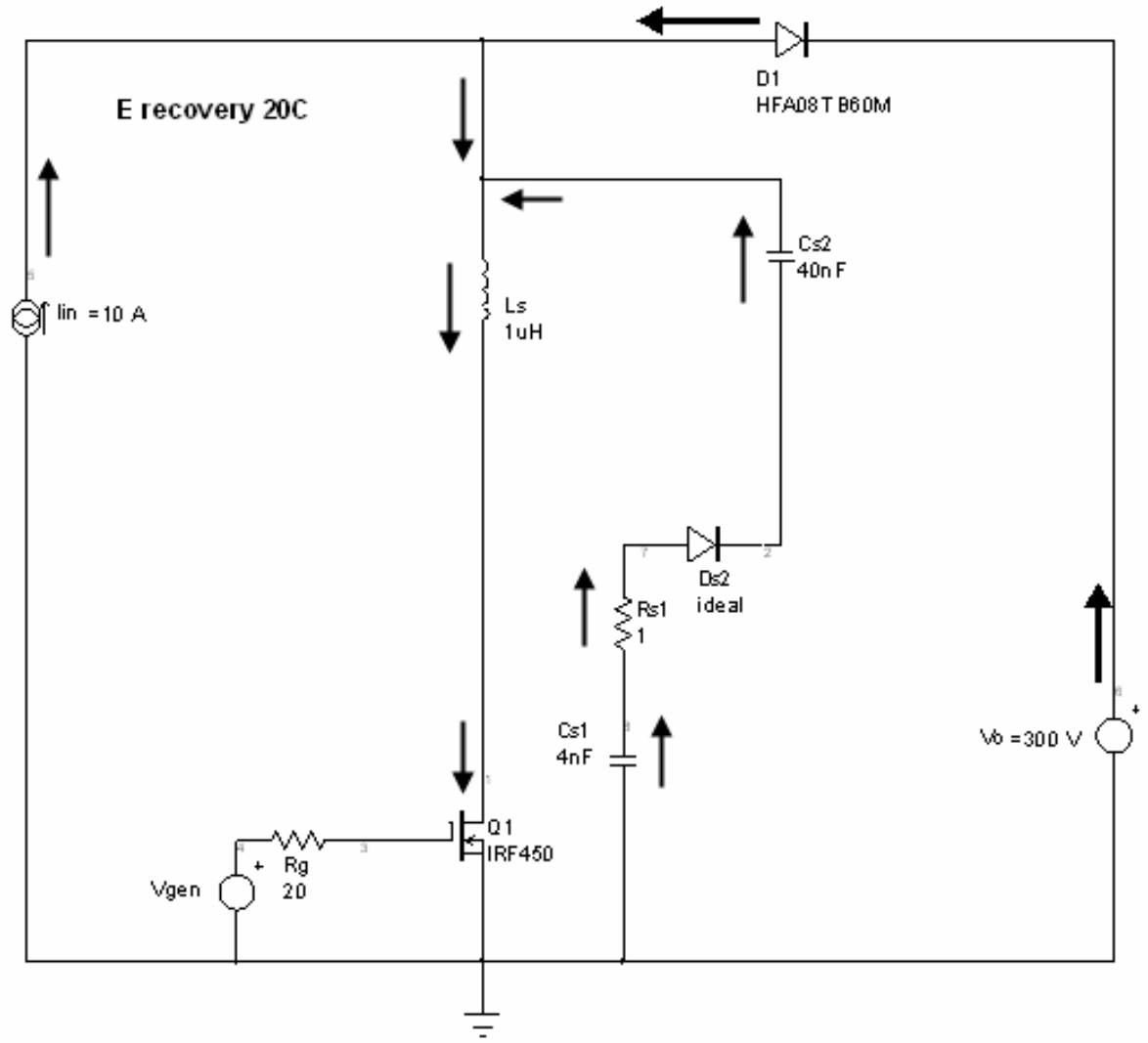


Figure 5-57, sub-circuit corresponding to t2-t3.

Figure 5-57 shows the equivalent circuit during t2-t3. At t2, the reverse recovery current in D1 reaches a negative peak and D1 enters the second part of reverse recovery where D1 can block reverse voltage and the current in D1 decreases. At t2 the voltage at the junction of Iin, Ls and D1 will begin to fall. This initiates the discharge of Cs1 through Rs1, Ds2, Cs2, Ls and Q1. The discharge of Cs1 is associated with the current spike in Q1 Ids which reaches a maximum at t3. Most of the energy in Cs1 ends up in Cs2 and Ls with a small amount dissipated in Rs1.

t3-t4

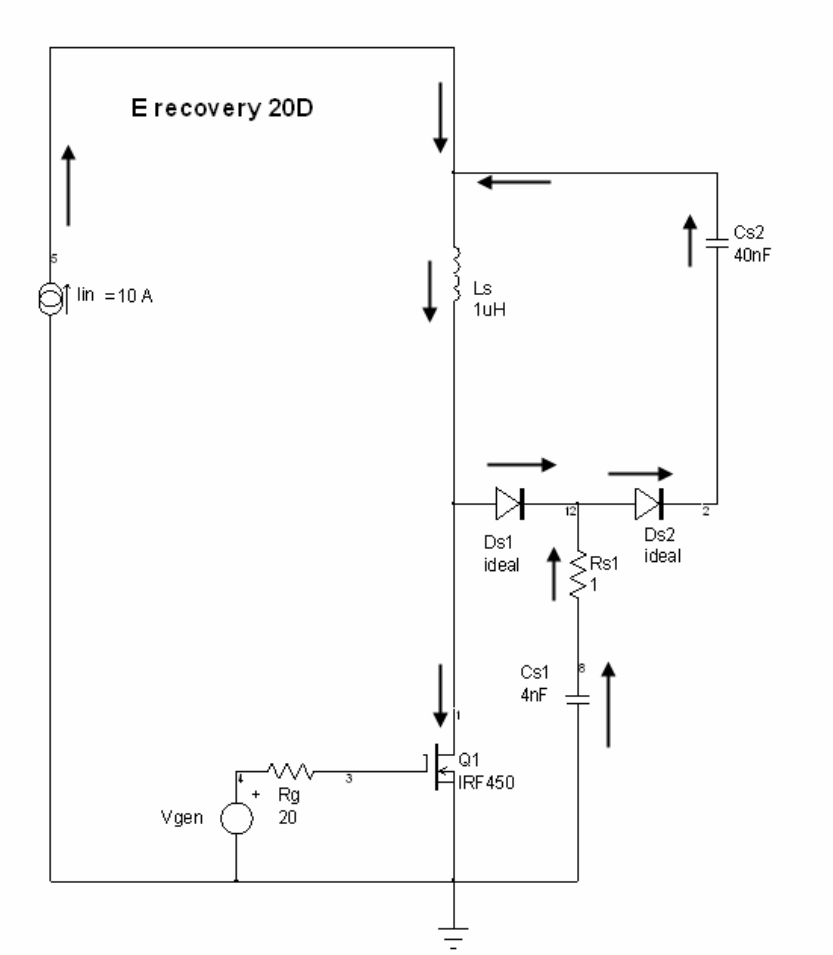


Figure 5-58, sub-circuit corresponding to t3-t4.

Figure 5-58 shows the equivalent circuit during t3-t4. At t3, Cs1 has discharged to the point where the voltage at the junction of Ds1, Ds2 and Rs1 is low enough (>Vds of Q1) that Ds1 can now begin conduction. VCs1 is low but not yet zero. However, there is a voltage drop across Rs1 which allows Ds1 to be forward biased. t3 also corresponds to the maximums of Ids and ILs. As ILs starts decreasing some of the energy in Ls is discharged into Cs2 via Ds1 and Ds2. Simultaneously the last of the energy in Cs1 is also discharged and VCs1=0 at t4.

t3 is also the point where VD1 = -Vo = -300 V. During t3-t4, Cs2 is being charged and VCs2 increases. This causes the junction of Iin, D1 and Ls to go negative, which in turn increases the reverse voltage across D1 beyond -Vo.

t4-t5

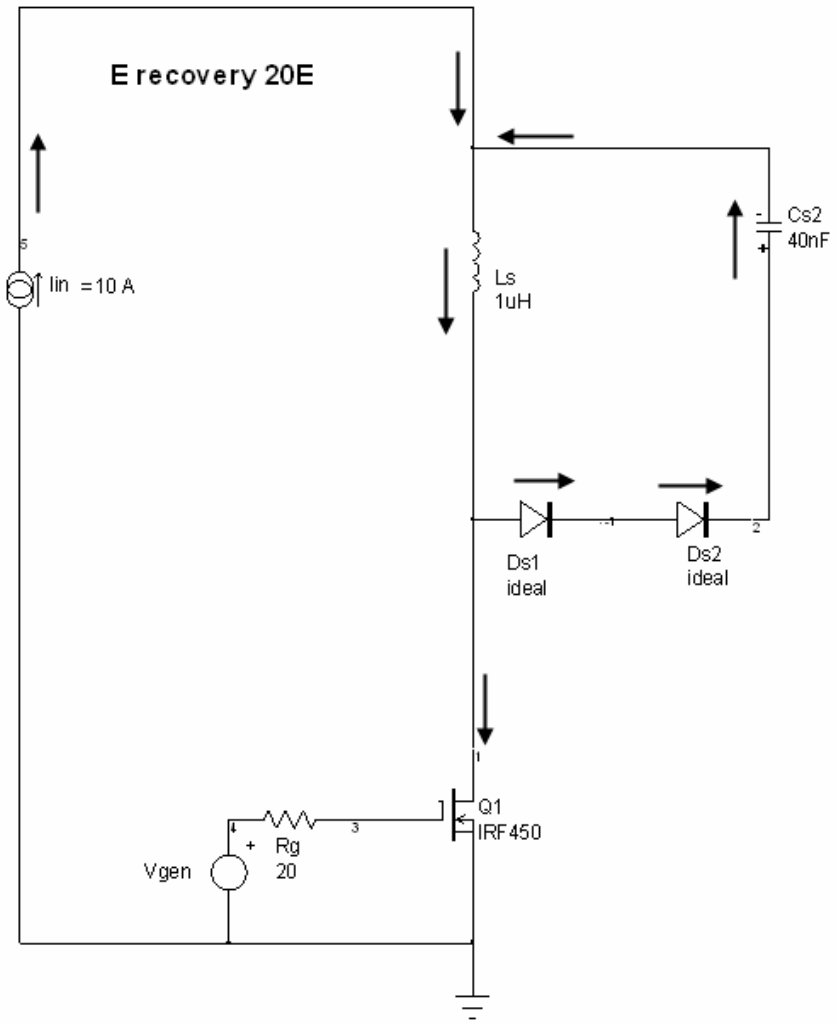


Figure 5-59, sub-circuit corresponding to t4-t5.

Figure 5-59 shows the equivalent circuit during t4-t5. During t4-t5 Ls continues to discharge into Cs2 until ILs=Iin = 10A. This occurs at t5. Ids for Q1 is a constant 10 A during this time interval. Note that during this interval VCs2 continues to increase and so does VD1. At t5 VCs1 = 85 V with the polarity indicated in the figure and VD1 = -385 V (VD1 = -[Vo + VCs2]). One of the penalties for using this snubber circuit is that it will increase both the peak current in Q1 and the peak reverse voltage across D1. The current spike on Ids is mostly due to the reset of Cs1 with a smaller contribution from the reverse recovery current of D1. The reverse voltage spike on D1 is due to the voltage across Cs2.

t5-t6

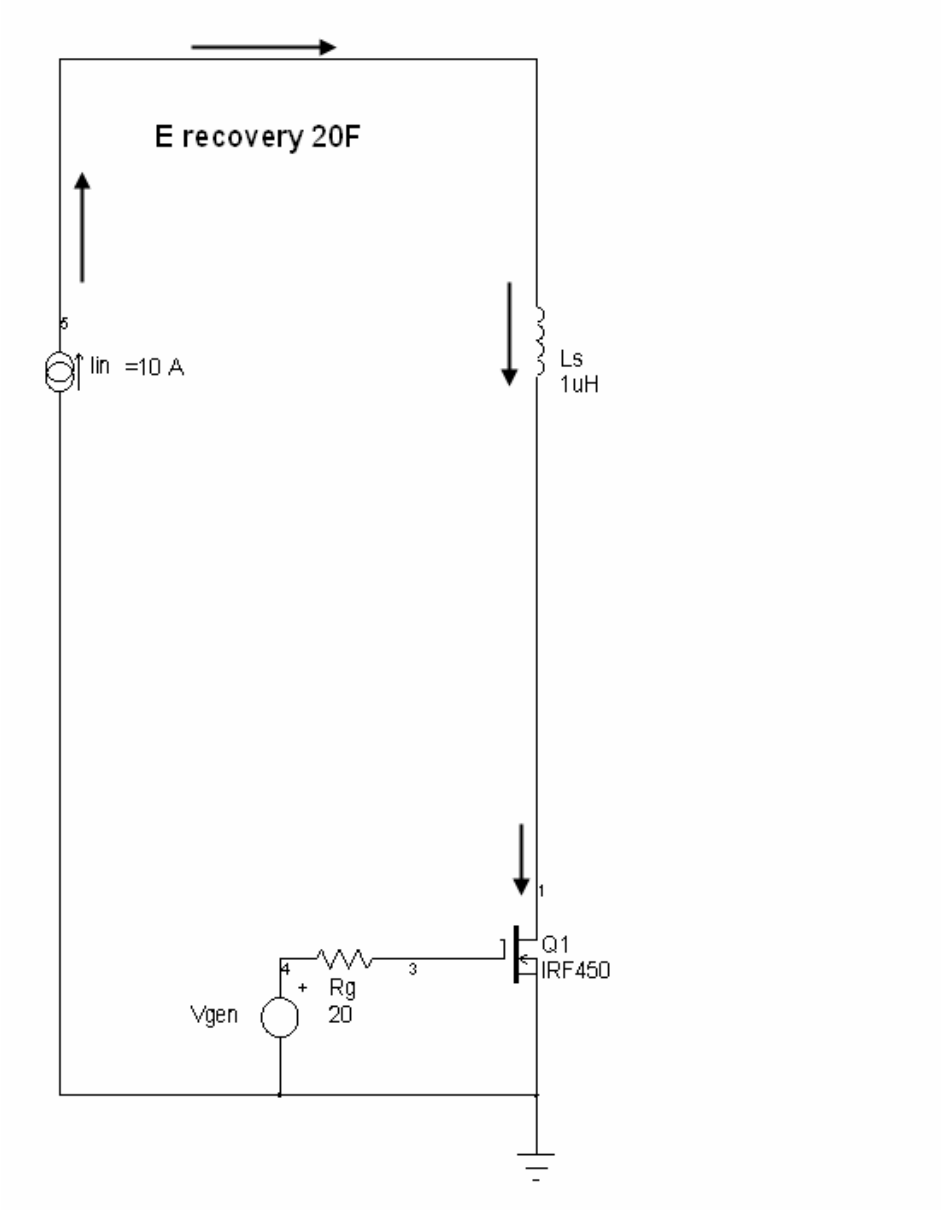


Figure 5-60, sub-circuit corresponding to t5-t6.

Figure 5-60 shows the equivalent circuit during t5-t6. At t5 the turn-on snubbing function and the energy transfer from Cs1 to Cs2 is complete and the circuit enters the normal "ON" state for the switch. This interval will persist until Q1 turn-off is initiated. Note that Ds3 has not conducted during the entire interval t0-t6 and will not begin to conduct until t=t7. Cs2 is used to store the energy recovered from Cs1 and Ls.

t6-t7

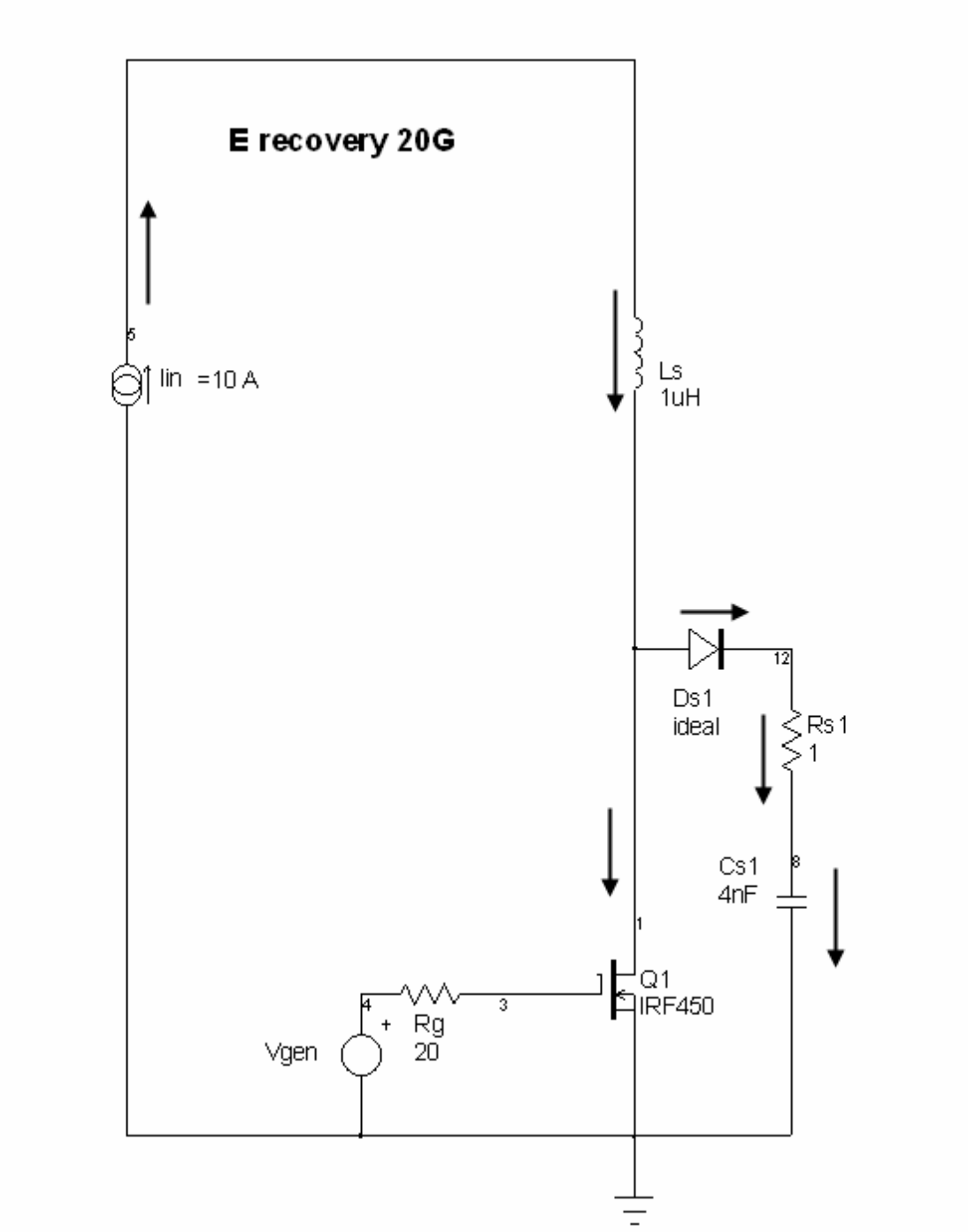


Figure 5-61, sub-circuit corresponding to t6-t7.

Figure 5-46 shows the equivalent circuit during t6-t7. The turn-off sequence for Q1 begins at t=t6. During the interval t6-t7, Cs1 behaves as a normal capacitive turn-off snubber.

t7-t8

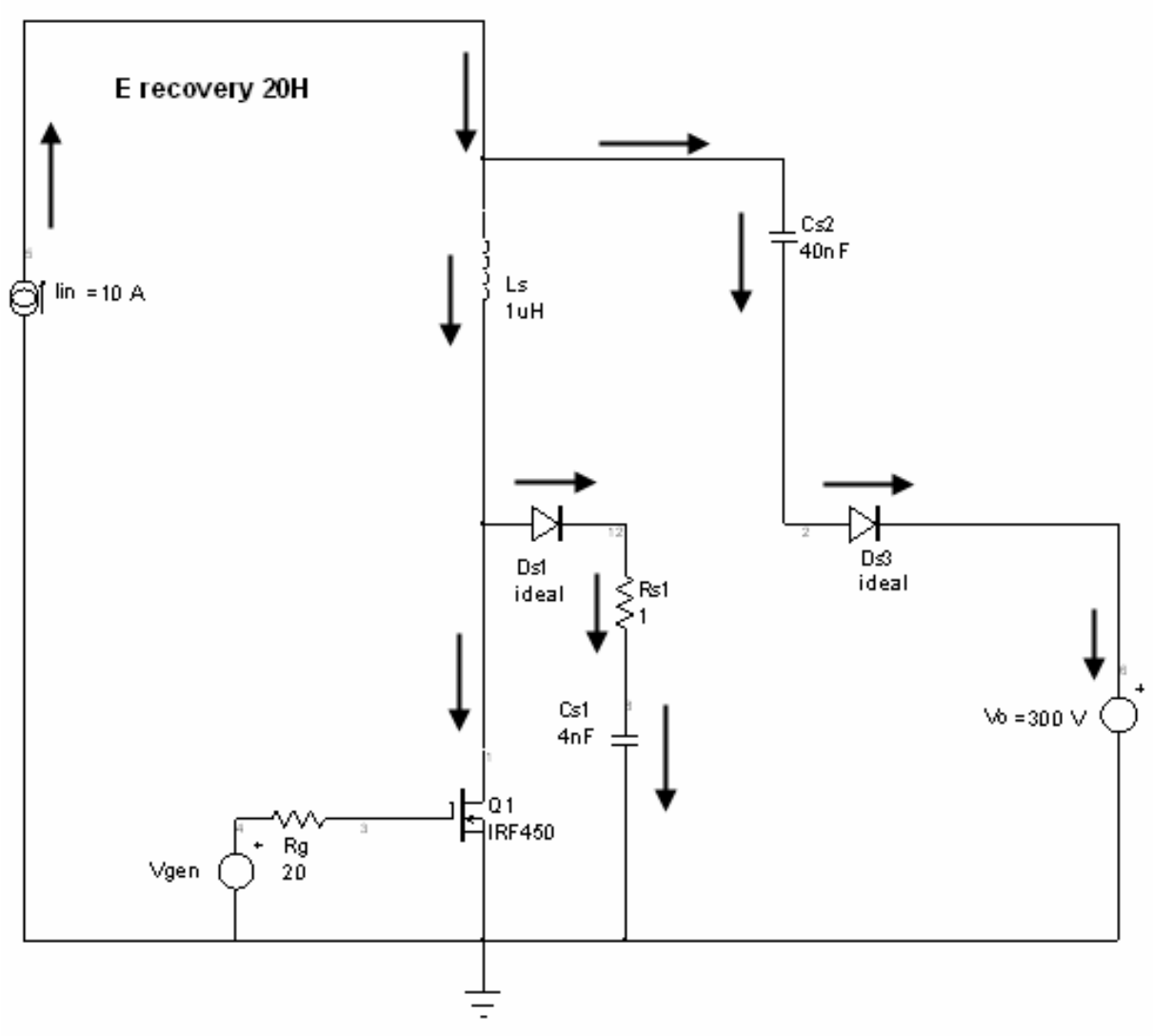


Figure 5-62, sub-circuit corresponding to t7-t8.

Figure 5-62 shows the equivalent circuit during t7-t8. At t=t7, the voltage (V10) at the junction of Iin, D1, Ls and Cs2 has risen to the point where Ds3 becomes forward biased (V10=Vo-VCs2). This is also the point where ILs begins to fall from 10 A. The difference between Iin and ILs flows through Cs2 and Ds3 into Vo and the energy discharge of Cs2 into Vo begins.

t8-t9

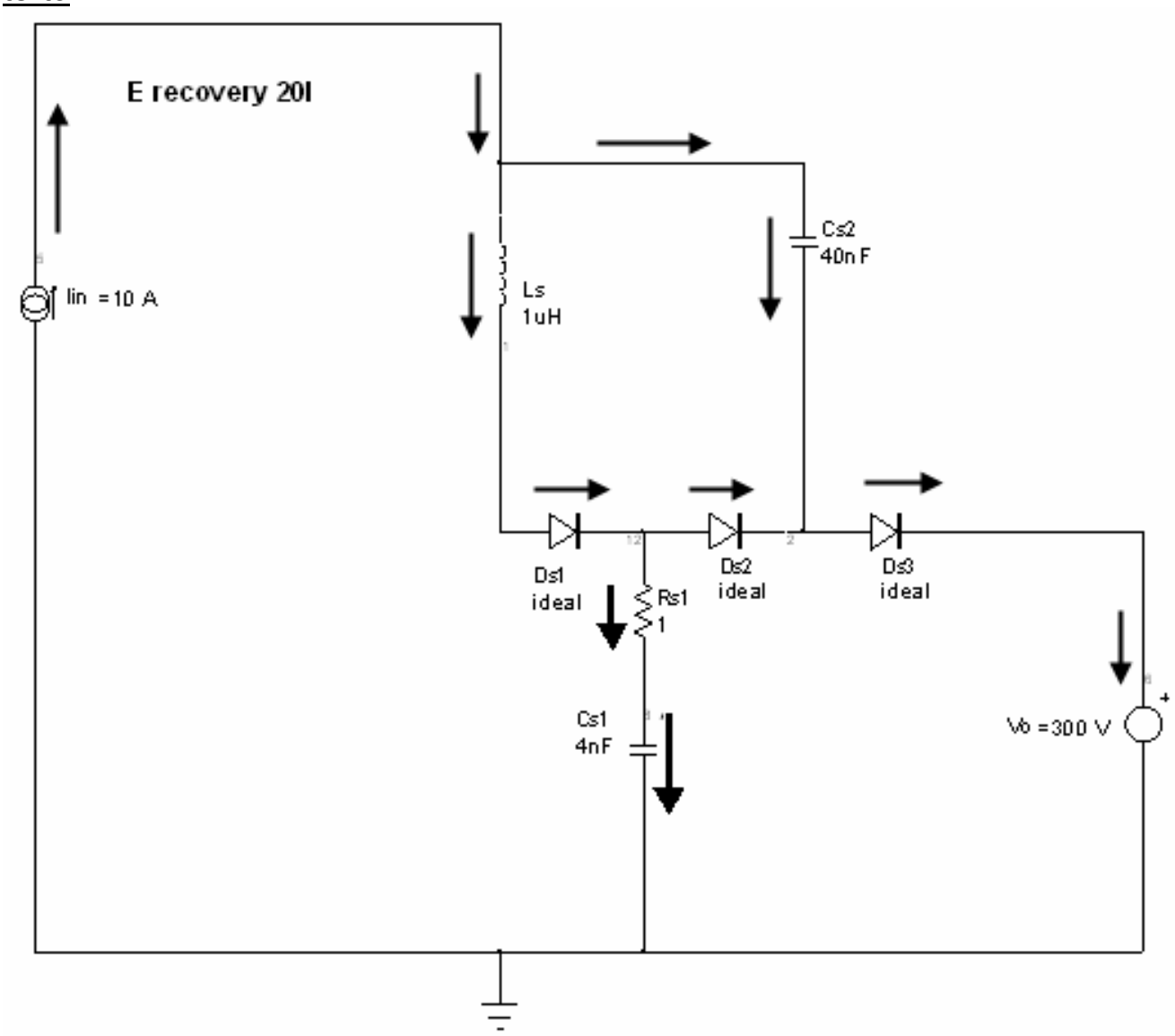


Figure 5-48, sub-circuit corresponding to t8-t9.

Figure 5-48 shows the equivalent circuit during t8-t9. At t=t8, VCs1 has not quite risen to the point where Ds2 would conduct but there is enough voltage drop across Rs1 to allow Ds2 to begin conduction. Charging of Cs1 continues until t=t9, at which point VCs1=Vo + two diode drops.

t9-t10

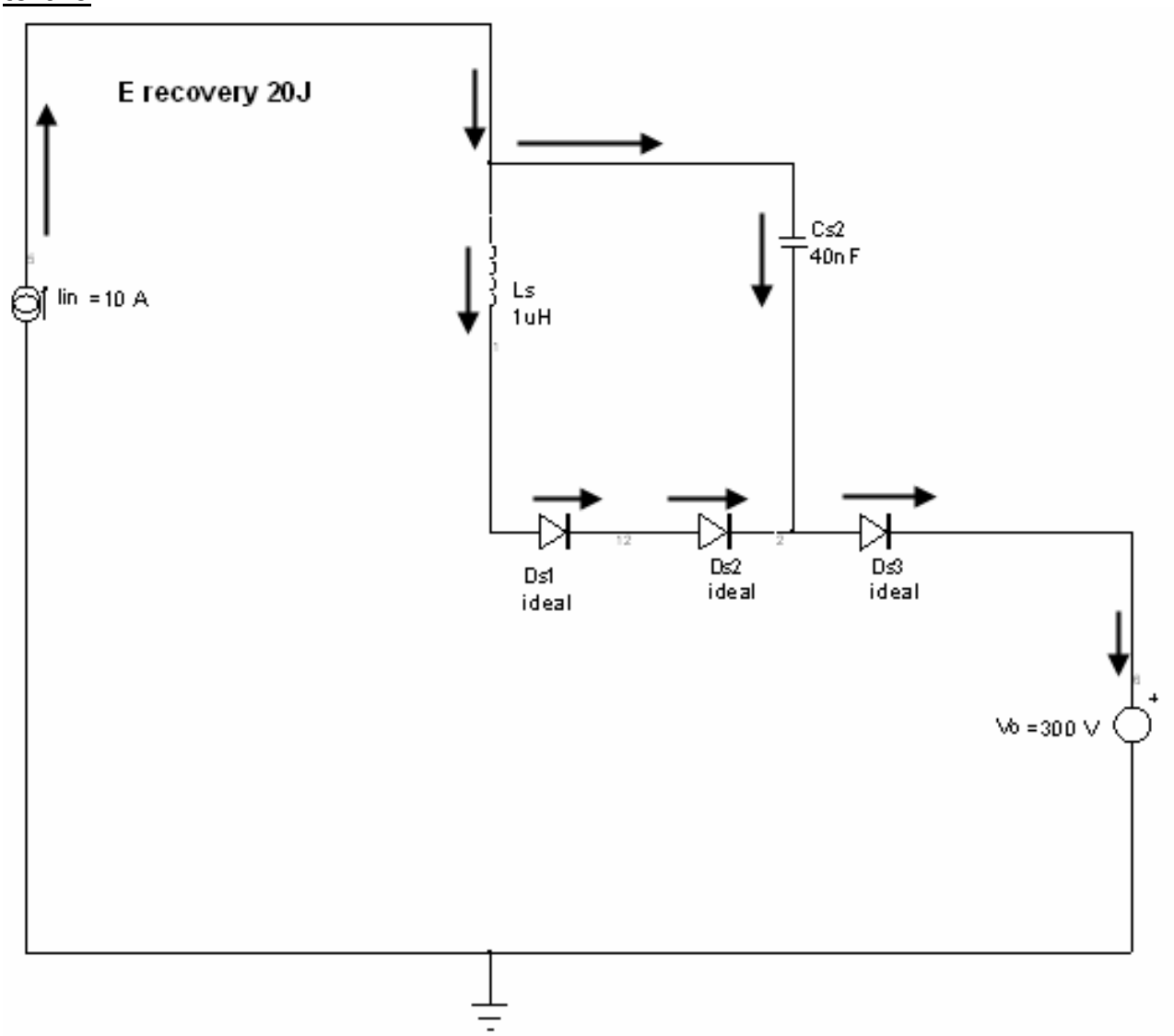


Figure 5-64, sub-circuit corresponding to t9-t10.

Figure 5-64 shows the equivalent circuit during t9-t10. At t=t9, Cs1 is fully charged and clamped to Vo via Ds2 and Ds3 in series. During the interval t=t9-t10, the remaining energy in Ls and some additional part of the energy in Cs2 is transferred to Vo. At t=t10 Ls is fully discharged and ILs= 0. Ds1 and Ds2 cease conduction.

t10-t11

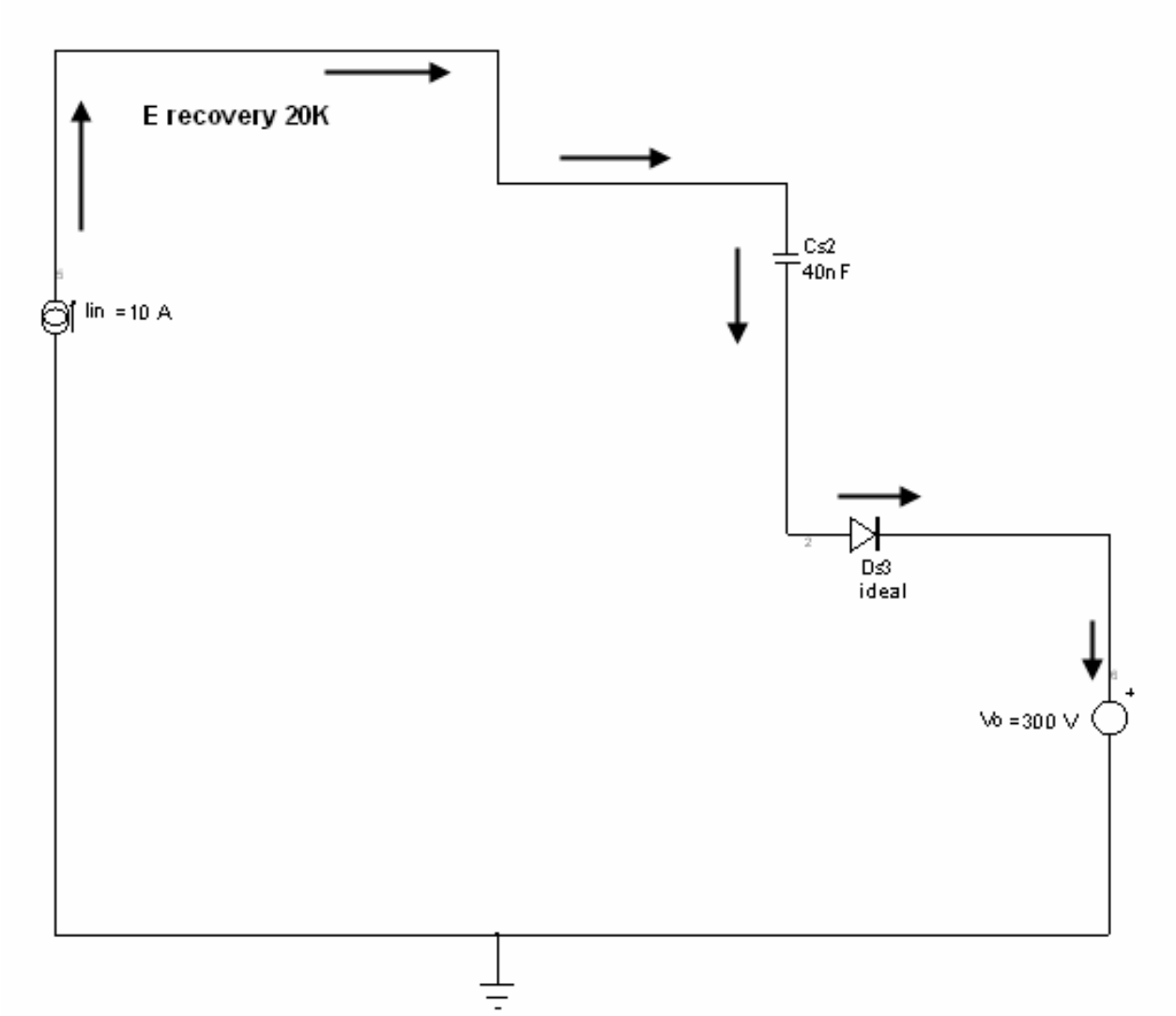


Figure 5-65, sub-circuit corresponding to t10-t11.

Figure 5-65 shows the equivalent circuit during t10-t11. During the interval t=t10-t11, Iin flows through Cs2 and Ds3, continuing the discharge of Cs2.

t11-t12

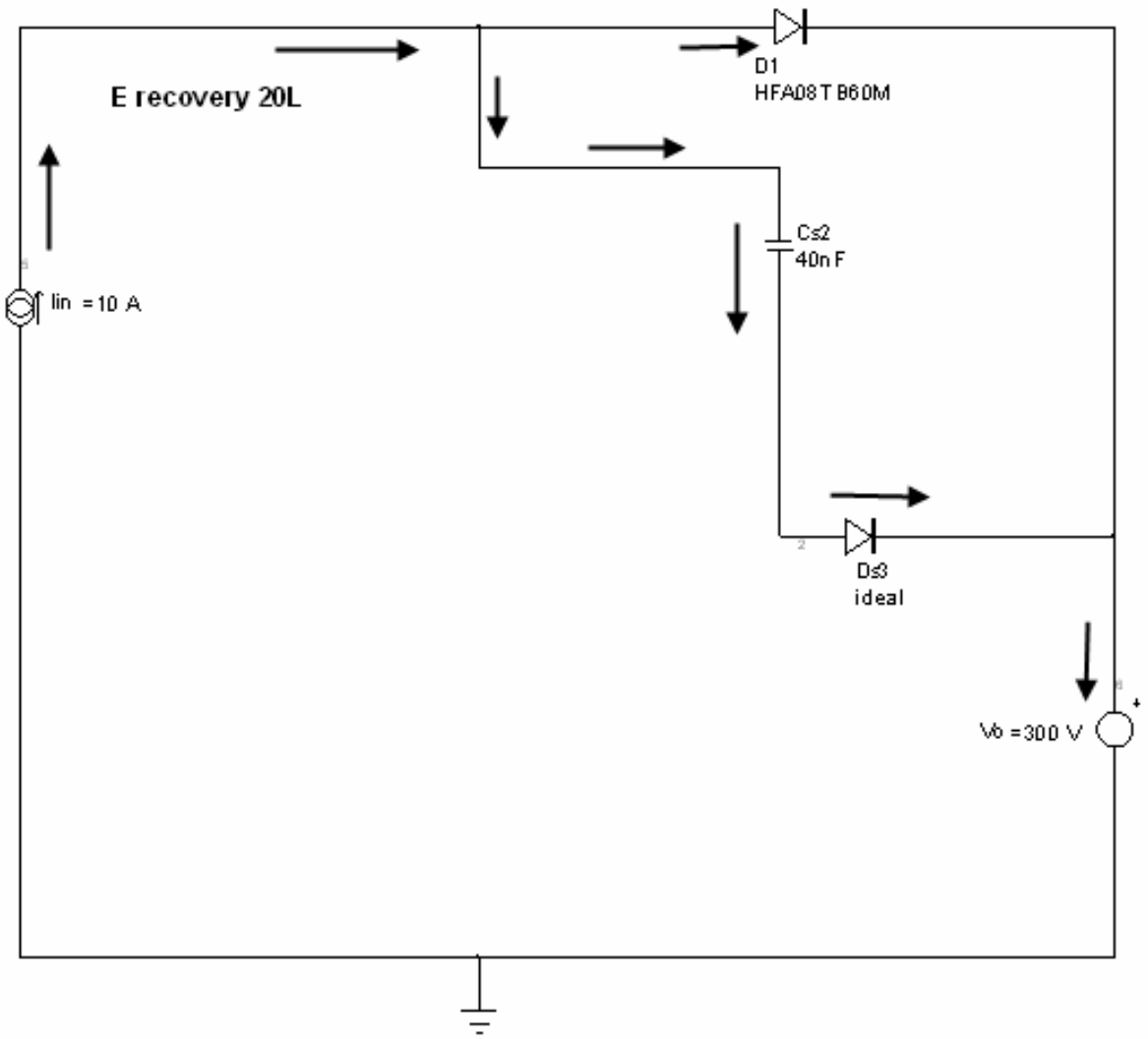


Figure 5-66, sub-circuit corresponding to t11-t12.

Figure 5-66 shows the equivalent circuit during t11-t12. At t=t11, as Cs2 is nearing complete discharge, V10 rises to the point where D1 goes into conduction and Iin commutates from Cs1 to D1.

t12-t0$^-$

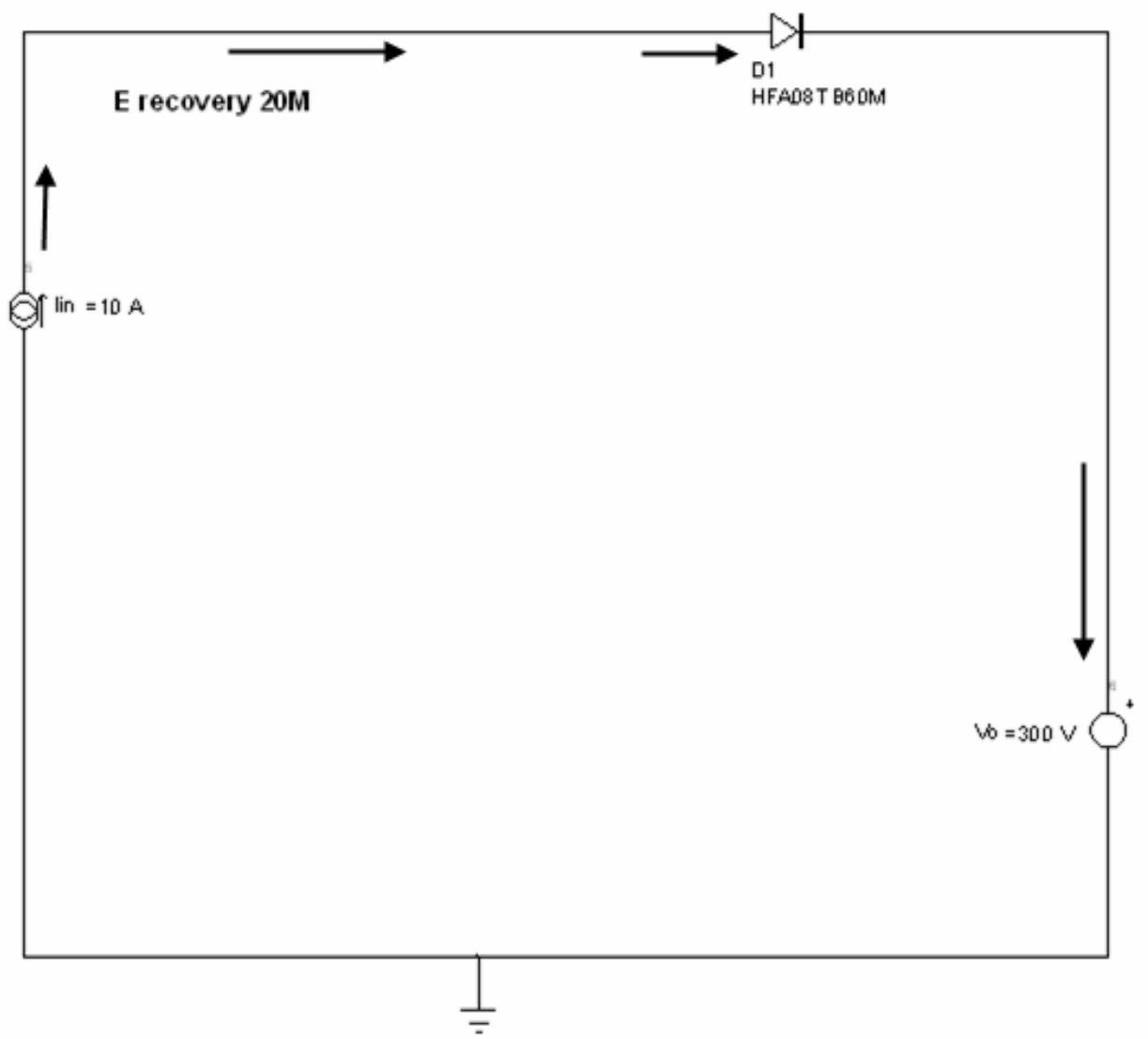


Figure 5-67, sub-circuit corresponding to t12-t0$^-$ next cycle.

Figure 5-67 shows the equivalent circuit during t12-t0$^-$. Finally, at t=t12 the discharge of Cs2 is complete and Iin is flowing through D1. The circuit is now in the normal off state for the switch awaiting turn-on of Q1 at the beginning of the next switching cycle.

A flyback converter snubber

A primary concern in converters with transformer isolation is the switch voltage spike at turn-off due to the leakage inductance of the transformer or coupled inductor. The amplitude of the voltage spike can be limited by employing a snubber and with an energy recovery snubber, most of the energy can be saved. The following example is for a flyback converter however, the snubber circuit and variations of it can be used with many other converter topologies. Much of the following discussion is based on the work of Domb[88,89]. Only a general description of circuit operation will be given. For more detailed design information the reader is referred to Domb and the other references[164,165,210,321,322,347,350].

An example of a flyback converter is given in figure 5-68.

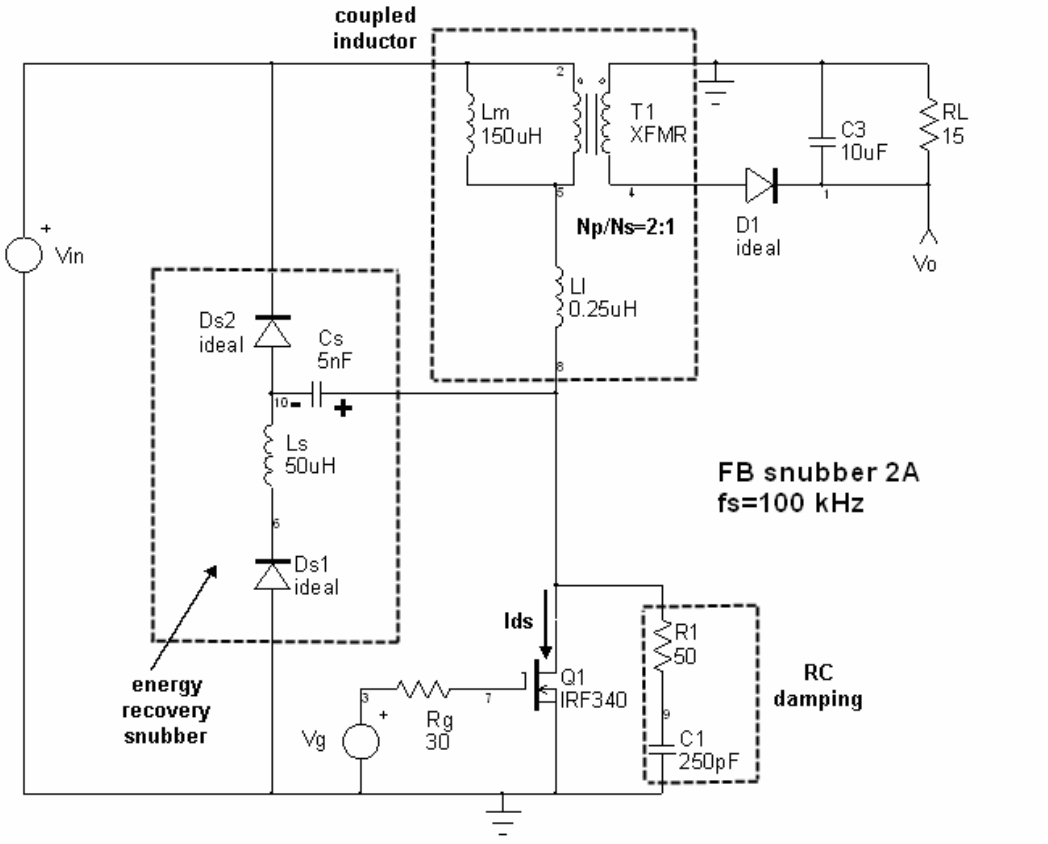


Figure 5-68, Example of a typical flyback converter with snubbers.

In this example the coupled inductor is represented by it's magnetizing inductance (Lm), leakage inductance (Ll) and an ideal transformer, which for this example has a turns ratio of 2:1. As pointed out earlier, some RC damping (R1 & C1) is usually required with energy recovery snubbers. Cs, Ls, Ds1 and Ds2 form the energy recovery turn-off snubber.

Just prior to Q1 turn-on ($t0^-$), the voltage across Cs (VCs) will have the polarity indicated. The value of VCs (VCsm) at $t0^-$ will depend on the operating conditions (Vin, Ids, load, etc) and the component values. This will be discussed shortly.

Domb has shown that four different modes of operation are possible, keyed to the maximum voltage on Cs (VCsm) but before discussing the different operating modes we will examine the circuit operation in one mode. This will make it easier to discuss the differences between operating modes.

Typical Vds and Ids waveforms for Q1 are shown in figure 5-69.

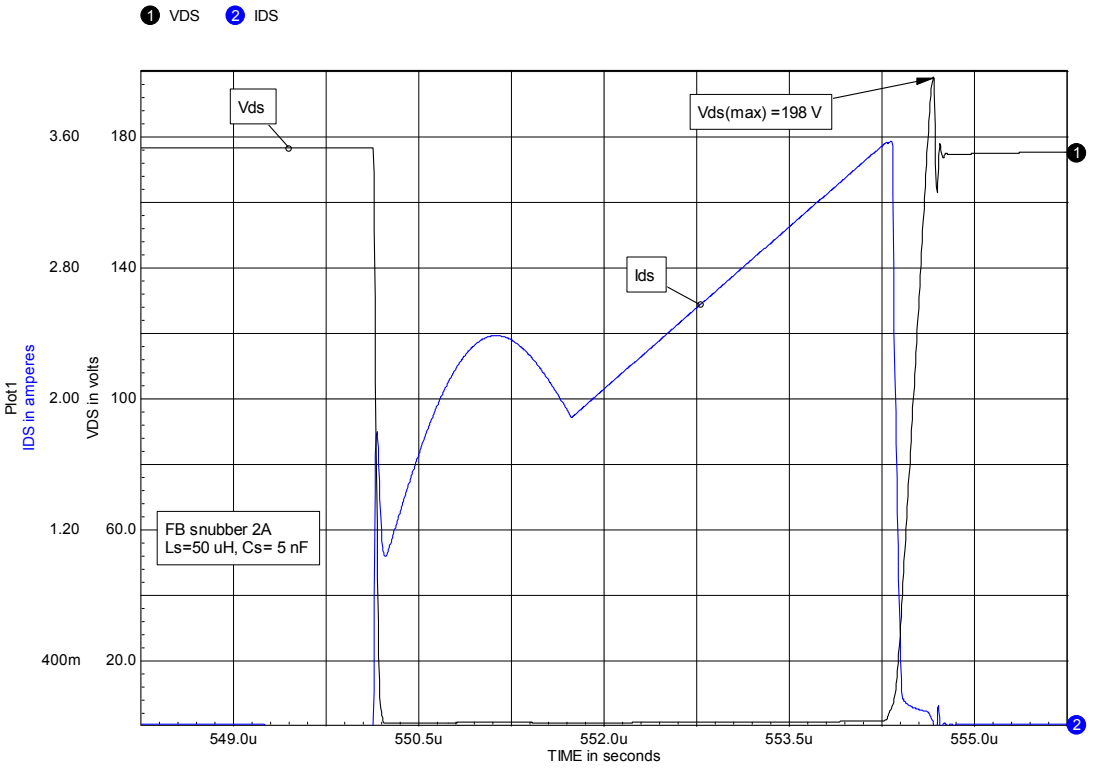


Figure 5-69, typical Vds and Ids waveforms for Q1.

At turn-on there is a current spike due to the discharge of C1 through R1 and Q1. There is also a 1/2-cycle ringing current pulse added to Ids. This is due to the resonant discharge of Cs around the loop formed by Ls, Ds1 and Q1. The waveforms for VCs and ICs are given in figure 5-70.

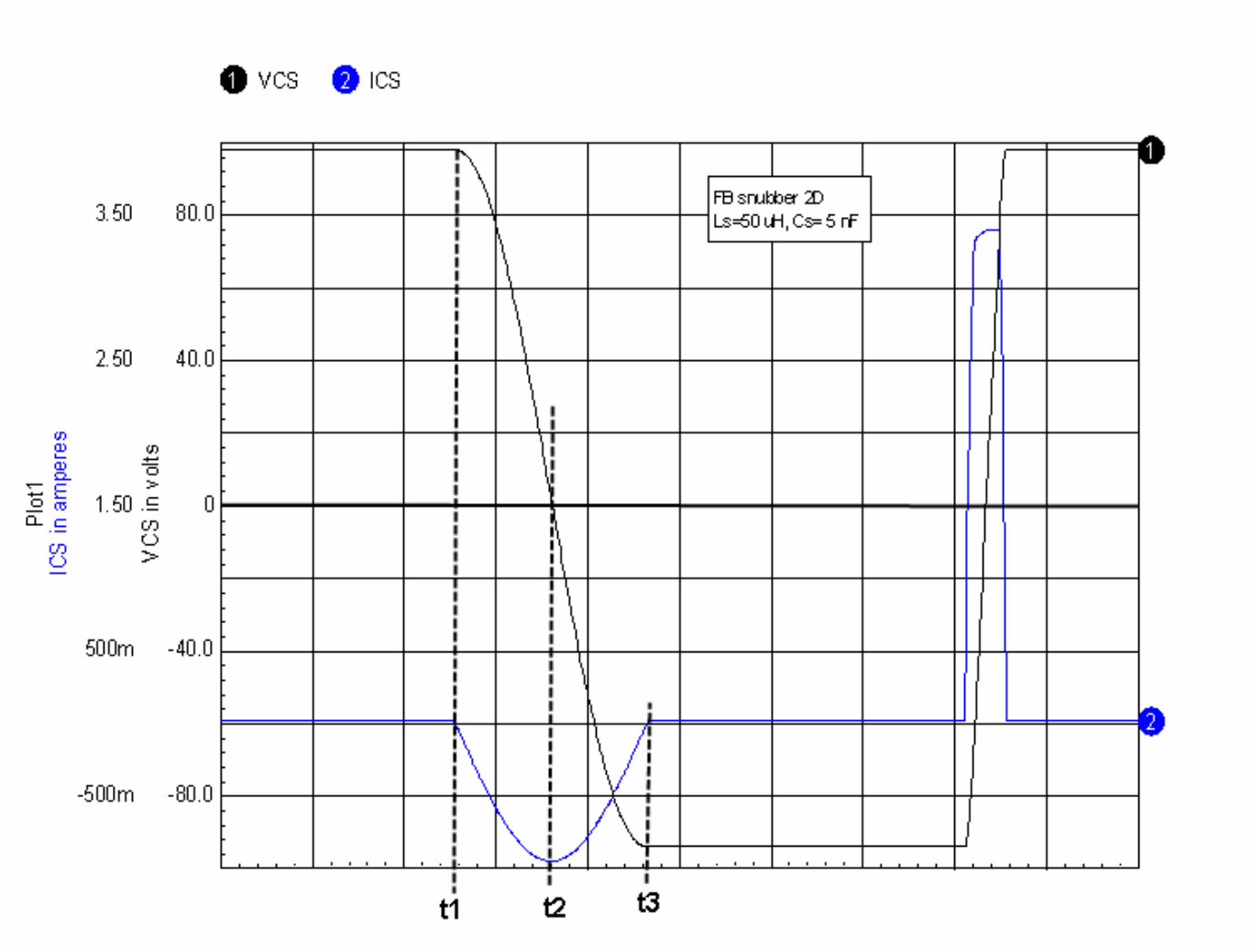


Figure 5-70, Cs waveforms during one switching cycle.

The energy in Cs is first transferred to Ls during the interval t1-t2 and then the energy in Ls is discharged back into Cs during interval t2-t3. At the end of the ringing interval, the polarity of VCs will be reversed as shown and it's amplitude very nearly the same as before the ringing with the exception of some dissipation in the process. Note that in this mode, at Q1 turn-on, energy is not returned to either the source or the load. Ls is serves only to reverse the polarity of VCs.

In other modes, some of the energy taken from Cs may returned to the source directly from Ls.

With it's polarity reversed, Cs is now ready to act as a capacitive turn-off snubber for Q1. An expanded view of the waveforms during the turn-off interval is given in figure 5-71.

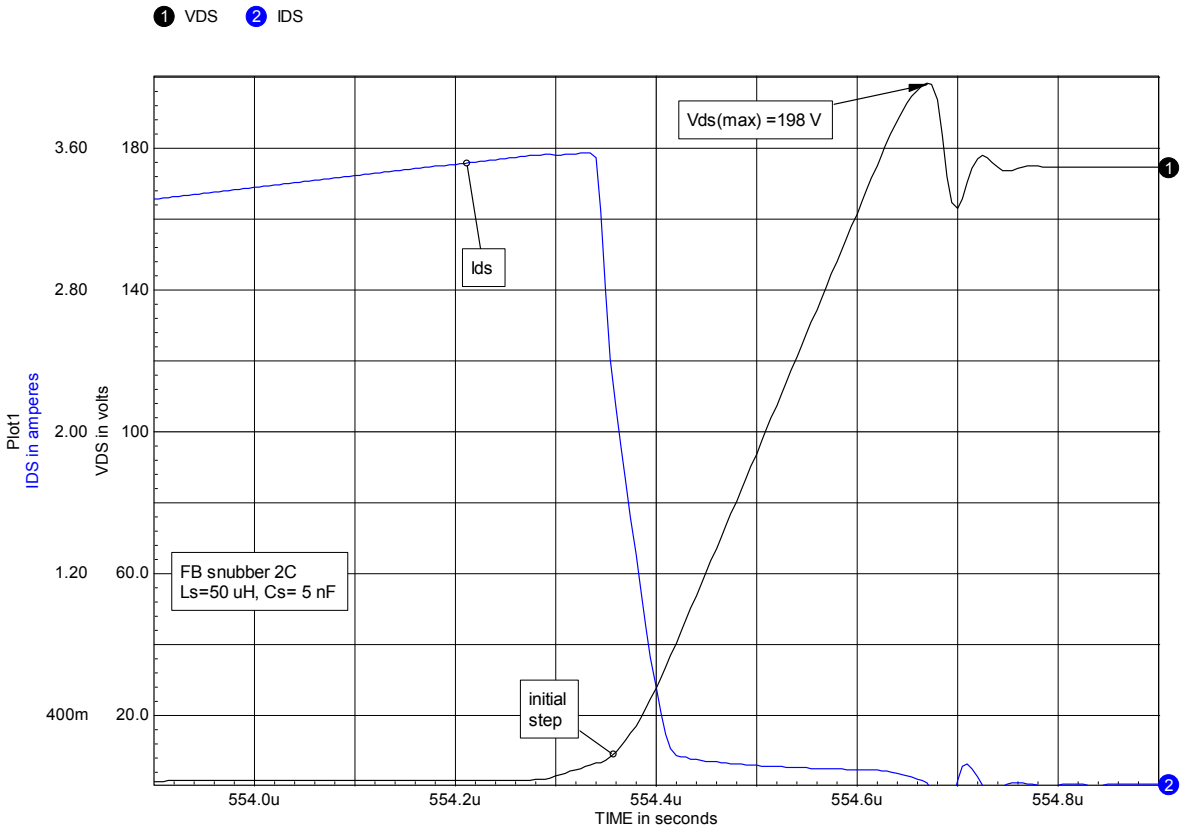


Figure 5-71, Q1 Vds and Ids waveforms during turn-off.

The waveforms are typical for a capacitive turn-off snubber. In this case, the value for Cs is usually chosen to limit the voltage spike (Vds-max). Normally this will result fairly heavy turn-off snubbing as shown. As Vds begins to rise at Q1 turn-off, there is a small kink or step in the waveform, labeled "initial step" in figure 5-71.

What interests us here is the disposition of the energy saved from the turn-off transition and the energy from the leakage inductance. From figure 5-70 we can see that VCs ≈ -92 V but Vin = 100 V, so there is a short period where Vds rises before Ids commutates to Cs. This

step will vary with operating mode and circuit component values. Usually it is small enough not to significantly affect Q1 turn-off losses.

The energy recovered from LI and Q1 turn-off is delivered to the output at Q1 turn-off. This process can be understood with the help of the VCs, ICs and VLI waveforms shown in figure 5-72.

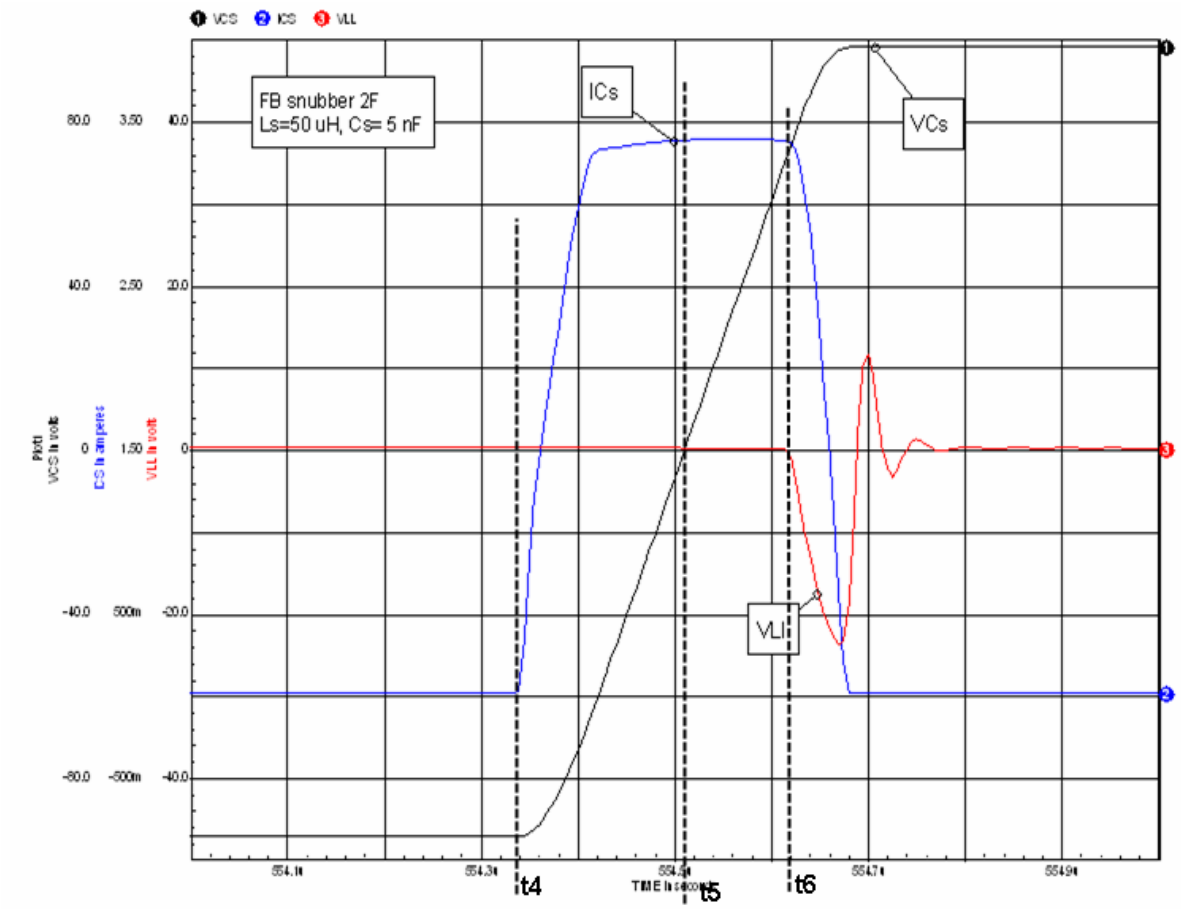


Figure 5-72, VCs, ICs and VLI waveforms at Q1 turn-off.

Time t4 corresponds to the step in the Vds turn-off waveform (figure 5-71). This is the point where Cs begins to discharge around the loop Cs, Ds1, Lm and LI. At t=t5 this discharge is complete and Cs begins to charge with the opposite polarity. This continues until t=t6, which is the point where D1 in the secondary begins to conduct, delivering energy to the output. At t=t6, LI begins to discharge into Cs. When that is completed, the turn-off portion of the switching cycle is finished and Q1 is in the off-state, awaiting turn-on. The energy recovered

from Ll will be delivered to Lm and then transferred to the output at the next Q1 turn-off.

If we increase the load by reducing RL to 7 Ohms and adjust the duty cycle to maintain the same Vo, we will increase Ip and modify the waveforms associated with Cs charging as shown in figure 5-73.

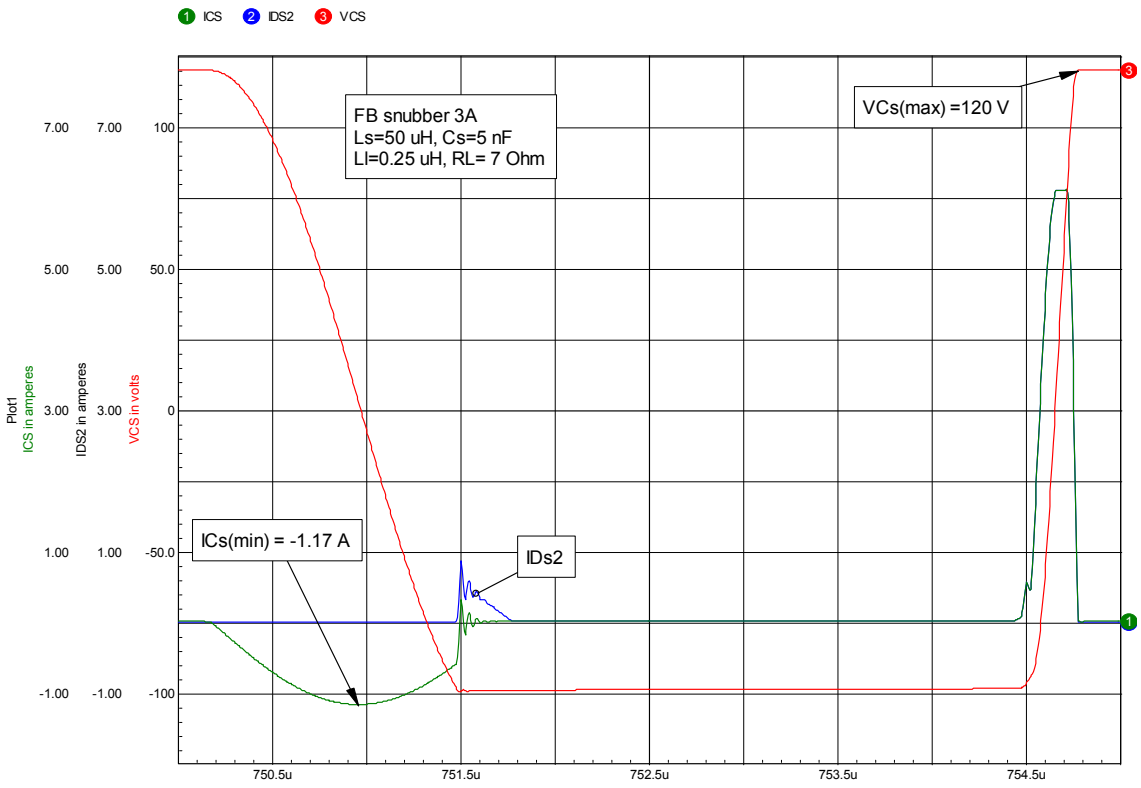


Figure 5-73, VCs, ICs and IDs2 for a heavier output load condition.

Note that at the end of Q1 turn-off, VCs= 120 V > Vin=100 V. At this point in the waveforms for RL= 15 Ohm, VCs=97.6 V < Vin=100 V. This heavier load condition represents a new operating mode. In this new mode, the 1/2-cycle ringing with Ls is terminated before ILs=0. At this point Ds2 begins to conduct and Ls discharges some energy into the source (Vin).

Domb has shown there are four operating modes which depend on the value of VCsm at $t0^-$:

$$mode1 \Rightarrow VCs(\max) \le Vin - \frac{Ns}{Np}Vo$$

$$mode2 \Rightarrow Vin - \frac{Ns}{Np}Vo \le VCs(\max) \le Vin$$

$$mode3 \Rightarrow Vin \le VCs(\max) \le Vin + \frac{Ns}{Np}Vo$$

$$mode4 \Rightarrow Vin + \frac{Ns}{Np}Vo \le VCs(\max)$$

VCs(max) is expressed by:

$$VCs(\max) \cong \frac{Np}{Ns}Vo + Ip\sqrt{\frac{Ll}{Cs}}$$

Where Np= primary turns, Ns= secondary turns, Vo= output voltage, Ll= leakage inductance, Cs= snubber capacitor and Ip= switch current at the beginning of Q1 turn-off. An approximate equality is used because in a real circuit there will be losses and diode drops which modify the exact mode boundaries but the approximation is still quite good.

For fixed values of Vin, Vo, Np/Ns, Ll and Cs, mode change is driven by changes in Ip, which depend on the output load. However, in practice, Vin will almost always vary, frequently by 2:1 or more. This will also affect the mode change points due to the effect of Vin on Ip. In most designs the range of Vin is given by the application, Ll is made as small as practical in the design of T1and we accept the residual value. Np/Ns is also fixed by the application. Ip is directly affected by the choice of Lm but Lm is usually chosen to provide either continuous or discontinuous inductor current over the load range (in the flyback converter). The value for Cs is driven by the size of Ll and the desired peak value of Vds.

The net result is that we simply accept the resulting operating modes and select component values from other considerations. Cs is selected to limit Vds peak and Ls is selected to allow complete inversion of the voltage across Cs during a time period less than the minimum on time of Q1, i.e.:

$$ton(\min) \geq \pi\sqrt{LsCs}$$

The reader is referred to Domb[88,89] for a detailed analysis of this snubber.

Energy recovery snubbers for bridge connections

Topologies using half-bridge, full-bridge and poly-phase switch connections can also employ energy recovery snubbers. While the previous energy recovery circuits can be adapted for this application, the symmetry of the switch connection provides some new opportunities.

Figure 4-70 illustrated a dissipative combination snubber. We can recover some of the trapped energy in this circuit by replacing the series resistor-diode (Rs3-Cs3) with a winding on the coupled inductor as shown in figure 5-74[286].

This configuration recovers some of the energy but there will still be substantial dissipation in Rs1 and Rs2.

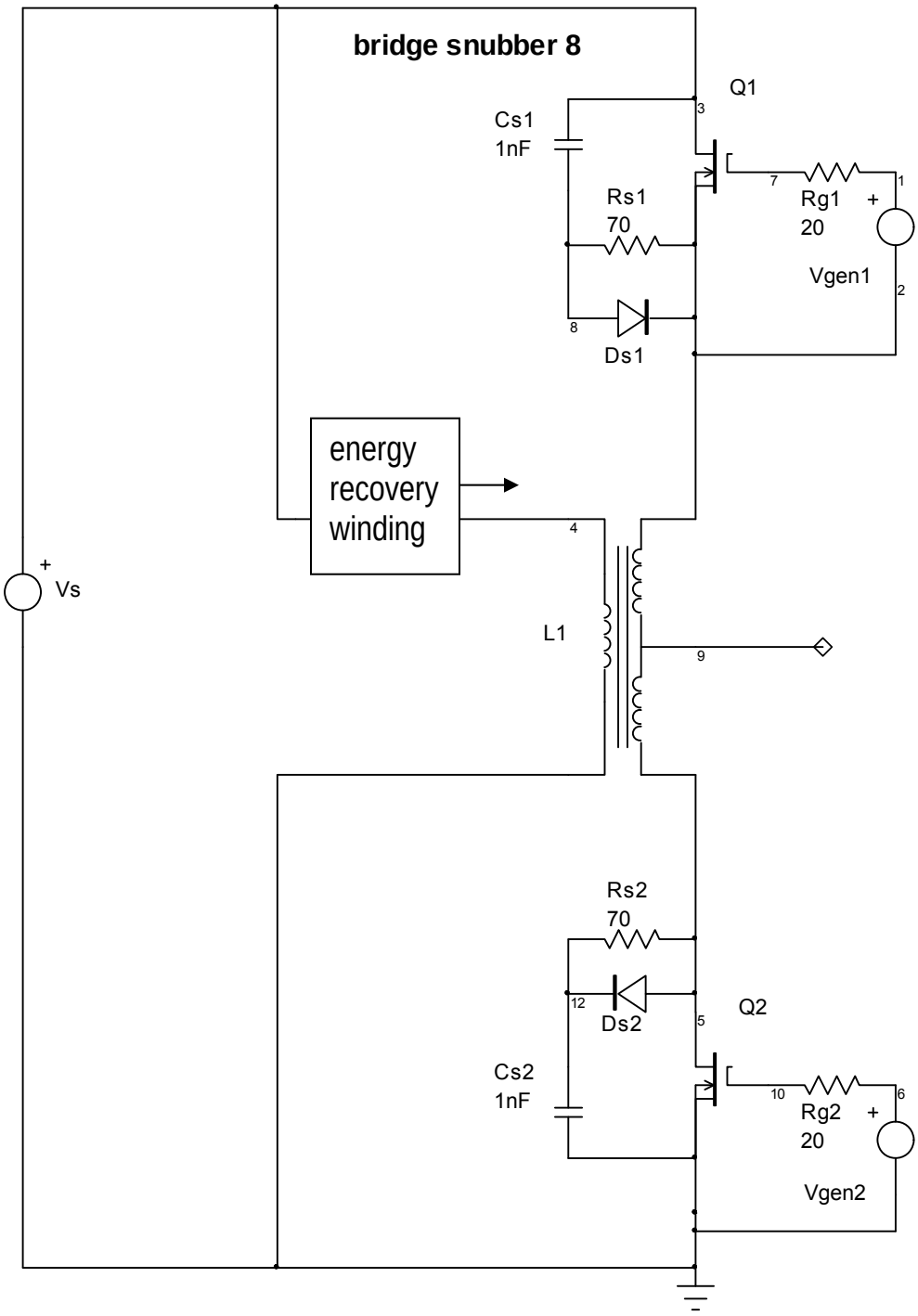


Figure 5-74, adding an energy recovery winding to the snubber inductance shown in figure 4-70.

A more efficient snubber which recovers most of the energy has been suggested by McMurray[286] and is shown in figure 5-75.

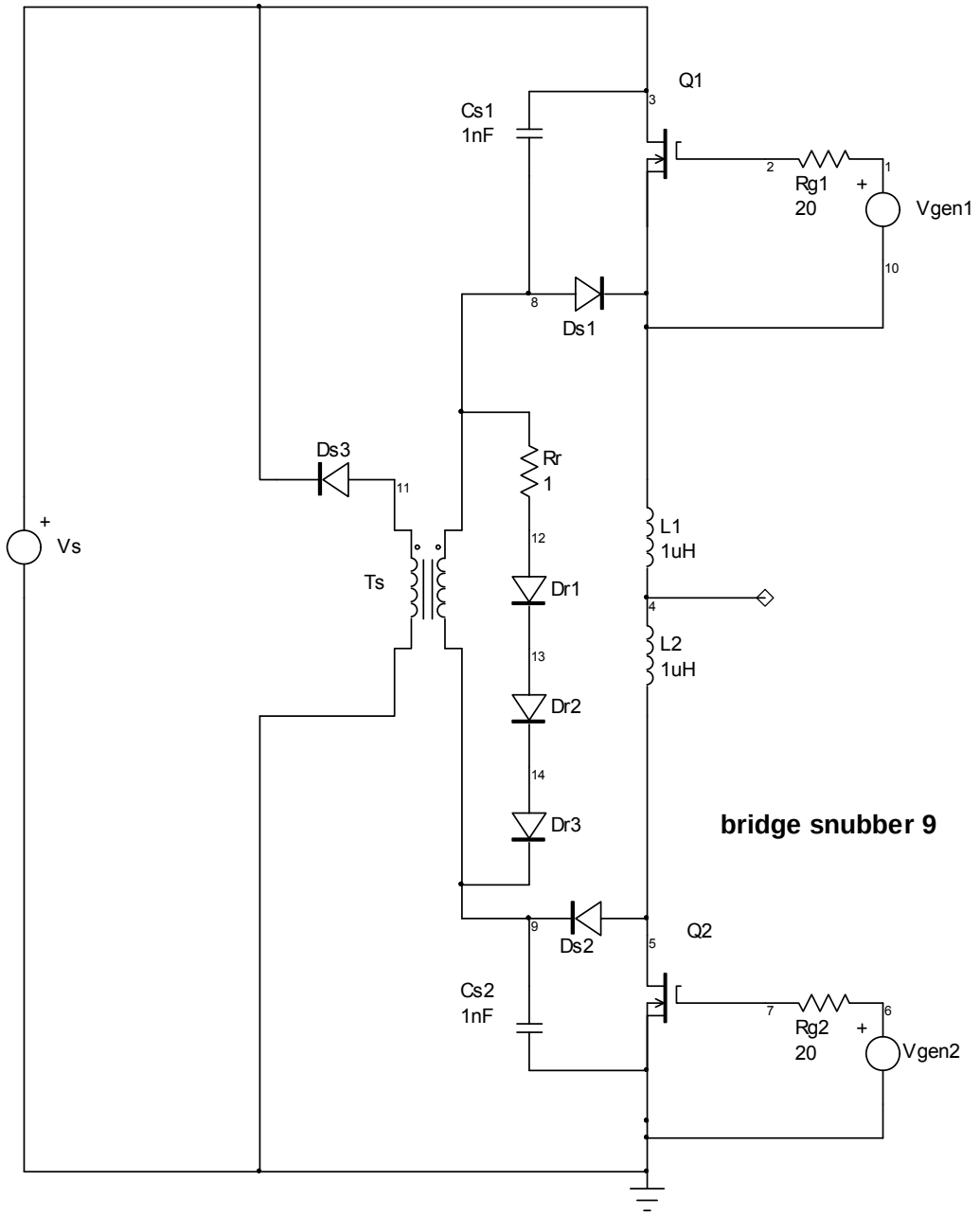


Figure 5-75, half-bridge energy recovery snubber.

L1 and L2 form a coupled inductor. Rr, Dr1, Dr2 and Dr3, are for core reset in Ts at the end of the recovery cycle when there may still be some energy stored in Ts.

Chapter 6

Component selection and circuit layout

Previous chapters have described how individual snubber circuits work and given some design guidance. The final steps in realizing an actual snubber are the component selection and the fabrication and testing of the snubber itself. In this chapter we will examine this step, beginning with the selection of suitable components, then deal with issues related to circuit layout and finally discuss some measurement issues.

With modern semiconductor switches it has become possible to have power converters processing hundreds of kW while switching at frequencies of hundreds of kHz. This can result in very high dI/dt and dV/dt waveforms. Both the peak and rms currents in the snubber components can be very high. The result is that snubber performance is increasingly affected by parasitic elements (primarily resistance and inductance) which unfortunately tend to increase with power level because the physical size of the snubber components must increase to accommodate higher currents and voltages. The problem of parasitics becomes more acute as the power level is increased. In general, the higher the power level, the more important snubbers are to reliable circuit operation but the more difficult they are to implement. The key is very careful component choices and circuit layout.

We will use the combination snubber shown in figure 6-1 as an example. This is a fairly complex example but it serves to introduce all the elements normally used in snubbers: resistors, inductors, capacitors and diodes. Other types of snubbers will of course have somewhat different component stresses but the component considerations will be very much the same. Other examples such as the RC-snubber will be introduced as needed.

Keep in mind that the effect of the parasitic components will depend on the actual circuit and the operating power level. In the examples discussed here we will be operating at only one power level.

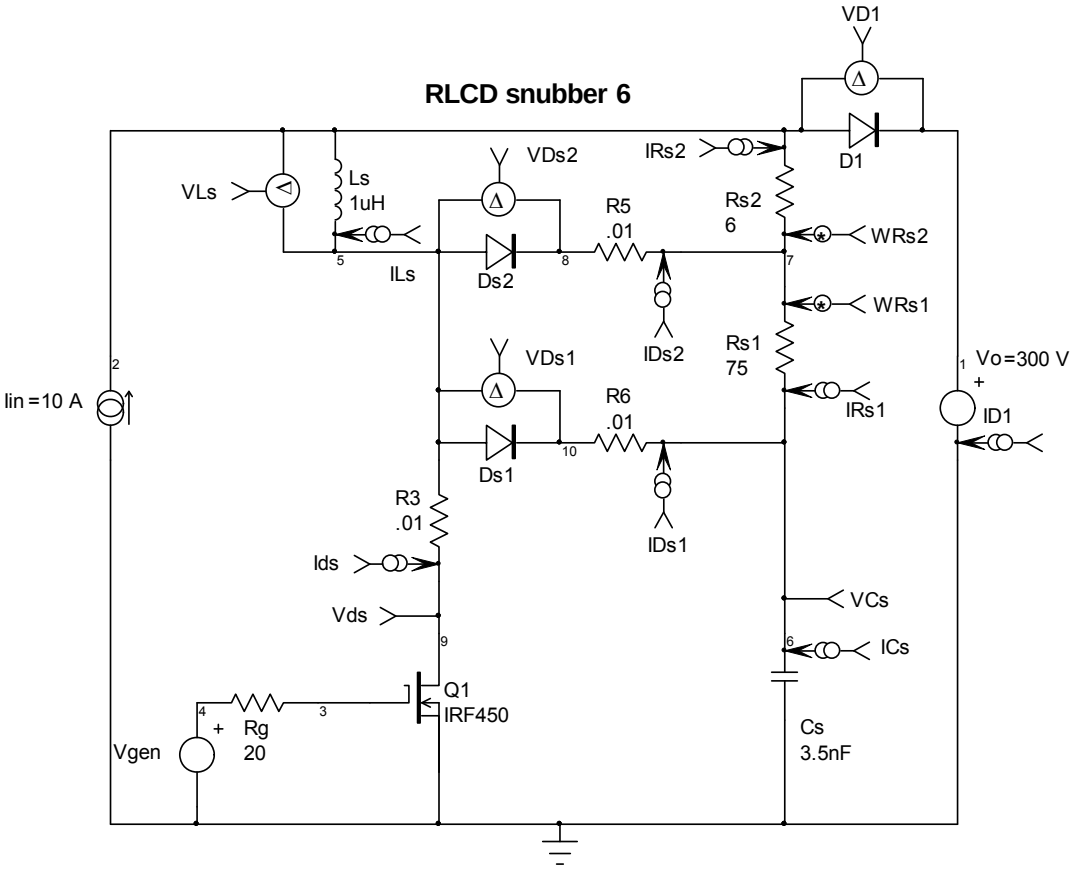


Figure 6-1, combination snubber example for component selection.

The model in figure 6-1 is very busy with multiple voltage, current and power measurement points. These are needed to determine the component stresses and are a reflection of the kind of measurements that would be made in an actual circuit. The switching frequency for this example will be 400 kHz and the duty cycle (D) of Q1 gate drive equals 0.20. The actual or effective duty cycle of the switch will depend on the characteristics of Q1 and the effect of snubber stretching turn-off time (see the discussion associated with figure 4-18). The converter will be delivering about 2 kW to the output. Average and rms values for currents, as well as the frequency spectrum will be calculated using these values of duty cycle and output power. Peak, average and rms values for waveforms will be given in text boxes on the waveform figures.

What is needed are the maximum voltage and current stresses on the snubber components and an estimate of the power dissipation in each component. In most cases the worst case voltage and current stresses do not occur simultaneously at a single operating point. In practice you will need to look at several different operating points: at the very least, full output load at high and low input voltage. You may also have to consider overload or fault conditions if you need the circuit to work through these events, at least for short periods of time. For this example we will be looking at only one operating point but the procedure is applicable at all operating points.

Diode selection

The current and voltage waveforms for the snubber diodes (Ds1 and Ds2) are shown in figure 6-2. We see that the peak reverse voltages are a bit less than Vo (300 V in this example). Allowing for normal derating we would chose diodes with a rating of 400 V or more. One of the key points to notice is that both diodes switch in the discontinuous current mode: i.e. the current through the diode is zero or very nearly so, before the voltage across the diode reverses. This means there is minimum stored charge and reverse recovery is relatively benign. This type of switching is typical of most (but not necessarily all!) snubber circuits and has the important effect that super fast diodes, even at relatively high switching frequencies, are usually not needed for snubber diodes. This doesn't mean that any old slug of diode can be used but there is usually no point in using the fastest and most expensive diodes. In this case diodes with reverse recovery times of 100 to 200 ns would be adequate.

Another feature of the current waveforms is that they are narrow, high amplitude pulses. The average currents are quite small (see text box on the graphs) but the peak currents are much larger and the rms current values are two to four times the average current. The diodes should be chosen with the rms current in mind rather than average. Ratings for the diodes will also be affected by the acceptable power loss in the diode. A larger diode will have a lower forward voltage drop and lower loss but generally cost more.

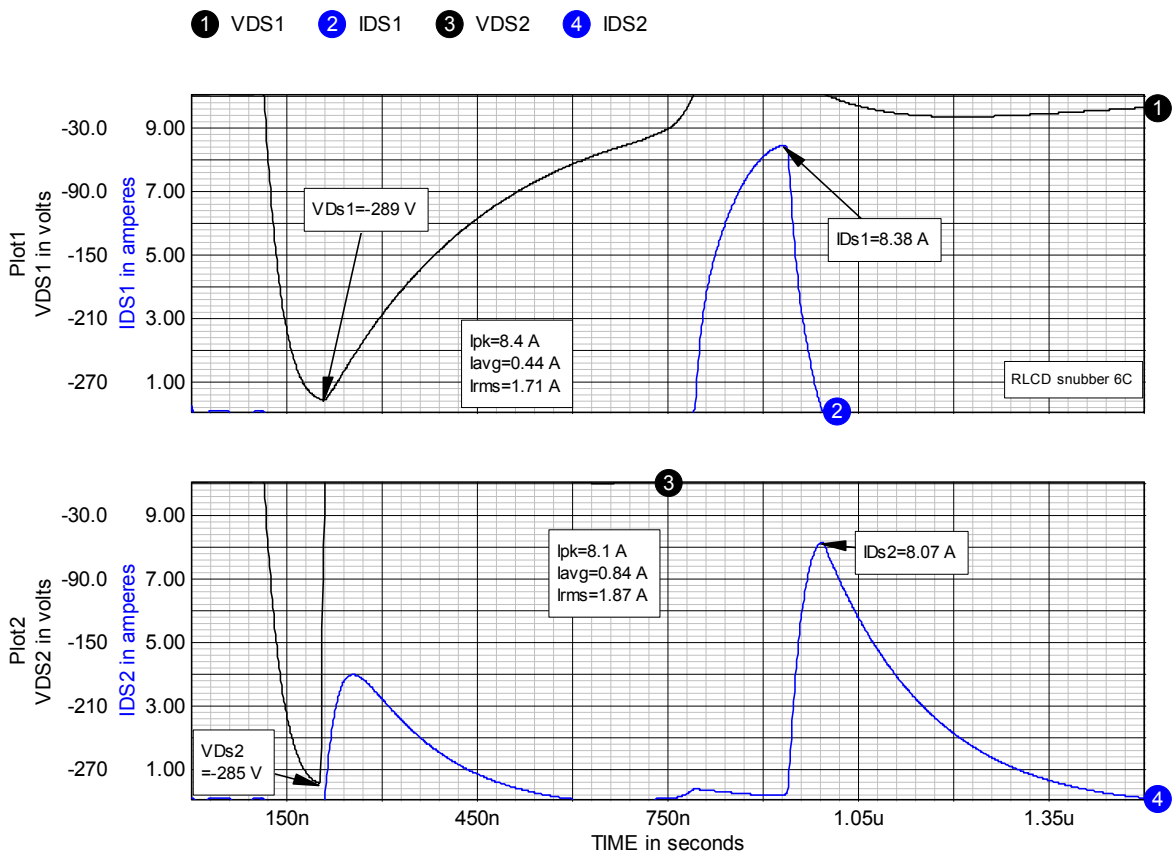


Figure 6-2, Ds1 and Ds2 voltage and current waveforms.

Ls design

The voltage and current waveforms for Ls are shown in figure 6-3. The current in Ls is a combination of a pulse with a rapidly rising leading edge and a DC component. The frequency spectrum associated with the current pulse, which is also a reflection of core flux, is shown in figure 6-4.

Ls is a non-trivial design challenge. It has both high DC and high frequency, high amplitude harmonic currents in the winding and must be designed accordingly. For small values of inductance (roughly 100 nH or less) an air-core inductor is sometimes used. This can be a simple solution but the external fields associated with air-core inductors must be kept in mind. In most cases Ls will be wound on a ferrite core with an air gap and careful attention given to minimizing eddy and proximity effects within the winding.

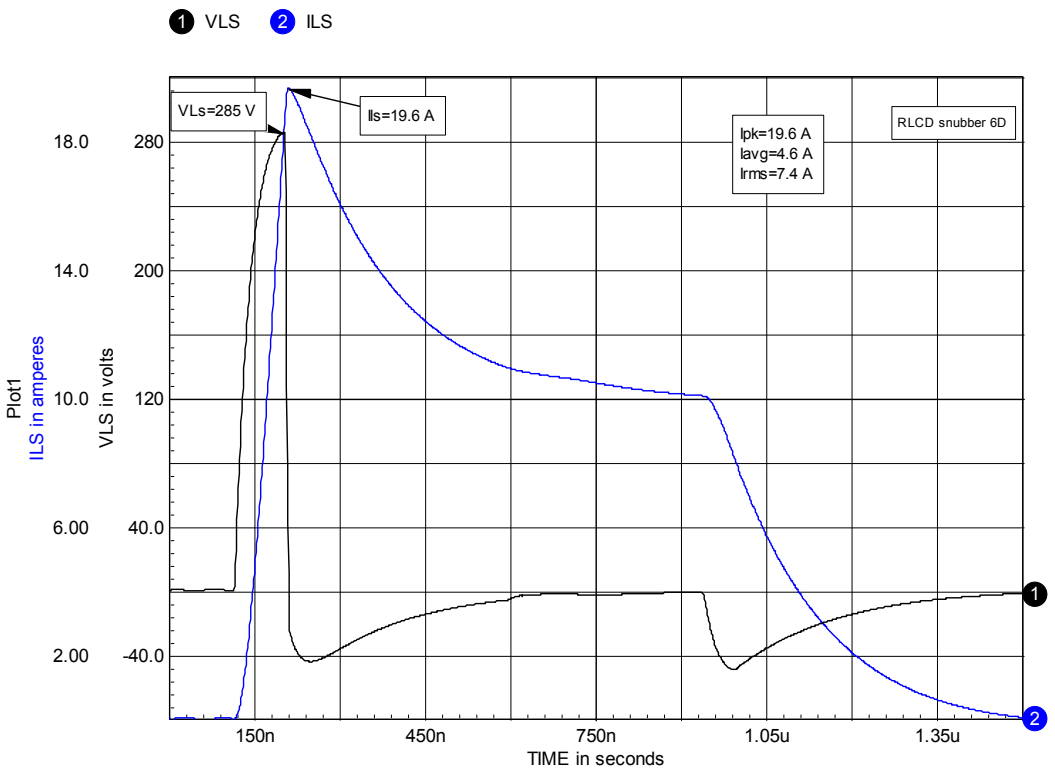


Figure 6-3, voltage and current waveforms associated with Ls.

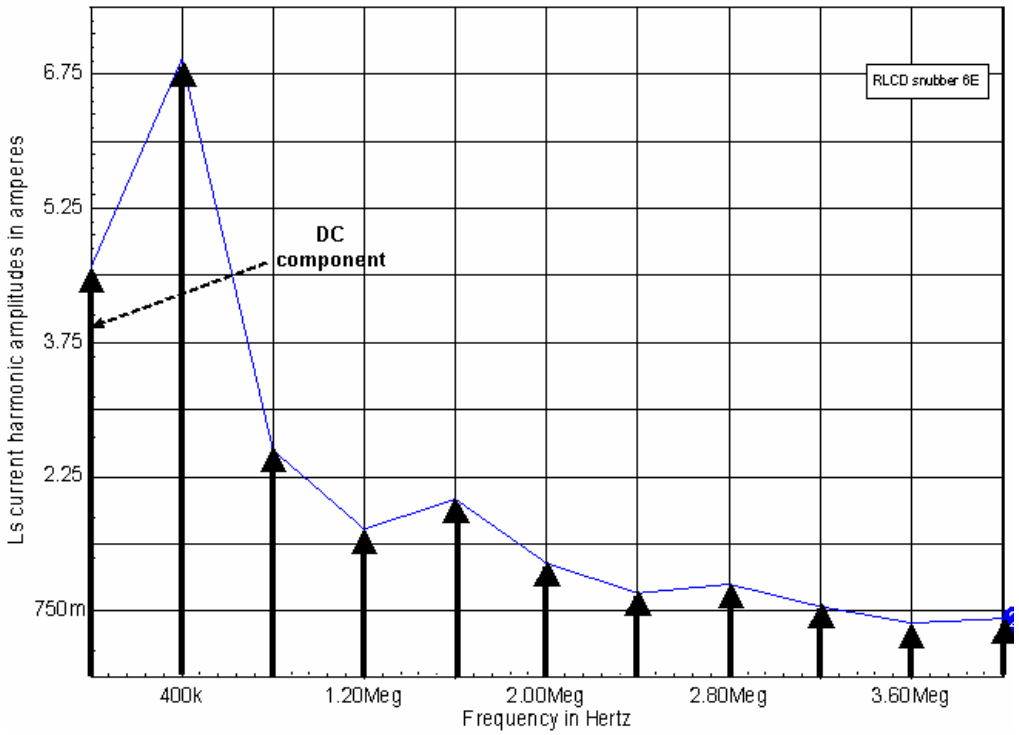


Figure 6-4, spectrum of the current waveform in Ls. Harmonic amplitudes are peak not rms. Note that both odd and even harmonics are present.

The choice of ferrite will depend on the frequency components of the current waveform. For manganese-zinc ferrites, at frequencies above 1 to 2 MHz, permeability drops rapidly. Normally the presence of the air-gap will mitigate this effect but in very high frequency converters it may be necessary to use nickel-zinc ferrites. The harmonics also appear in the core flux which can lead to higher core loss than anticipated. Eddy currents in the core and electromagnetic resonances excited at harmonic frequencies are problems which can appear at higher power levels where the size of the core for Ls is substantial.

As shown at the end of chapter 4, non-linear or saturating inductors can be used in snubbers. However, because these types of inductors are driven into saturation during every switching cycle, core loss can become an issue. The problem is the need to limit ΔB to a value which limits core loss to a acceptable value. In a ferrite this would typically be 200-300 mW/cm^3. Normally a ferrite core with an air gap is used. But the use of an air gap usually makes the remnant flux density (Br) small and typically the energy in Ls is allowed to self discharge at the end of the switching cycle. The ΔB will then be quite large, 3 to 4 kG, varying with temperature. This large a ΔB is allowable only at very low frequencies. The result is that Br must be controlled which may mean a auxiliary winding with a DC bias current or some other means to control ΔB. This is an undesirable complication.

In addition to the desired inductance, Ls will also have an equivalent series resistance (ESR) and at least some parasitic shunt capacitance. Both of these quantities need to minimized during design.

The following caution should be kept in mind:

> *In most cases Ls will be a custom design which deserves very careful attention! Especially at higher power levels, the design of Ls is not a trivial exercise. It is all too common to find casual designs running red-hot in the actual circuit with much of the efficiency improvement expected from the snubber lost in Ls dissipation.*

Cs selection

Like Ls, Cs is subject to pulse currents with rapid dI/dt and pulse voltages with rapid dV/dt. Typical Cs current and voltage waveforms are shown in figure 6-5. The harmonic spectrum for the current is shown in figure 6-6. As will be shown shortly, Cs will be self resonant at some frequency determined by the ESL (equivalent series inductance) of the capacitor in combination with additional parasitic inductance inherent in the circuit physical layout.

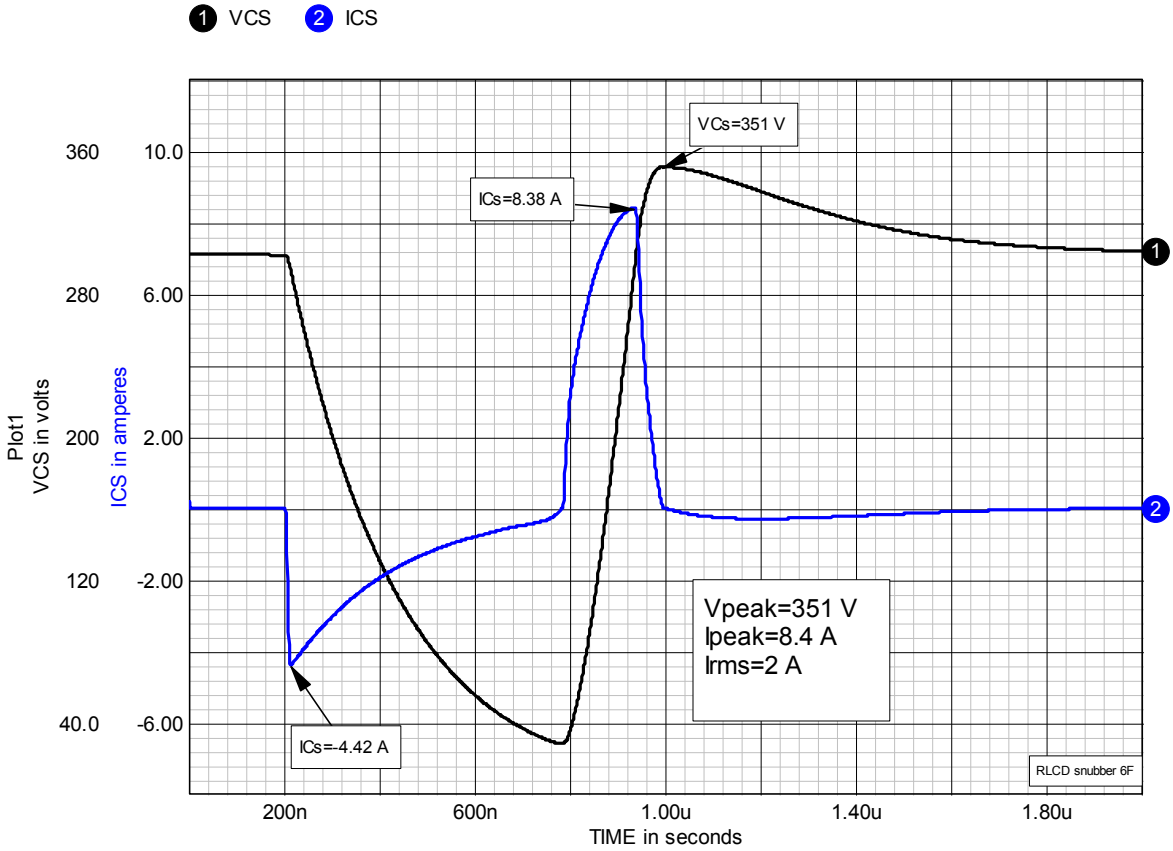


Figure 6-5, Cs voltage and current waveforms.

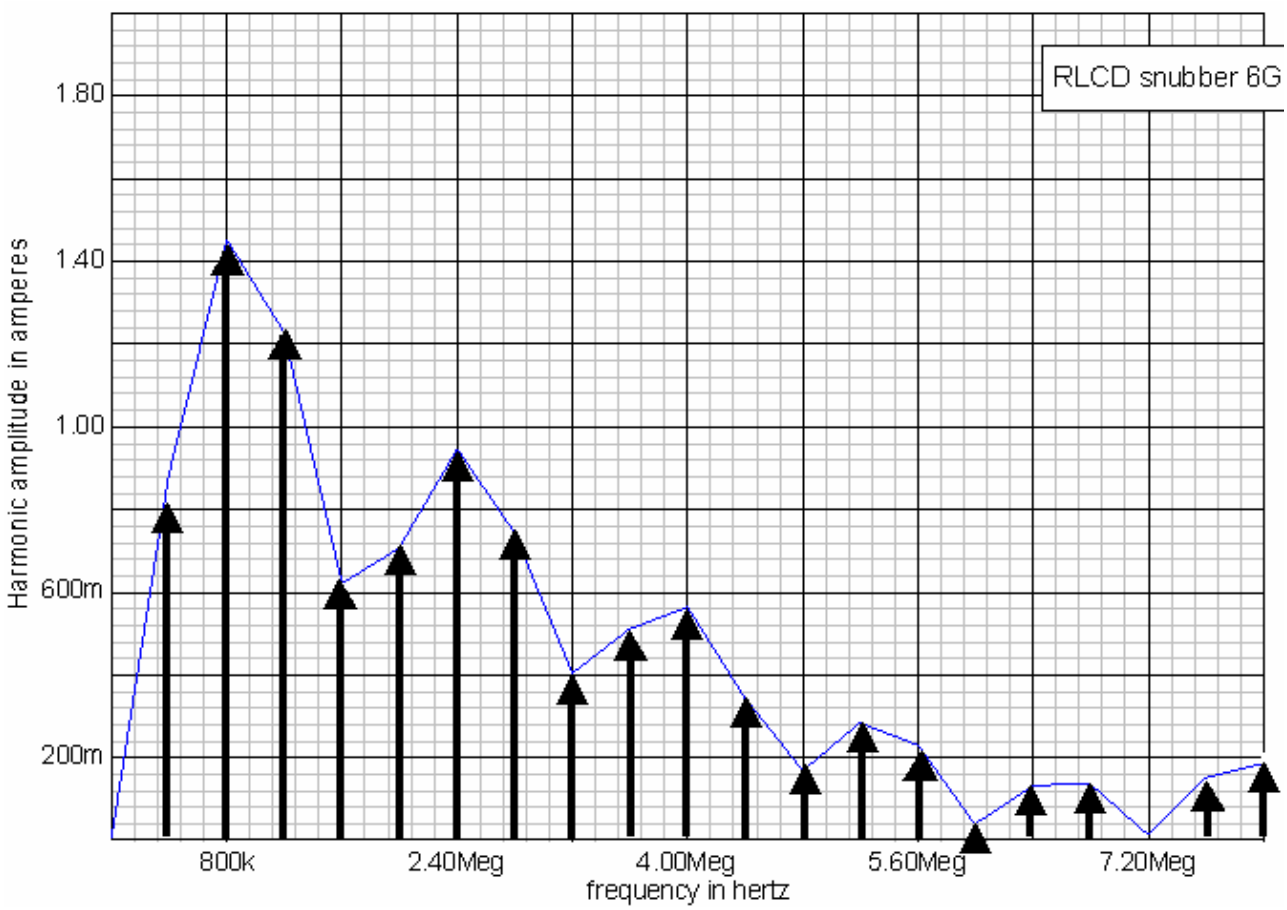


Figure 6-6, spectrum of Cs current waveforms.

Above it's self-resonant frequency, Cs becomes an inductance, the reactance of which increases with frequency. This can lead to the appearance of high frequency ringing with the introduction of the snubber that was not present before the snubber was added. This can necessitate the addition of another RC-snubber just to fix this new problem! For this reason every effort should be made to push the self-resonant frequency as high as practical.

The current in Cs has both high rms and high harmonic content. This is typical for snubber capacitors and means that Cs must be a capacitor intended for high current, high frequency applications.

In addition to the desired value of capacitance, a capacitor will also have ESL and ESR. In the case of Ls where we are usually designing the inductor ourselves, we can control these quantities. Cs on the other hand will usually be a standard capacitor selected from a catalog. It is also possible to have custom capacitors fabricated but

in general these do not deviate greatly from standard capacitors in materials or fabrication technique.

Capacitors are available with a wide variety of dielectrics but in general high frequency pulse capacitors use either mica or metal foil-polypropylene film construction.

The dipped mica capacitor shown on the left in figure 6-7 is typically used at power levels up to 1 kW and voltages ratings to 1 kV. Higher powers and voltages can be handled with mica capacitors like those shown on the right in figure 6-7.

The effect of ESL on the impedance of a capacitor is shown in figure 6-8.

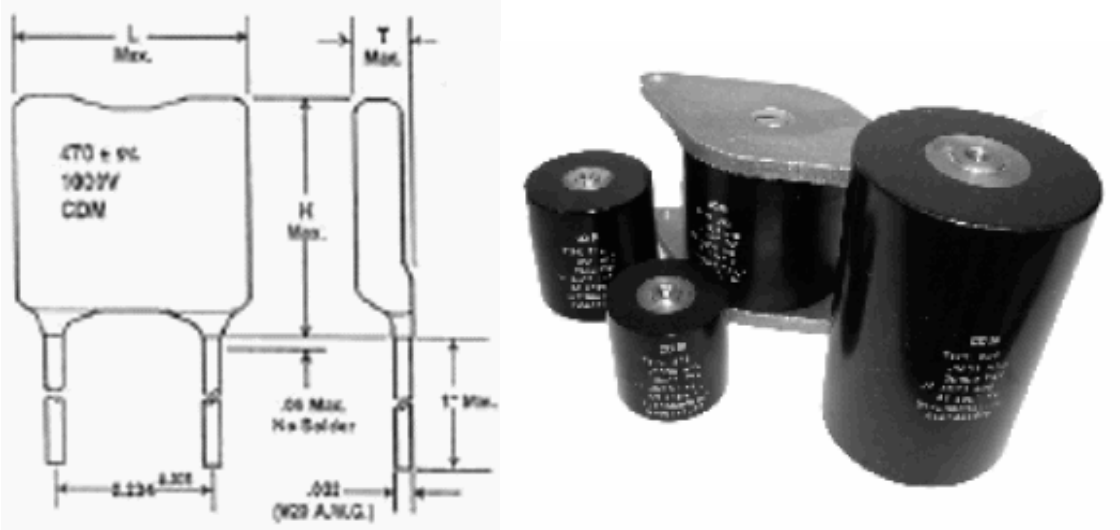


Figure 6-7, examples of mica capacitors suitable for snubbers.

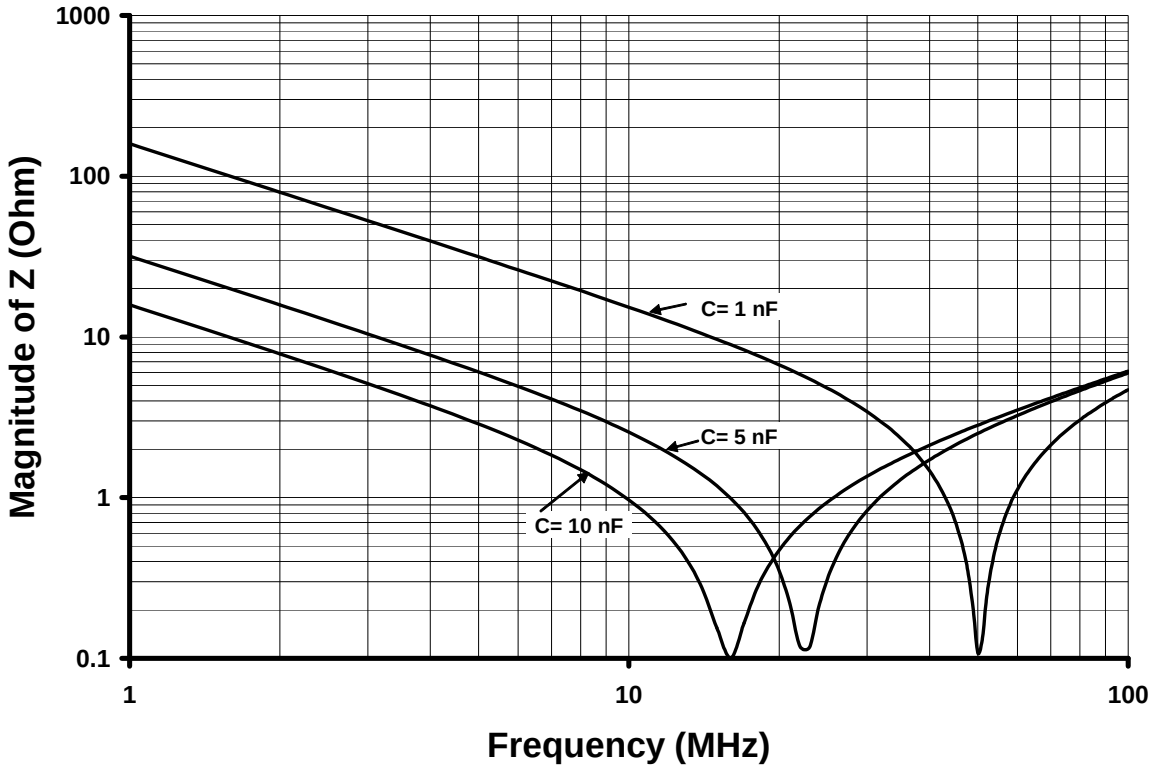


Figure 6-8, impedance versus frequency for capacitors with ESL= 10 nH.

The self resonant frequencies are in the tens of MHz which is what's needed when we look at the harmonic current spectrum of Cs (see figure 6-6 for example). Unfortunately mica capacitors, while very good at high frequencies, are also quite bulky for a given capacitance and are generally only used for relatively small values of capacitance (up to a few nF).

Axial Leaded High Frequency Pulse Capacitors

Type WPP axial-leaded, polypropylene film/foil capacitors incorporate non-inductive extended foil construction with epoxy end seals. Type WPP is rated for continuous-duty operation over the temperature range of –55 ºC to 105 ºC without voltage derating. Low ESR, low dissipation factor and the inherent stability make Type WPP ideal for tight tolerance, pulse and high frequency applications

Figure 6-9, rolled foil/film polypropylene capacitors.

Another choice for Cs would be a metal foil-polypropylene film capacitor like those shown in figures 6-9 and 6-10.

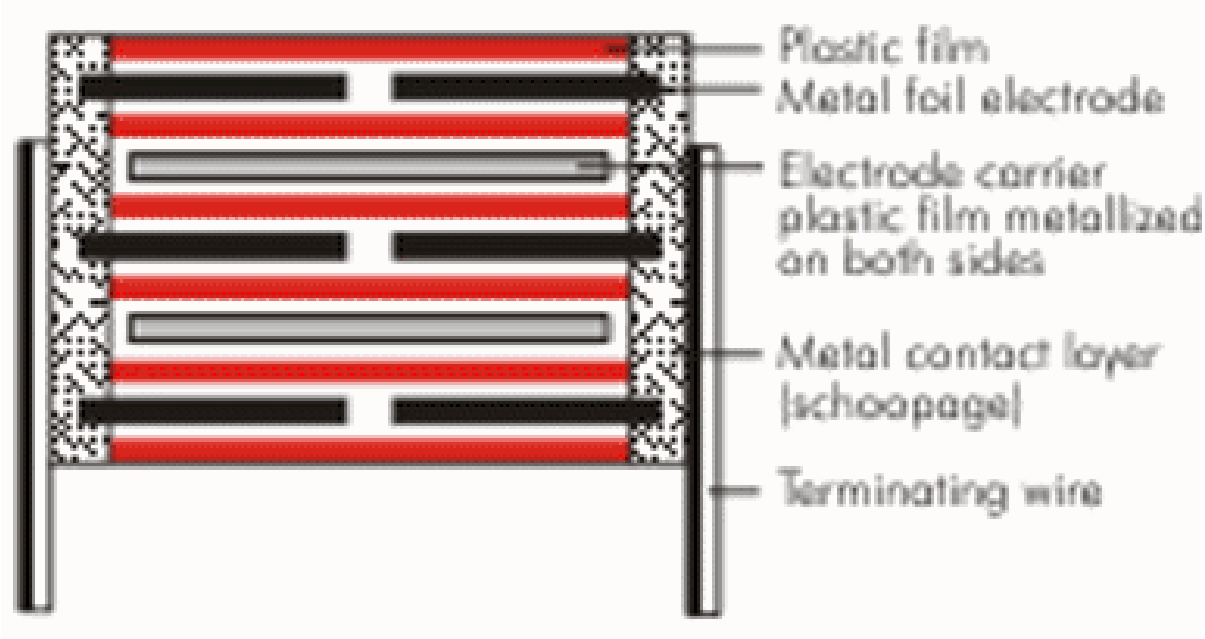


Figure 6-10, stacked foil/film polypropylene capacitors.

Rs selection

Dissipative snubbers and RC damping networks associated with energy recovery snubbers often dissipate considerable power in the snubber resistors (Rs). We can use the RC-snubber shown in figure 6-11 as an example. Note this is the same example as given earlier in figure 3-6 except that I have added L1 in series with Rs to simulate the effect of the inductance in Rs, the ESL of Cs and probable parasitic layout inductance. We will look at the effect of this inductance shortly but for the moment lets determine the power dissipation in Rs.

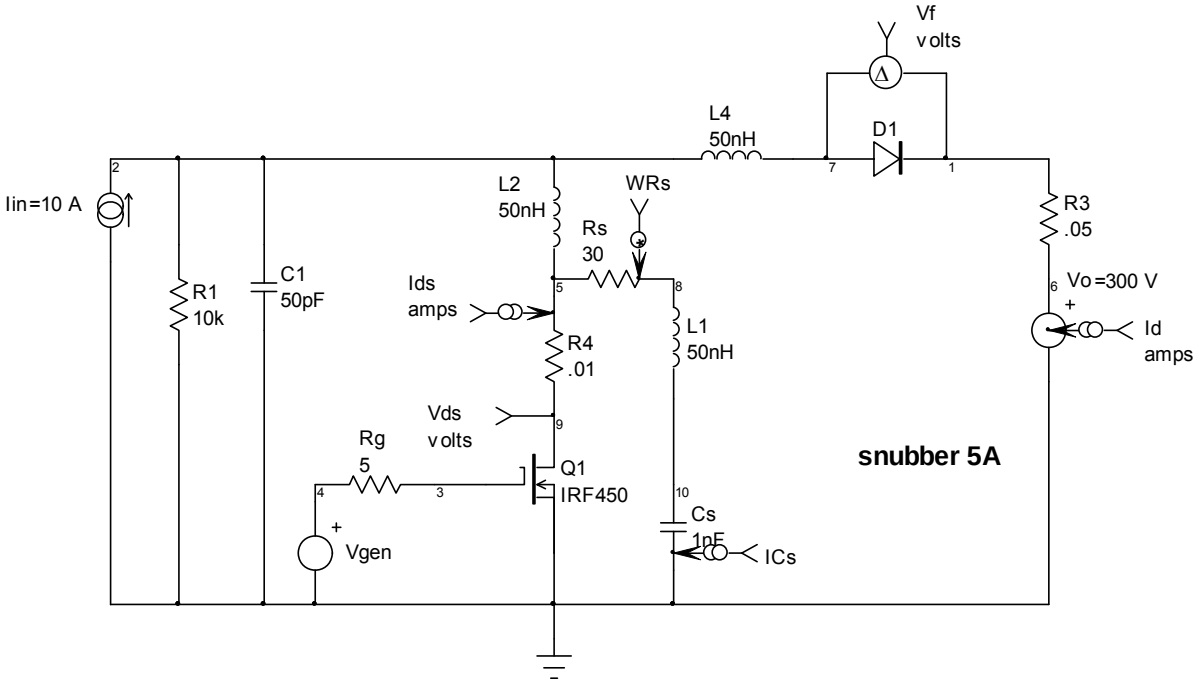


Figure 6-11, RC-snubber example.

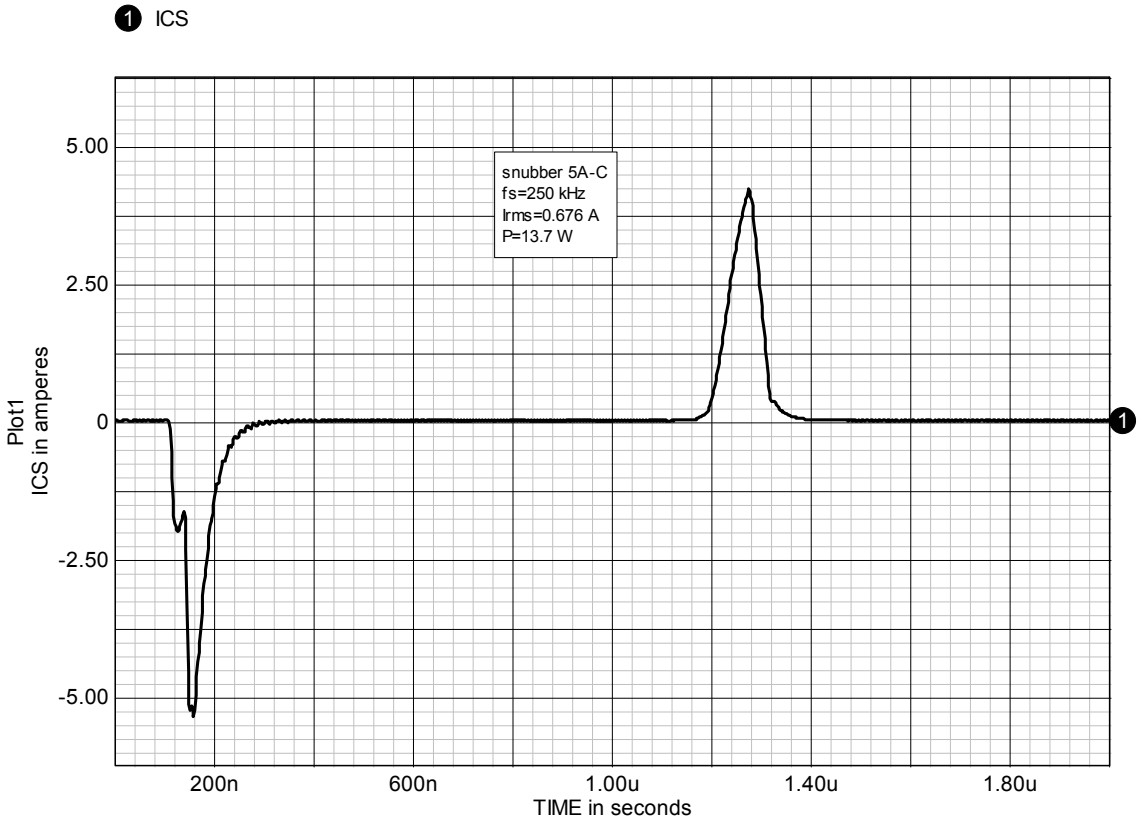


Figure 6-12, current waveform in Rs.

The current waveform in Rs is shown in figure 6-12. For a switching frequency (fs) of 250 kHz and Rs=30 Ohm, the power dissipation will be about 14 W. Normally we would use a resistor rated for about 25 W for this purpose.

Figure 6-13, shows three different power resistors we might be tempted to use for this application.

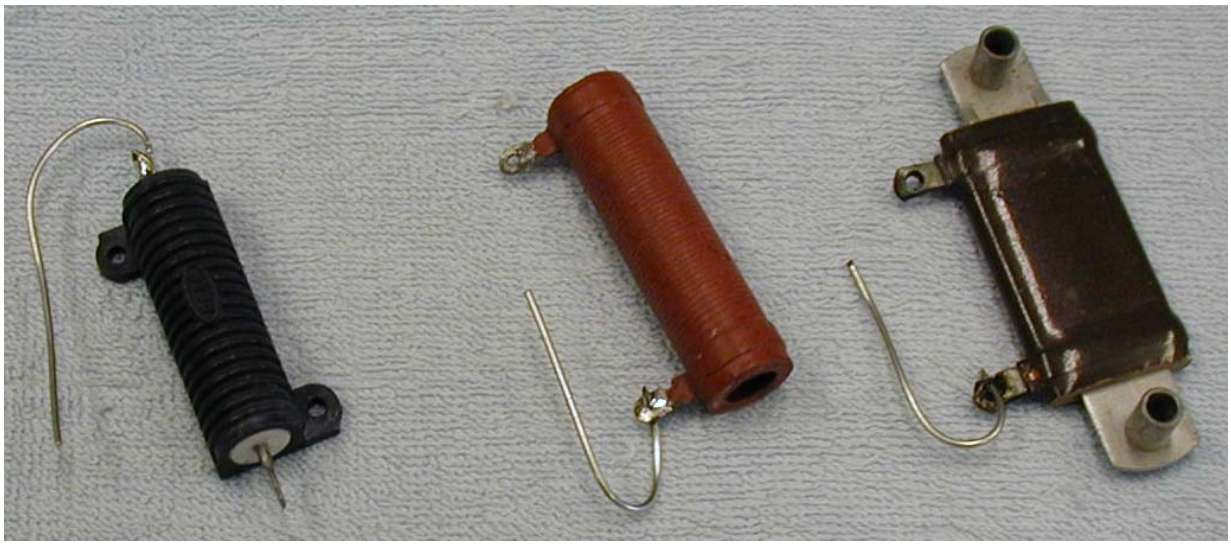


Figure 6-13, typical power resistors.

Each of these is capable of safely dissipating 14 W but there is a fundamental problem with them: their series inductance is very large. The resistor on the left has 14 uH of inductance, the center resistor has 18 uH and the resistor on the right has 22 uH. As we will see shortly, this large a value of series inductance will completely disable the RC snubber. For RC damping networks it is necessary to use non or at least very low inductance power resistors. Low inductance power resistors are available and it is also possible to parallel 2 W carbon composition resistors, at least for dissipations up to 10 W or so. There are some advantages to using parallel resistors which include better surface area to volume ratios which make cooling easier and lower net inductance.

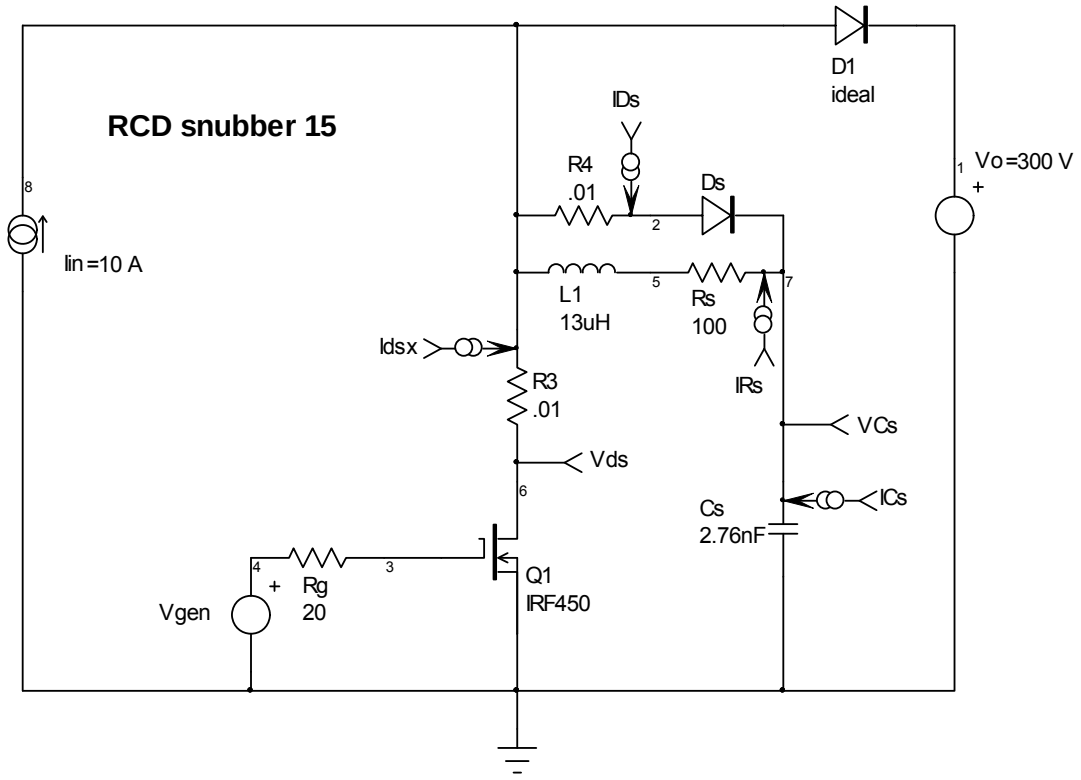


Figure 6-14, series inductance of Rs (L1) added to the model.

On the other hand, when Rs is the discharge resistor for a capacitive turn-off snubber, like that shown in figure 6-14, series inductance in Rs can actually be useful by delaying the rise of the reset current pulse superimposed on Ids at Q1 turn-on. The resulting waveforms shown in figure 6-15.

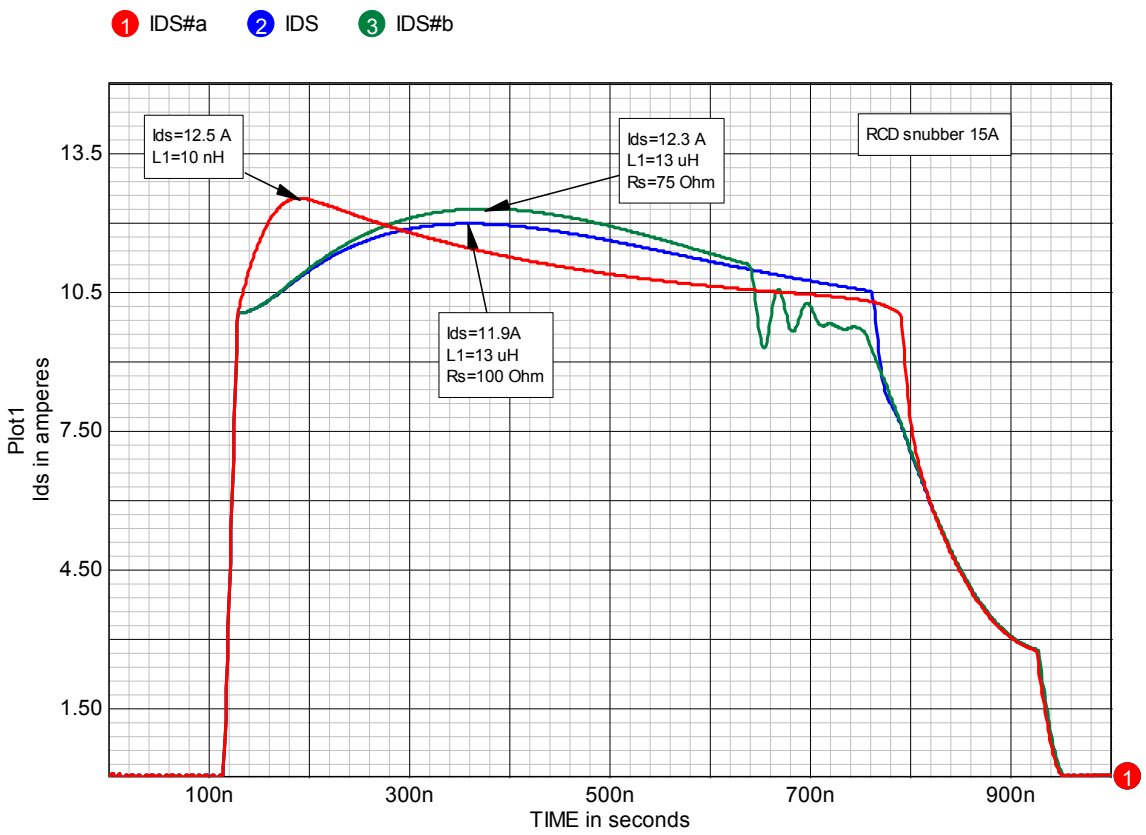


Figure 6-15, Ids current waveform with and without Rs ESL.

The useful value for L1 may be limited by the minimum on-time of Q1 which determines the minimum time available for Cs discharge. We could reduce the value of Rs somewhat as indicated by the third waveform where Rs=75 Ohm. In this case Cs is discharged sooner but all the energy in L1 has not yet been discharged. The result is the discontinuity (with some ringing) where L1 stops discharging into Q1 but continues it's discharge through Ds.

Effect of parasitic L on snubber behavior

In chapter 2 we saw that parasitic L and C in the circuit could lead to voltage and current spikes as well as ringing waveforms that generated EMI. These problems are often the primary motivation for using snubbers. Unfortunately these parasitic elements, particularly series inductance, which are inherent in component packaging and circuit layout, may interfere with the operation of the snubber. The

tools we use to minimize this problem are our choices of component packages and the physical circuit layout.

In this section we will look at the magnitude of the effects on example snubbers to get a feeling for how small we need to keep parasitic inductance to maintain proper snubber function. In the next section we will examine package selection and layout techniques which minimize parasitic inductance. We will use figure 6-11 for the first example.

Figure 6-16 gives a Vds waveform comparison with and without the RC-snubber.

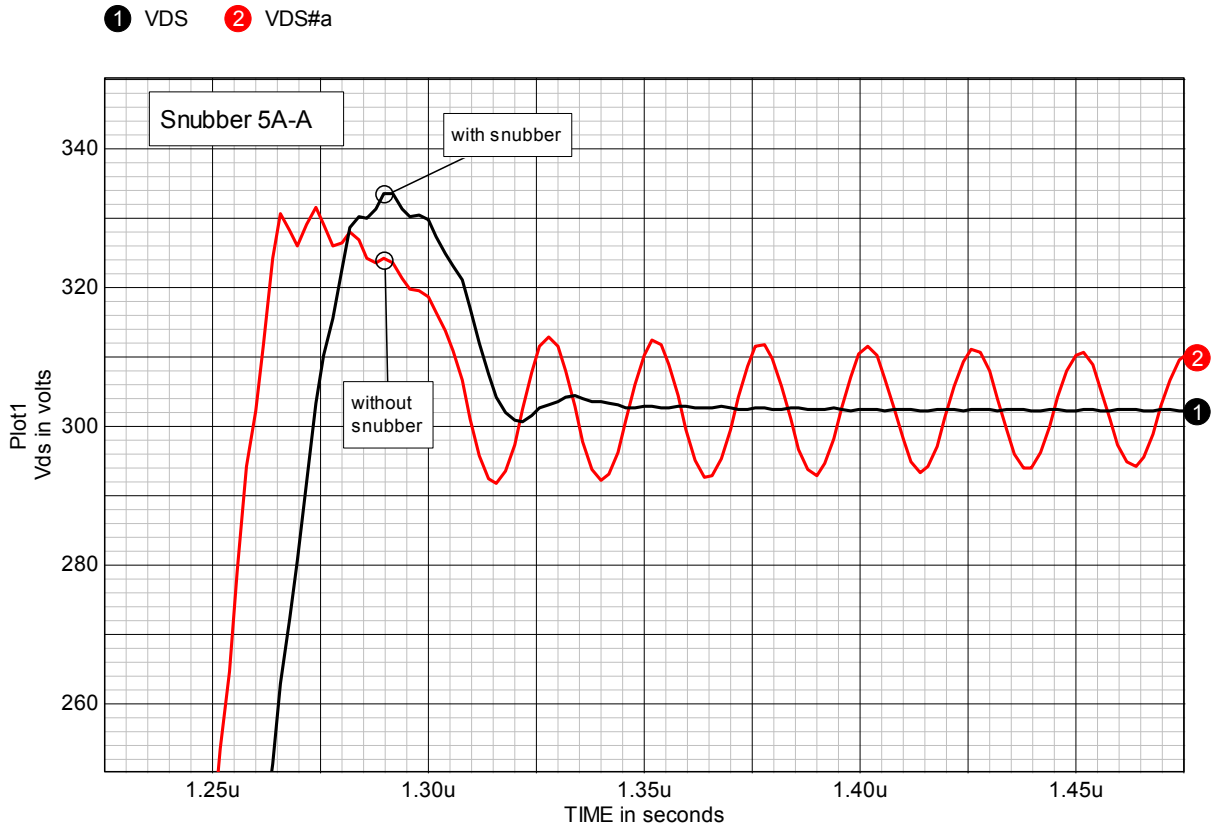


Figure 6-16, Vds waveform with and without the RC-snubber.

Without any parasitic inductance the snubber is very effective in damping the voltage ringing. Now let's look at what happens as we increase L1 (the ESL of Rs) from 5 nH, to 50 nH and then to 500 nH. The resulting Vds waveforms are compared in figure 6-17.

In this example, parasitic inductance up to 50 nH has little effect but by the time we get to 500 nH the snubber has ceased to be effective. Obviously the power resistors in figure 6-13, which have more than 10 uH of inductance, are not usable in this application.

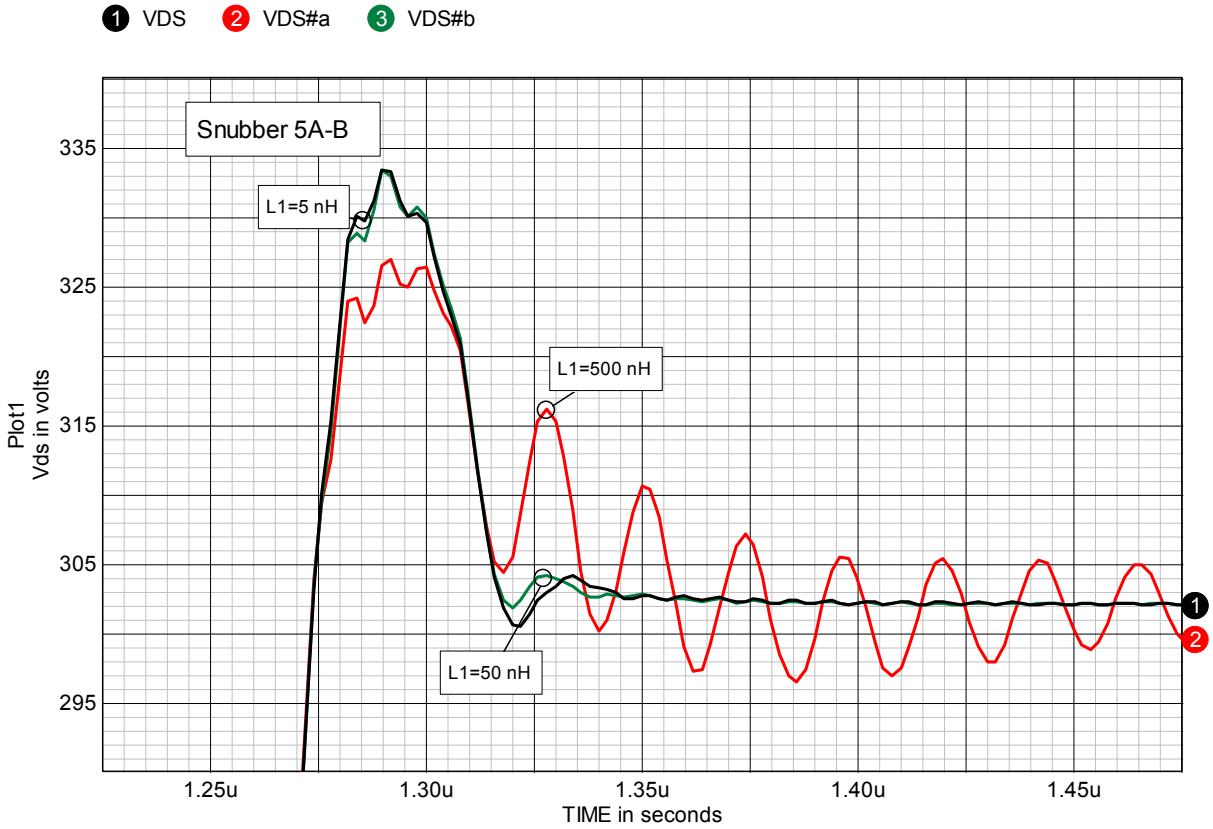


Figure 6-17, comparison of Vds waveforms at turn-off for three values of parasitic inductance (L1): 5 , 50 and 500 nH

Going back to the snubber circuit in figure 6-1. The normal discharge path for Rs1 includes an inductance (Ls) so some parasitic inductance in Rs1 is probably not a problem in the light of the previous discussion. But, Ls has to discharge through Rs2 and inductance in that resistor may be a problem. Vds waveforms for several values of inductance in series with Rs2 are shown in figure 6-18.

Again we see that relatively small values of inductance has only a small effect but in this example 500 nH doubles the amplitude of the voltage spike (above Vo=300 V). It's pretty clear that while we may tolerate some inductance in Rs1, we have to be more careful with Rs2.

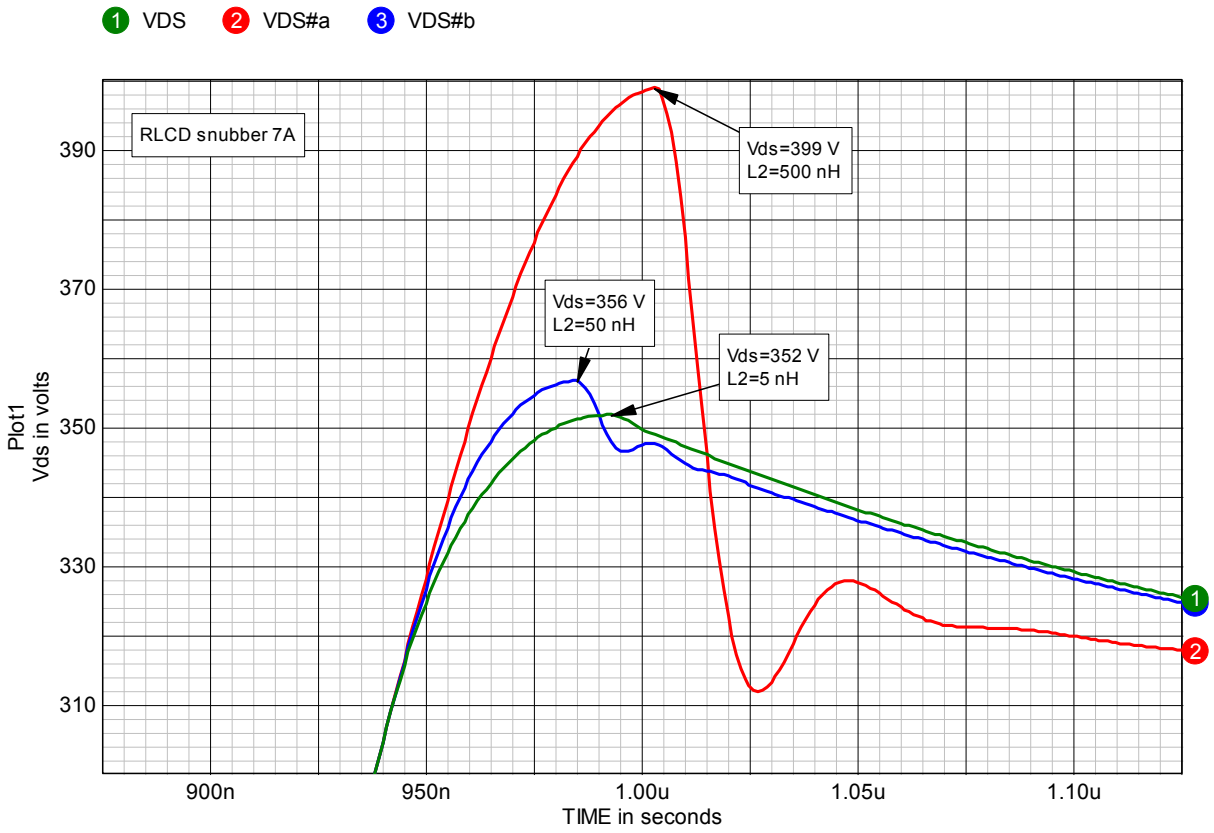


Figure 6-18, effect on Vds voltage spike at Q1 turn-off of three values of parasitic inductance (L2): 5, 50 and 500 nH.

As another example (staying with figure 6-1), suppose we have parasitic inductance (in the form of ESL and layout) in series with Cs. Figure 6-19 compares the Vds overshoot at turn-off for Cs ESL equal to 5 and 500 nH.

ESL in Cs does not appear to have serious consequences for Vds at Q1 turn-off. The reason is that the voltage overshoot is primarily determined by the discharge of Ls through Rs2 and the ESL of Cs has only a second order effect. Parasitic inductance in series with Ds1 would show an effect much like that for Cs ESL. With the exception of parasitic inductance in Rs2, this snubber circuit is relatively tolerant of parasitic inductances.

This example of using a SPICE model to determine the effect of parasitic inductances at different points in the circuit demonstrates a way to estimate the relative importance of circuit layout in different areas. With this kind of information the layout can be modified to improve snubber effectiveness.

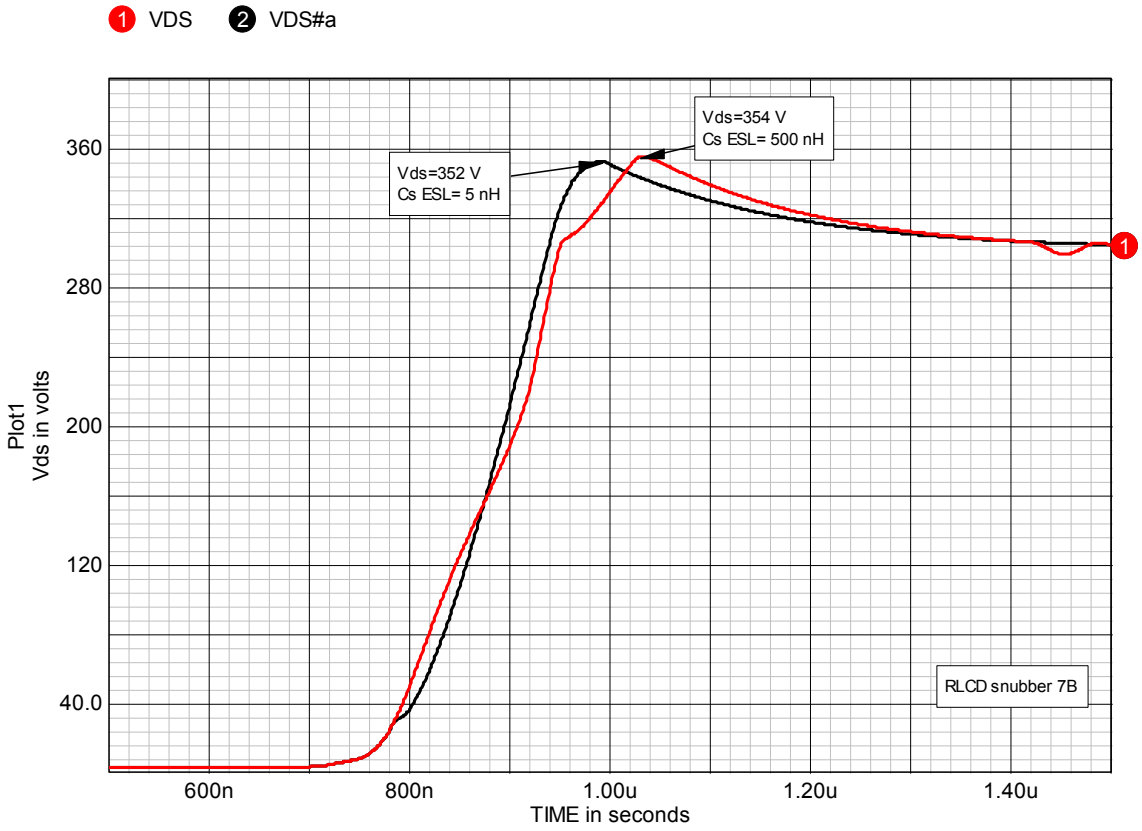


Figure 6-19, effect of ESL in Cs on Vds overshoot at Q1 turn-off.

Package and layout inductance

The ESL of snubber capacitors can be determined from the series self resonant frequency and the capacitance using the following equation.

$$L = \frac{1}{4\pi^2 f_r^2 Cs} \qquad (6\text{-}1)$$

Where f_r is the self resonant frequency and Cs is the capacitance measured at a frequency well below f_r. Using the value for Cs measured at a frequency well below resonance works well for snubber capacitors because the dielectric constant of dielectrics commonly used in pulse rated capacitors (mica and polypropylene) has relatively little dispersion (variation with frequency). A vector network analyzer (VNA), with careful fixture calibration and the shortest possible leads, is the best way to make these measurements but by no means the only way.

The ESL associated with a snubber capacitor will increase with the size of the capacitor. Four examples of typical snubber capacitors are given in figure 6-20. Table 6-1 shows measured values for the capacitors in figure 6-20.

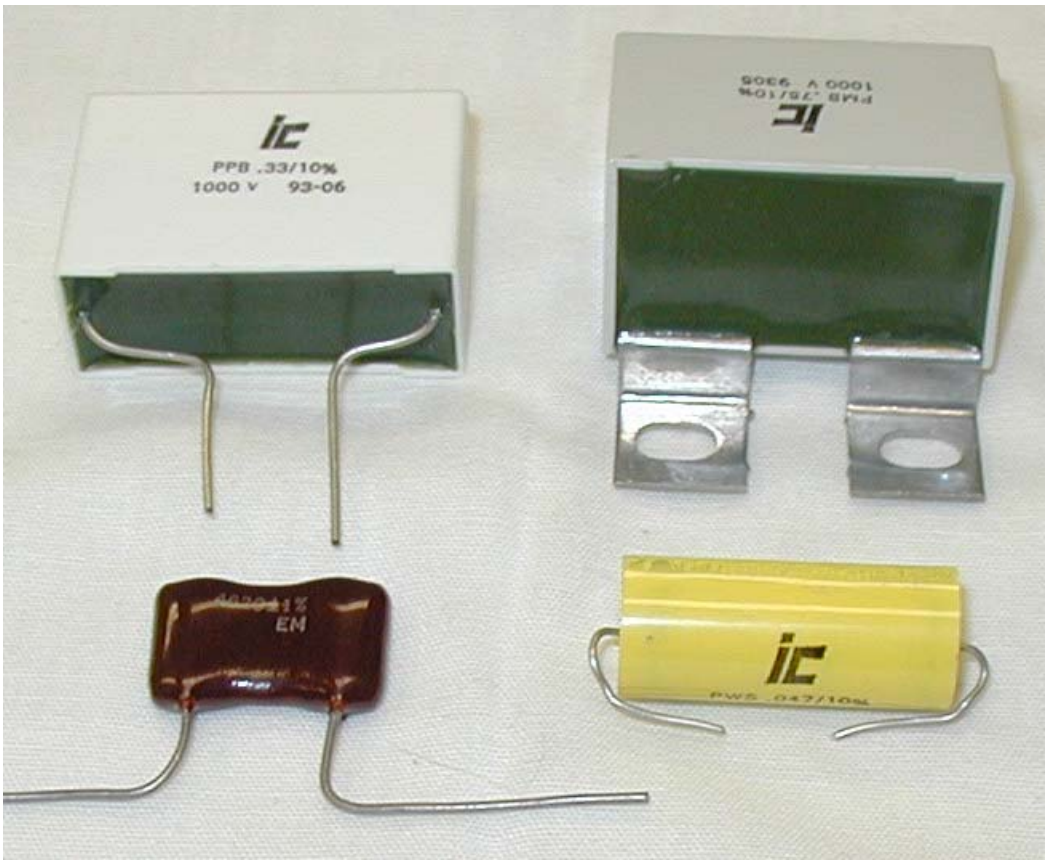


Figure 6-20, typical snubber capacitors. A dipped mica, an axial leaded polypropylene-foil and two rectangular polypropylene-foil capacitors.

Table 6-1, capacitance and ESL for the capacitors in figure 6-20

capacitor	measured capacitance	series resonant frequency	ESL
dipped mica	4615 pF	16.5 MHz	9 nH
axial leads	0.049 uF	4.6 MHz	24 nH
small rectangular	0.338 uF	1.5 MHz	33 nH
large rectangular	0.751 uF	1.05 MHz	31 nH

These are quite small values and it would appear that capacitor ESL is not a problem. That however, is misleading.

> *The values in table 6-1 are only for capacitors with the shortest possible leads. The VNA measurement plane is right at the capacitor. When installed in a real circuit across a switch, perhaps in series with a resistor or a diode, the effective layout inductance can be much larger than the values shown.*

It is important to minimize additional parasitic inductance due to the physical layout. Besides minimizing cross sectional area of any high dI/dt loops and using wide conductors, you can also use multiple parallel components to reduce inductance. A subsidiary benefit of paralleling can be better component cooling. In an application where multiple parallel switches are employed, the snubber components should be divided up so there is a snubber directly across each switch in the assembly.

It can be very helpful to mock-up the actual layout of the snubber and switch assembly, using small inductors to represent the packaging inductance of any diodes or switches in the circuit. You can also add small capacitors to represent the parasitic and junction capacitances. By judiciously shorting elements you can simulate both on and off-states of the various semiconductors for network analyzer measurements. Various layouts can be tried to determine the most effective. This exercise can be very revealing and well worth the trouble, especially in high power applications where snubber function

is critical but component sizing makes it difficult to minimize parasitics.

Comments on measurements

Earlier in this chapter and in other chapters, I have alluded to measurements which are needed as part of the snubber design process. In this section I'm going to repeat some of those comments and expand on them.

For some measurements I will be suggesting fairly advanced test equipment which may be available in large corporate laboratories but not in the laboratories of smaller organizations, particularly in developing countries. For this reason in addition to the more advanced test equipment, which is great when available, I will be suggesting much simpler, if somewhat more time consuming, ways to make the measurements.

We will use the circuit shown in figure 6-20, which indicates typical converter measurements, as a reference for the following discussion.

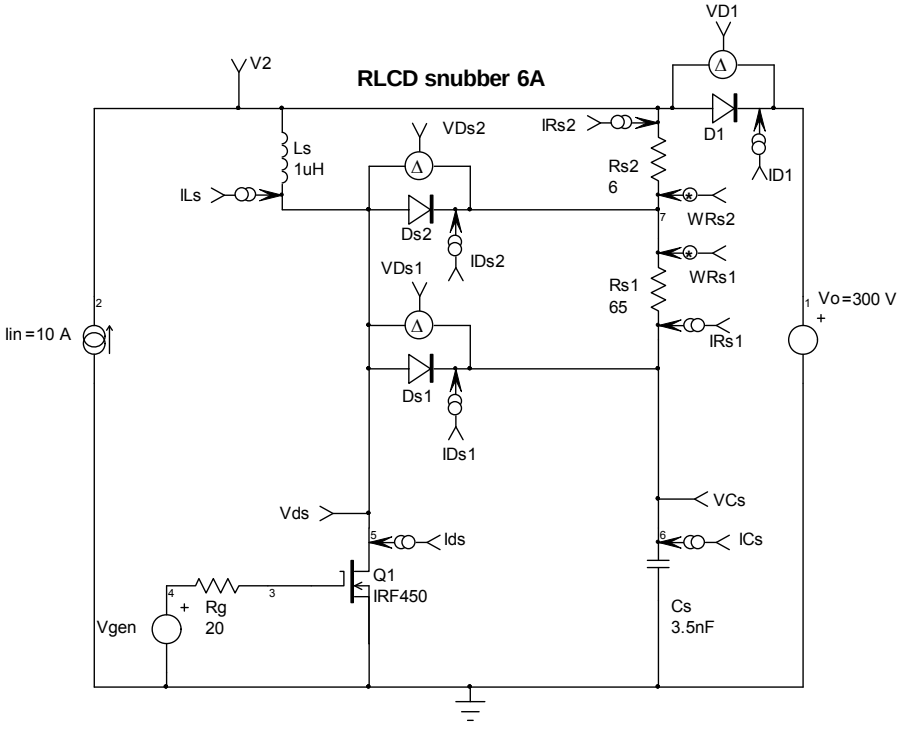


Figure 6-20, typical measurement points in a converter.

Voltage and current measurements serve several purposes and will normally have to be repeated as the snubber design or any circuit layout changes and/or testing proceeds. This is usually an iterative process.

Initially we need to determine the voltage and current stresses on the semiconductors and any possible EMI from ringing voltage and/or current waveforms before snubbers are added to the circuit. This initial assessment should be done on a unit as close to the final configuration as possible. This is important because if there are substantial changes between the test or breadboard units and the final assembly, you may waste time fixing a problem which does not exist in the final unit but miss one that does. This is the point to carefully review the circuit physical layout and try to minimize the work the snubbers will have to do: i.e. minimize the energy managed by the snubber(s) with good layout practices.

It's necessary to measure the current through each semiconductor and the voltage directly across the package leads in time synchronicity. This is normally done with an oscilloscope and various probes. You need to be careful to take into account the time delays inherent in current probes. It should be pointed out that while a modern oscilloscope with waveform multiplication capabilities, graphical print-out, etc, is very nice for these measurements, it is not necessary. For most applications, a old vacuum tube oscilloscope with a bandwidth of 20 MHz is perfectly adequate. The use of a less advanced oscilloscope just means that the engineer will have to spend a bit more time deciphering the circuit operation.

Circuit waveforms not only show the component stresses which snubbers may need to address but can also provide a good estimate of the power loss in each component. This information is needed for thermal design and also is a crucial part of the overall converter power budget survey which shows where the losses are and their magnitude in relation to the overall circuit loss, usually determined from direct input-to-output efficiency measurements. This kind of survey may very well show that while the stresses on a given component are acceptable, the component loss is large enough to significantly impact the overall efficiency. While a snubber might not

be needed to control the stress, it might be helpful to improve overall circuit efficiency. In any case, this information is needed to define the desired snubber function: stress reduction or EMI reduction or efficiency improvement or some combination of all three.

Computation of device losses from the voltage and current waveforms is very easy when an oscilloscope with waveform multiplication capability is available. If this is not possible then a good estimate for the power loss can be obtained by using waveforms from a simpler oscilloscope, approximated with straight lines, and the equations in chapter 2 (2-1 and 2-2). This approach is a bit tedious but works just fine.

In addition to an initial determination of the semiconductor waveforms, it's a very good idea to go through the circuit with a probe looking at the voltage ringing at different points. This survey can be very helpful in determining the base cause(s) of the ringing and perhaps enable you to make an estimate of the parasitic inductances and capacitances present. This information is fundamental for the design of the snubber!

The following is an excerpt from the discussion in chapter 3, repeated here for convenience.

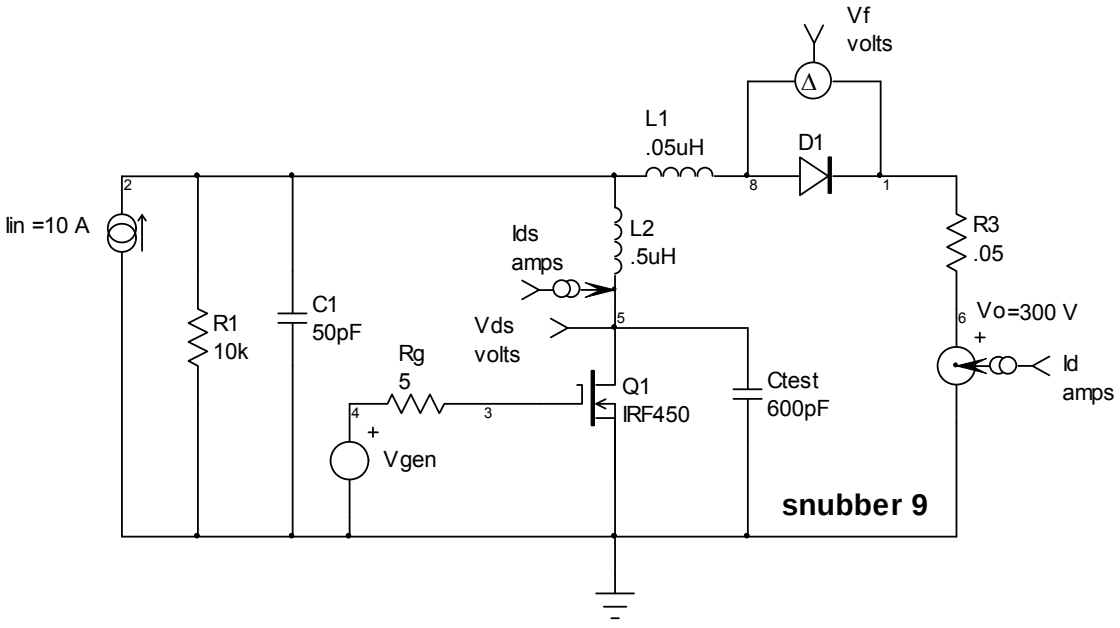


Figure 6-21, adding a test capacitor to the circuit.

It is possible to perform a test on the actual circuit to derive an approximation of the values for the parasitic elements. First we determine the ringing frequency from the ringing waveform(s) for the circuit as it stands. Then we add a known capacitance (C_{test}) across the point of interest. For example, Q1, drain-to-source, as shown in figure 6-21, and measure the new ringing frequency. The two waveforms for this example are shown in figure 6-22. In this case f_1 = 18.86 MHz (without C_{test}) and f_2 = 7.6 MHz (with C_{test}).

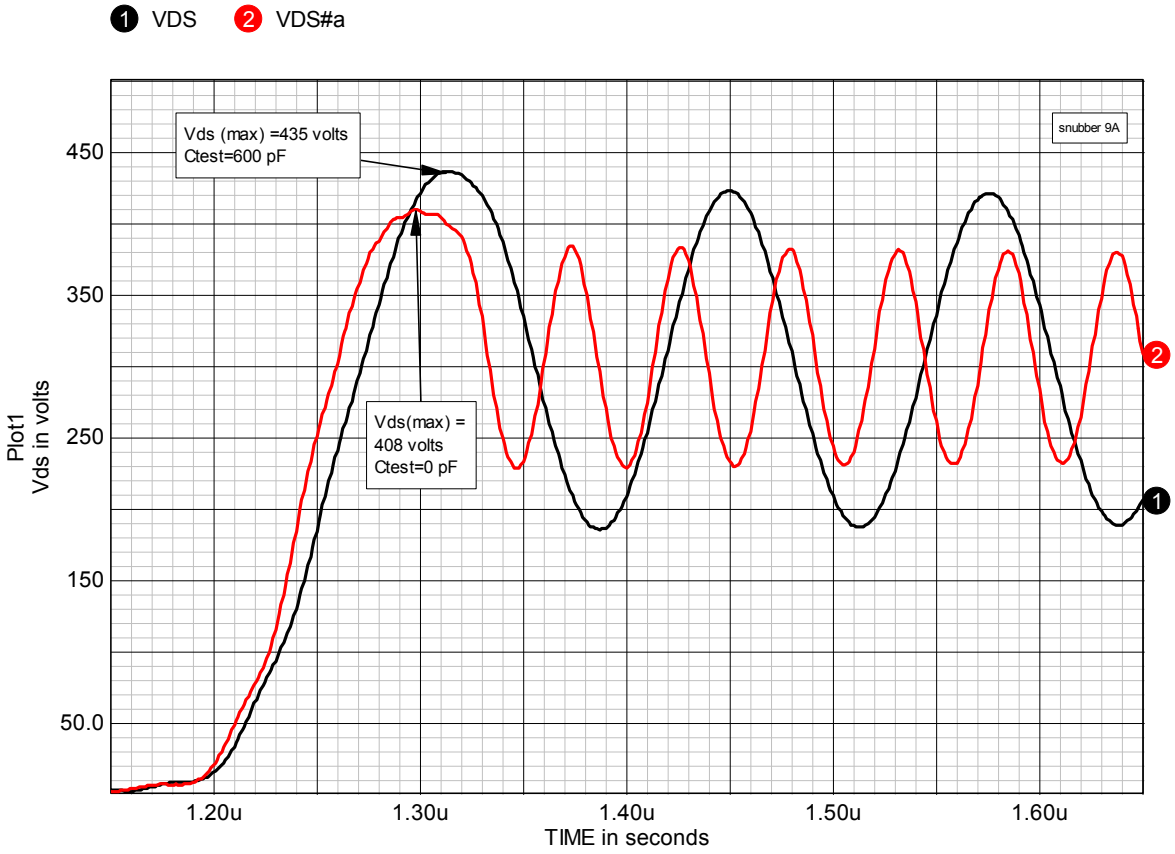


Figure 6-22, Vds ringing with and without C_{test}.

Knowing the value for C_{test}, f_1 and f_2, we can use the following equations to estimate both L2 and

$$L2 = \frac{1}{C_{test}}\left[\frac{1}{\omega_2^2} - \frac{1}{\omega_1^2}\right]$$

$$Coss = \frac{1}{L2\omega_1^2}$$

$$\omega_1 = 2\pi f_1$$

$$\omega_2 = 2\pi f_2 \qquad (6\text{-}2)$$

Equation (6-2) strictly speaking is only for the simple case of a single L and C so when we apply it to a practical circuit, we only get an approximation since the other elements in the circuit will have some effect. For example, using f_1 = 18.9 MHz, f_2 = 7.6 MHz and C_{test} = 600 pF, we get L2= 582 nH and Coss = 122 pF. Because we're using a SPICE model, we know that L2 is actually 500 nH. But, during turn-on and turn-off, L1 and L2 are effectively in series, i.e. L=550 nH. The calculated value of 582 nH is close however.

From the capacitance data for an IRF450 shown in figure 3-14, we can see that the calculated value for Coss = 122 pF is a reasonable for Q1.

This technique gives an approximation of the actual circuit values which is adequate to begin the snubber design. But we have to be careful. When there are multiple different parasitic inductances and

capacitances in the circuit, depending on the relative values, the approximation may not be so good.

Often multiple ringing frequencies will be present which complicates things. If a spectrum analyzer is available then it's very straightforward to separate and determine the different ringing frequencies. If a spectrum analyzer is not available, another possibility would be to replicate the observed waveforms with SPICE modeling by trial addition of parasitic inductances, adjusting the model values until you have approximated the waveforms in the actual circuit.

The parasitic inductance of the physical layout can often be estimated quite well using the circuit dimensions and the inductance equations from Terman [436].

A simple technique for determining the self resonant frequency of a capacitor when a network analyzer is not available is shown in figure 6-23. The generator is just an ordinary manual signal generator covering the range of interest. R1 would normally be 10 to 20 X the anticipated ESR as a starting point. The probe would be an oscilloscope or an RF voltmeter. The probe capacitance will have some effect on the resonant frequency but that is usually very small because the probe will be a few pF and the capacitors hundreds of pF or larger. Also the resonant frequency varies as the square root of the capacitance so the effect of the probe is usually very small.

You adjust the frequency of the signal generator for the minimum signal level on the oscilloscope. That occurs at the series resonant frequency.

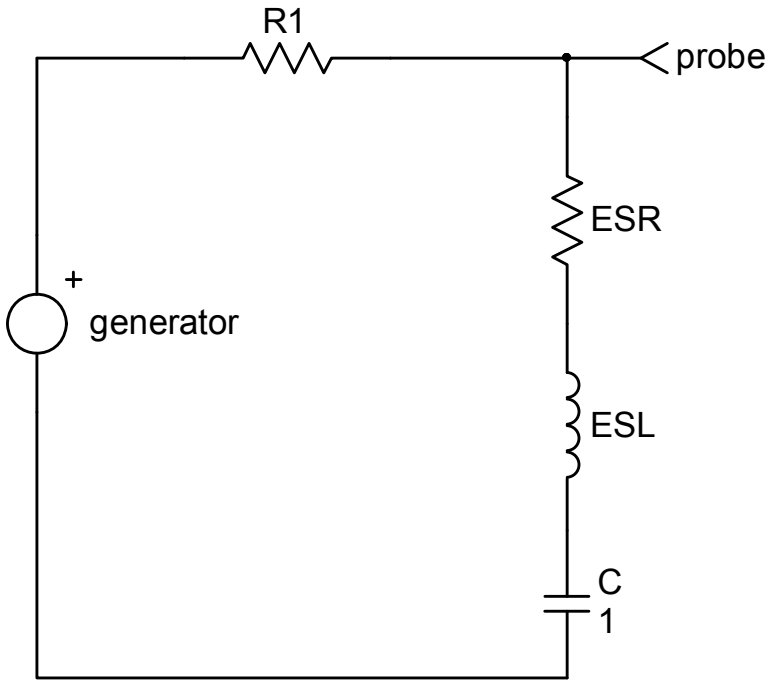


Figure 6-23, setup to measure self resonant frequency of a capacitor.

One final reminder

As stated near the beginning of this chapter, the waveform measurements we make should be done over the full range of operating conditions, high and low input line, high and low output load, etc. In general we are seeking the worst case conditions to define the requirements for the snubber.

The final step is to verify that the snubber(s) is (are) actually performing as expected over the entire range of operating conditions. All too often in the heat of battle this final step is overlooked. It's all too easy to say "oh, the voltage spike is gone!" and charge off to deal other converter issues without checking to see if the spike is really gone everywhere.

Chapter 7

Bare Bones Snubber Design

This chapter is intended for those dark and stormy nights in the lab when you need a quick solution to a snubber problem so you can move on to other concerns. With that in mind, the examples in this chapter are presented in a "do this, use this approximation," format. If you follow the directions and perhaps make some small final adjustments, you should get a snubber which performs as expected. The performance will probably not be optimized but it should be close.

You can use this chapter without reading all the other chapters in this book. However, if you take the time to read the earlier work, you will understand much better the reasoning behind the directions given here. Justification for the assumptions used in the examples to follow has been given at length in chapters 1 through 6.

For the purposes of this discussion we will assume we have a converter with some problems for which a snubber might be useful. We will work with a SPICE model of the converter and assume we have, in one way or another, estimated the values for the parasitic elements (see chapters 2 and 6). These will be added to the model. Then we will go through the model examining voltage and current waveforms and estimating power losses just as we would in a real circuit. From these waveforms we will see problems which may be addressed with snubbers.

We can then proceed to snubber design examples. Several different examples will be given:

An RC-snubber, in three variations
An RC-diode turn-off snubber
An RLC-diode combination turn-on and turn-off snubber
An energy recovery snubber

In the process we will critique the improvement in circuit performance for each example. But we will also include in the critique the undesired side effects that are introduced by the addition of snubbers to a circuit. This is a point seldom addressed in snubber discussions but is vital to the proper application of snubbers. Adding a snubber to a circuit can alleviate one problem but will very likely introduce some increase in either peak voltage or peak current into the switch. There is no free lunch in this business. You may very well have to balance the degree of improvement in one part of the waveforms against some undesirable features in other parts of the waveforms.

Getting started

The first step is to define the problem to be fixed with a snubber. This will usually appear while going through the waveform and power loss survey for various line and load conditions. This is a normal part of any converter or motor controller development. In the worst case, the problem may take the form of catastrophic device failures, which can be discouraging. The trick case is to find some operating condition at which the circuit does not self destruct immediately so you can investigate the circuit waveforms. Frequently lighter output loads or lower input voltages are tried to find such a condition.

The second step is to at least approximate the parasitic inductances and capacitances actually present in the circuit. This information is needed to determine snubber component values. Typically, device parameters like package lead inductances and junction capacitances can be found from manufacturers data sheets. The ESL (equivalent series inductance) and ESR (equivalent series resistance) of capacitors can be found from data sheet information or from a measurement of impedance and self resonant frequency. Parasitics due to layout may require some calculation and/or measurements in the circuit. Chapter 6 provides guidance in determining these values.

Example circuit

For the snubber examples that follow, we will use the boost converter shown in figure 7-1.

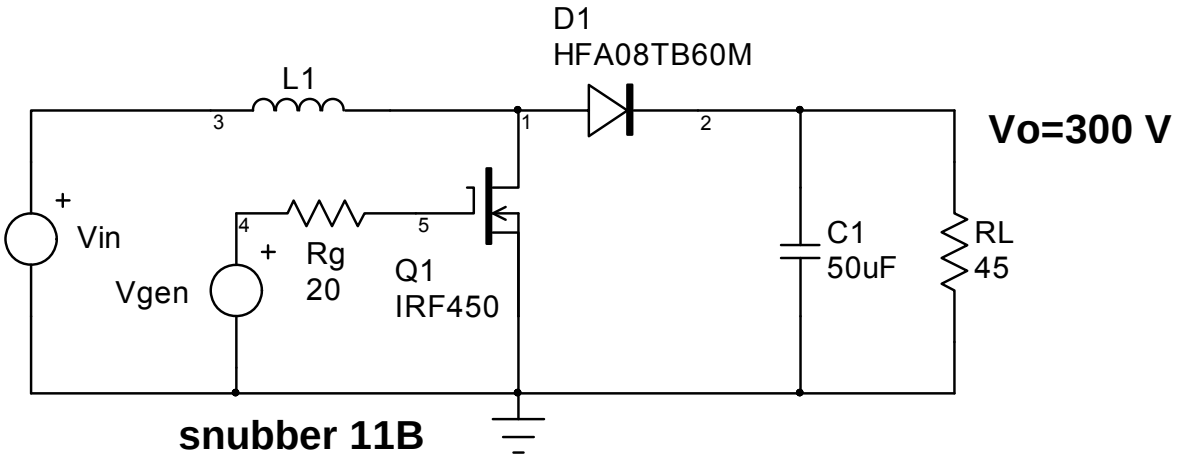


Figure 7-1, boost converter example.

This is a particular converter circuit but, as was shown in the discussion associated with figure 2-14 (chapter 2), in terms of switch and snubber behavior, it is representative of power converters and motor drives in general. The snubber design procedures presented here will apply to a wide range of different power conversion circuits. The converter is assumed to have an output voltage (Vo) of 300 V, a switching frequency of 250 kHz and a switch duty cycle of 0.25. The load power is about 2 kW.

Because we are interested in modeling the circuit behavior due to switch transitions, which are very short in time compared to the time constants of the input inductor current and the output capacitor voltage, we can replace the input voltage source and inductor with a current source (with an appropriate current waveform!). We can also replace the output filter capacitor and load resistance with a voltage source as shown in figure 7-2. For more explanation of this point see the discussion associated with figure 2-13 in chapter 2.

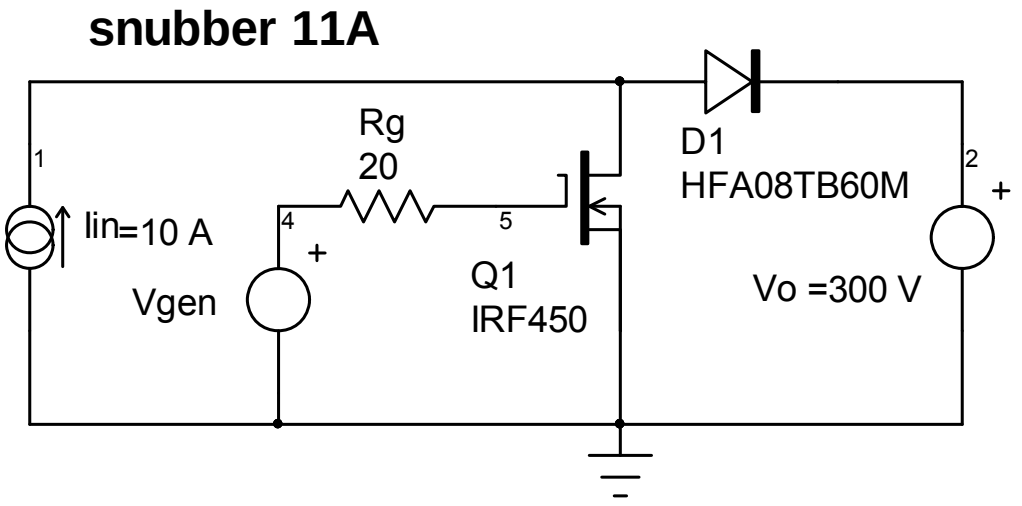


Figure 7-2, simplified converter circuit for SPICE modeling.

For this discussion we will add reasonable values for the parasitic elements as shown in figure 7-3. Some of the parasitic elements (junction capacitances in particular and Q1 source inductance) are included in the device models for Q1 and D1, so we don't need to add them because they are already there.

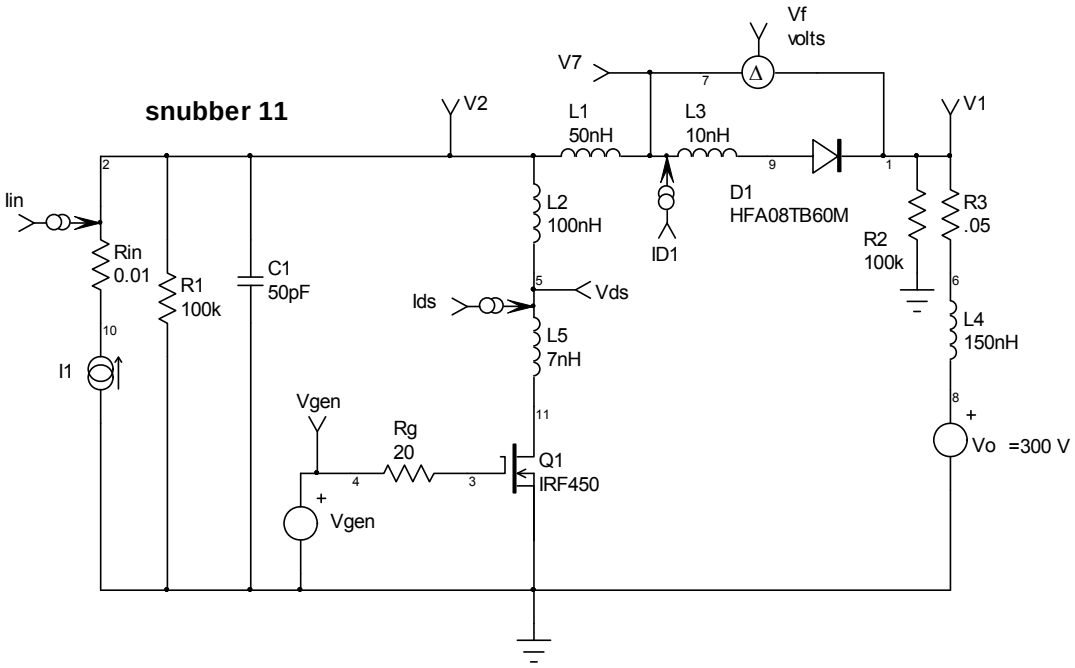


Figure 7-3, circuit model with parasitic elements added.

L3 and L5 represent package inductances not included in the SPICE subcircuit models. R3 and L4 represent the ESR and ESL associated with the output filter capacitor. L1, L2 and C1 are estimates for the parasitics due to the physical layout for a converter of this power level. Very careful layout design might reduce these values but poor design could greatly increase them. The values chosen represent a reasonable compromise.

The metering points included in figure 7-3 represent measurements we would normally make in a real circuit.

Circuit waveform and power loss survey

The next step is to examine the circuit current and voltage waveforms to see what's going on. Vds and Ids for Q1 are shown in figure 7-4.

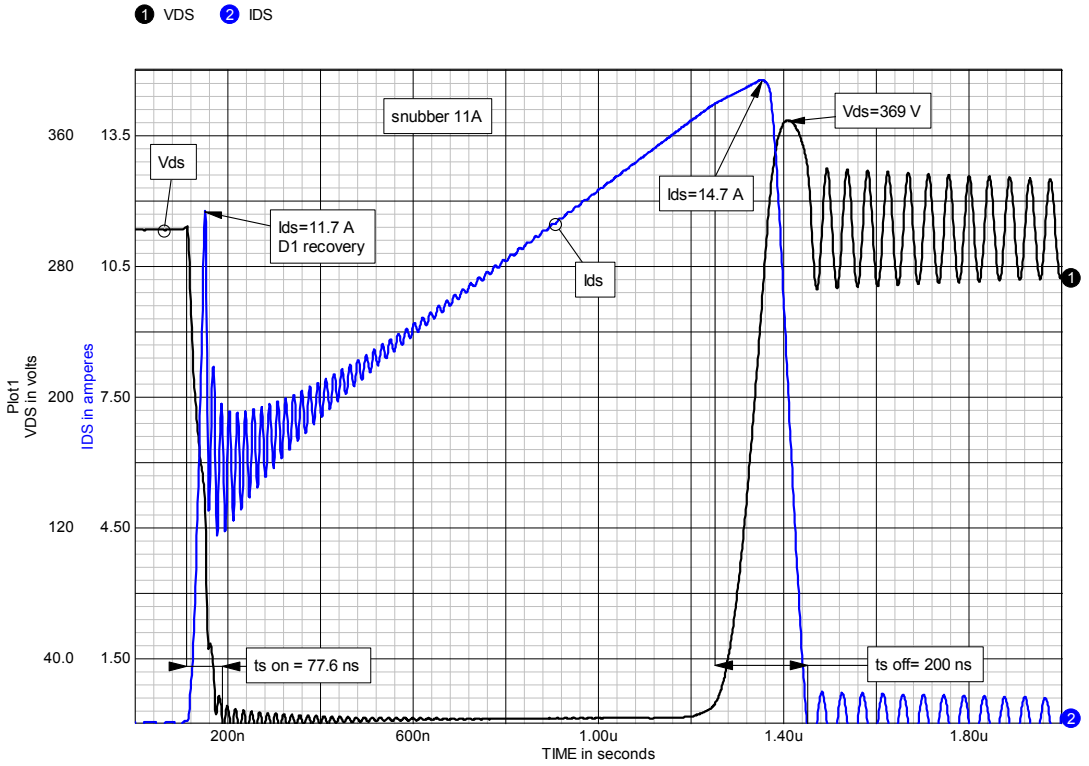


Figure 7-4, Q1 Vds and Ids waveforms.

These are ugly waveforms but unfortunately they are not unusual! On Vds there is a 70 V turn-off spike added to Vo (Vo=300 V) followed by large amplitude high frequency ringing. The voltage spike is not

especially threatening but the ringing is a sure source of EMI. Ids has a large turn-on current spike (about 7 A), from the reverse recovery of D1, added to the 5 A level of the initial input current. Ids also has significant high frequency ringing.

Note that the total turn-on time (ts-on =78 ns) and turn-off (ts-off = 200 ns) times are given in figure 7-4. We will need that information later when we design turn-on and turn-off snubbers for this circuit.

The effect of voltage and current ringing shows up very clearly in the load-line for Q1 shown in figure 7-5. The rather bizarre shape of the load-line locus is due to both the voltage and current ringing and to the reverse recovery current spike associated with D1.

Clearly there is work here for one or perhaps two RC-snubbers to damp the ringing waveforms. Q1 is an IRF450 with a maximum Vds rating of 500 V. Normal derating practice would be to limit the maximum operating Vds to 400 V (80% of maximum). At the moment with Vds peak =369 V we are well below that limit. However, as we add snubber components, one side effect may be an increase in Vds peak. It will be a judgment call if that is acceptable.

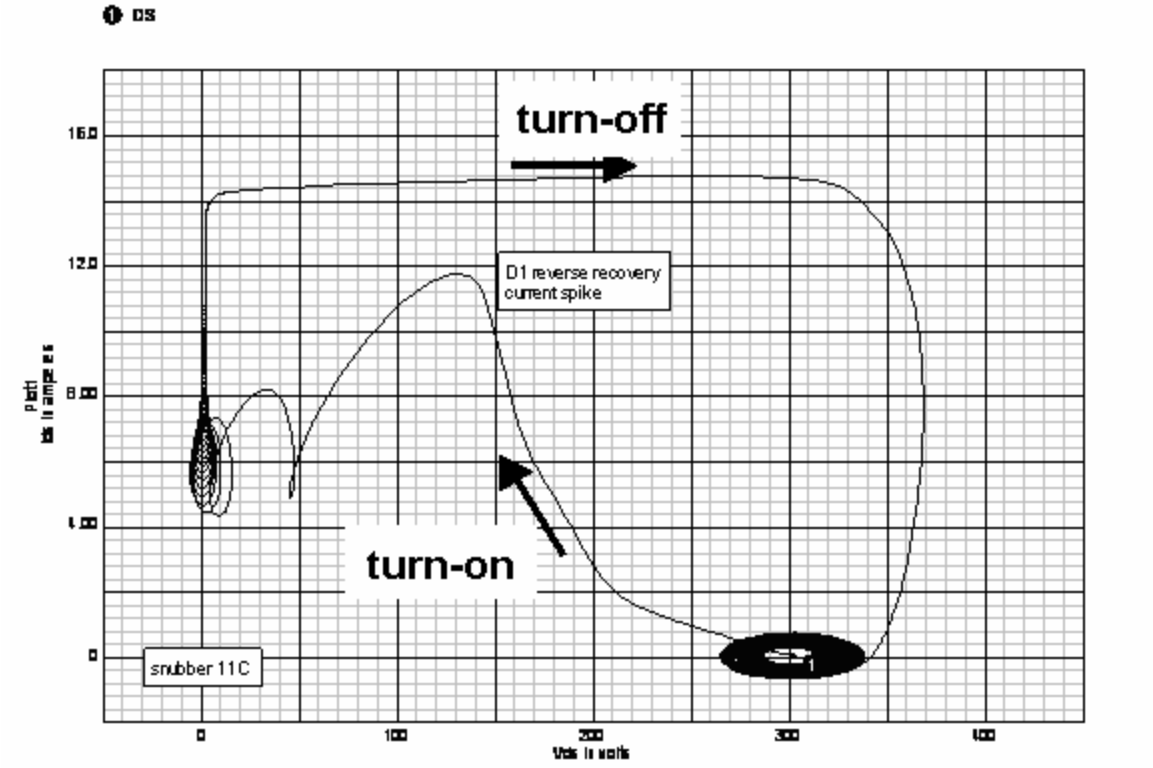


Figure 7-5, Q1 switching load-line.

From the Vds and Ids waveforms we can estimate the peak power dissipation and average power loss in Q1 by multiplying the waveforms. In this case we can have the modeling software do this directly as shown in figure 7-6. In the real world you can either use an oscilloscope with waveform multiplication capability or do it manually using the approximations given in chapter 2.

Included in figure 7-6 is a tabulation of the power loss assuming fs = 250 kHz. This was obtained by integrating the power waveform over one cycle to get the energy dissipation per switching cycle and then multiplying by fs.

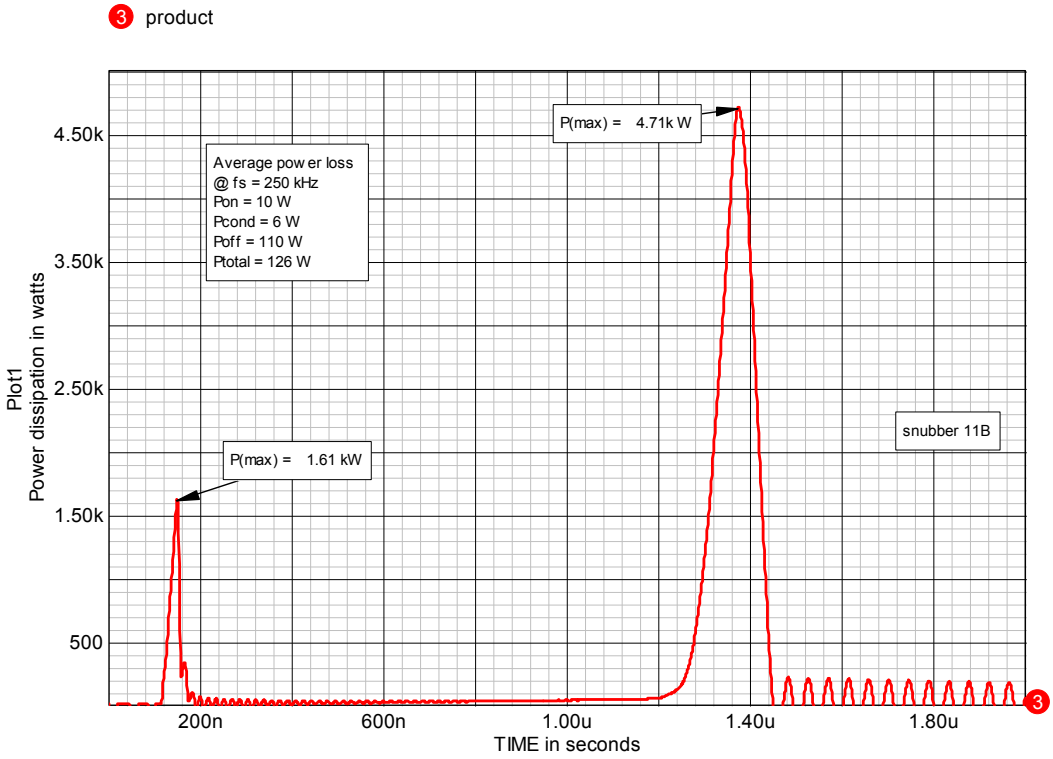


Figure 7-6, instantaneous power dissipation in Q1 during one switching cycle.

In this example the output power is about 2 kW. One percent of 2000 W is 20 W, so for every 20 W of loss we can eliminate, we will gain about 1% in overall circuit efficiency. The turn-on and conduction loss is relatively small (10 W and 6 W) but the turn-off loss is 110 W which reduces overall efficiency by over 5%. From a thermal point of

view it would be helpful to move this loss out of Q1 into a snubber resistor using a RC-diode turn-off snubber. But in general, dissipative snubbers will at best reduce the overall circuit loss by only a small amount. If we want to substantially improve the overall efficiency then we will need to consider using an energy recovery turn-off snubber. We will examine this option shortly.

Turning our attention now to D1. As shown in figure 7-7, we see that the voltage and current waveforms associated with D1 also have severe voltage and current ringing. If we expand the initial part of the voltage waveform in time, as shown in figure 7-8, we see that there is a large reverse voltage spike across D1 (-453 V). Both the ringing and this voltage spike are likely targets for an RC-snubber.

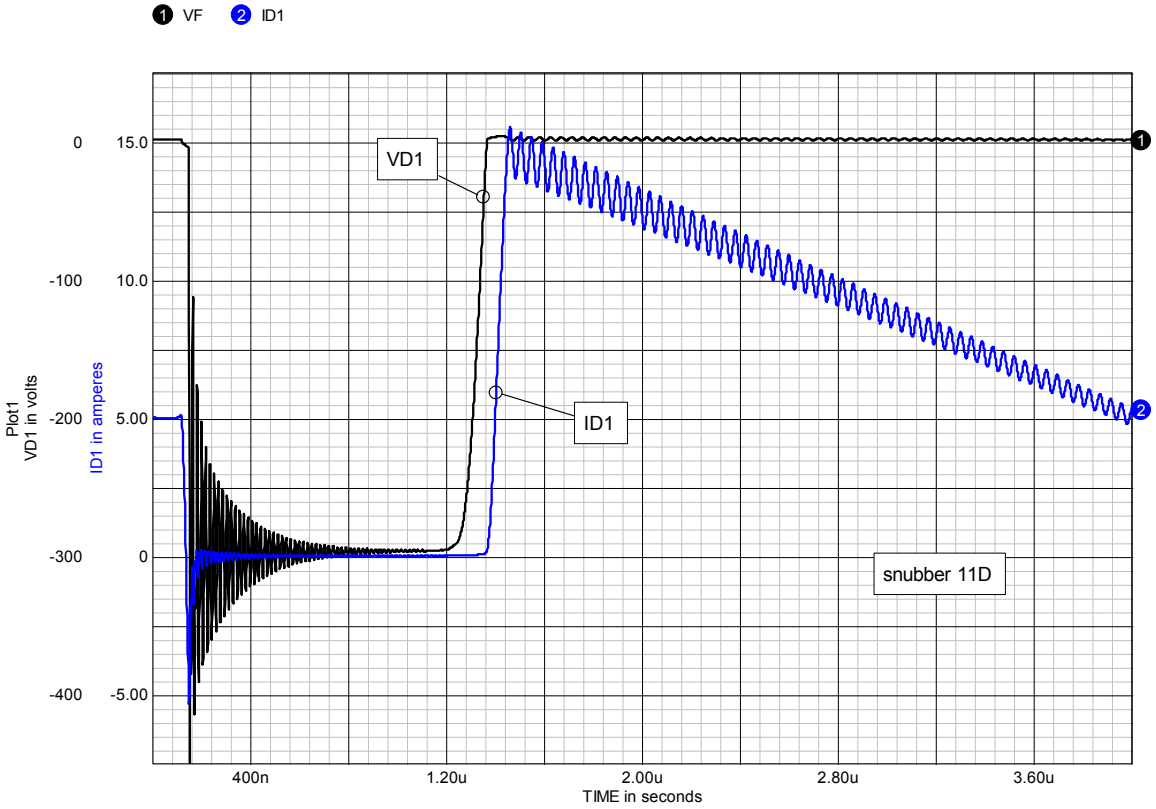


Figure 7-7, voltage and current waveforms associated with D1.

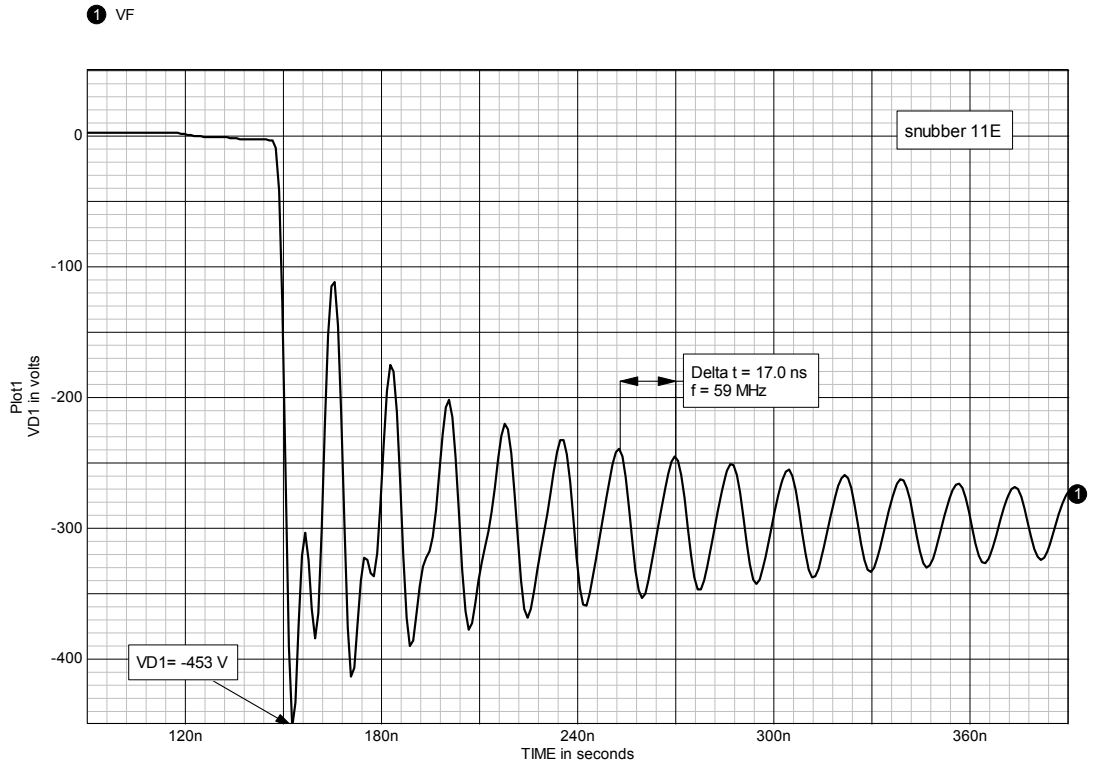


Figure 7-8, expanded view of VD1 at Q1 turn-on.

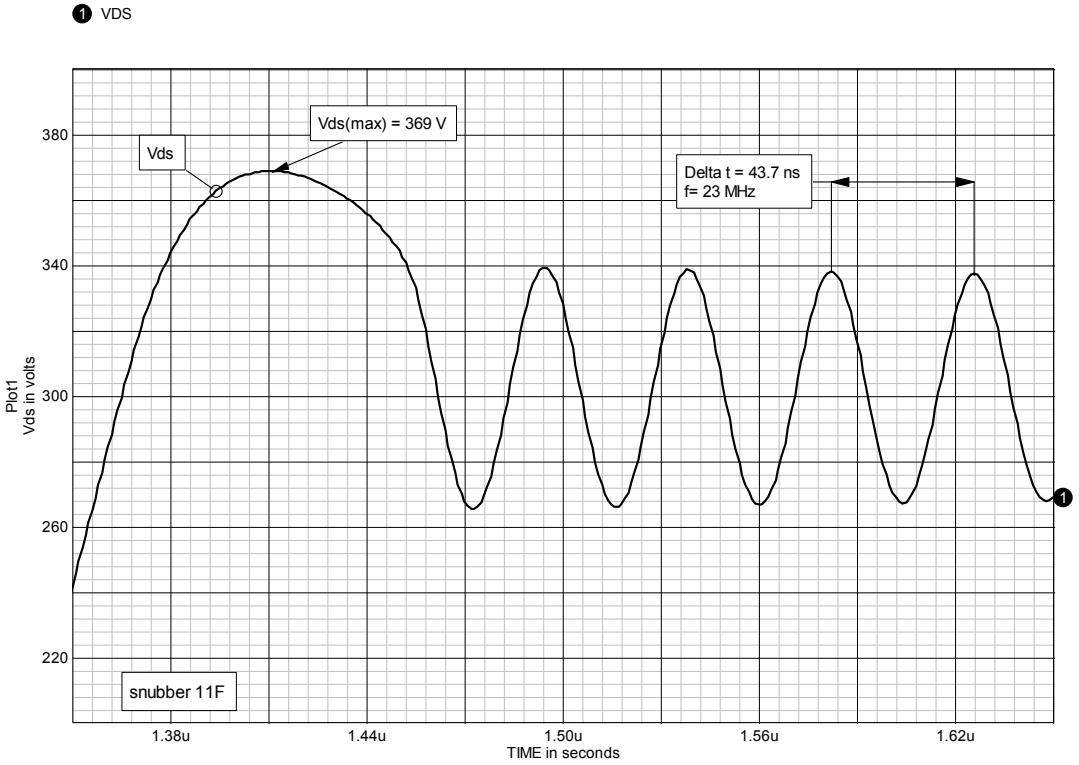


Figure 7-9, expanded view of Q1 Vds waveform at turn-off.

Figure 7-8 includes a measurement of the ringing frequency (about 59 MHz). In a similar way, we can expand a portion of the Q1 Vds waveform, as shown in figure 7-9, to get the ringing frequency associated with this waveform (about 23 MHz).

From the ringing frequency (*f*) and the following expression:

$$C = \frac{1}{4\pi^2 f^2 L}$$

where C is the effective capacitance in the ringing circuit, L is the parasitic inductance and f is the ringing frequency. We can determine equivalent value for C during the two switching states (Q1 on-D1 off or Q1off-D1 on). We are assuming operation in the continuous conduction mode (CCM). In the discontinuous mode there would be three operating states.

When Q1 is on, D1 is off and the ringing is primarily due to the series combination of the parasitic inductances and the reverse capacitance of D1. When Q1 is off and D1 is conducting, then the same series inductance is present but the capacitance is primarily the output capacitance of Q1. In this case the result is: C = 23 pF when Q1 is on and C = 151 pF when D1 is conducting. These values are for the assumption of a simple series LC resonant circuit but the presence of C1 can affect that picture. We could do a more complex analysis to separate out all the effects but usually that's not needed. The simple approximation of a single resonant circuit is usually adequate for the design of an RC-snubber.

This example assumes CCM for the current in the input inductor. In the discontinuous mode there will be a third state where both Q1 and D1 are off. In the discontinuous mode you would expect the ringing frequency to be about 63 MHz because the two capacitances (Q1 Coss and D1 C reverse) are in series.

We have assumed we knew the parasitic inductances and then calculated C from the ringing frequencies. We could also have looked up the reverse capacitance for D1 and Coss for Q1 and then

calculated the effective L from the ringing. As shown in chapter 6, if we don't know either L or C we could insert a test capacitor to determine both (see figures 6-21 and 6-22 and the associated text).

This completes the initial waveform survey. We now have the basic information needed to design some snubbers which may improve these waveforms!

Example 1, an RC-snubber

As a first step in taming the ringing waveforms we will place an RC-snubber across Q1 as shown in figure 7-10. This should damp the Vds ringing at Q1 turn-off but will probably not have much effect on the ringing across D1.

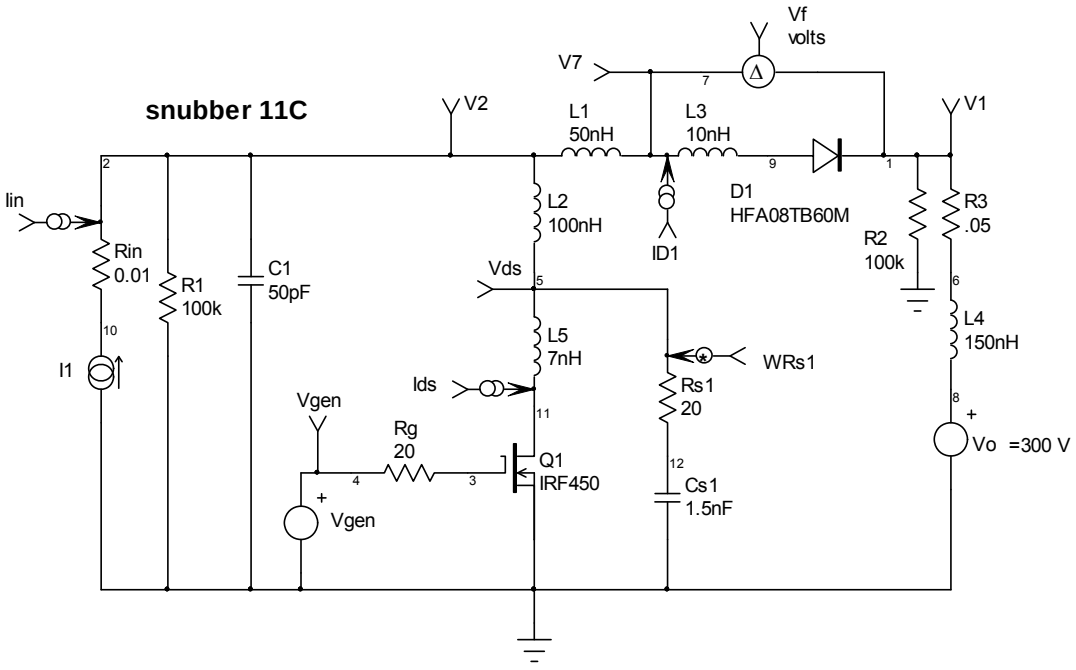


Figure 7-10, an RC-snubber placed across Q1.

When Q1 is off, it is the output capacitance (Coss 151 pF) that rings with the parasitic inductance (L=L1+L2+L3+L4+L5=317 nH). The RC-snubber capacitor (Cs1) is usually made 3 to 10 X Coss. Larger values of Cs1 give better damping and reduce dissipation in Q1 but result in greater power dissipation in Rs1. Figure 7-11 shows the effect of two different values for Cs1 (with optimized values for Rs1)

on the Vds waveform at turn off. One version of the RC-snubber has Cs1= 470 pF (3 X Coss) and Rs1=34 Ohm. The second version has Cs1=1.5 nF (10 X Coss) and Rs1=20 Ohm. In both cases the peak value for Vds and the total circuit loss are almost the same, however, the dissipations in Q1 and Rs1 are different. The larger value for Cs1 acts like a turn-off capacitive snubber for Q1, reducing the turn-off dissipation in Q1 from 126 W to 111 W but the loss in Rs1 rises from 4 W to 18 W. When I employ this kind of snubber I prefer to use a larger value for Cs1 to obtain the benefits of lower switch loss, a somewhat better load-line and better damping in exchange for needing a higher power resistor for Rs1. This is a judgment call. You will have to decide for yourself which way to go.

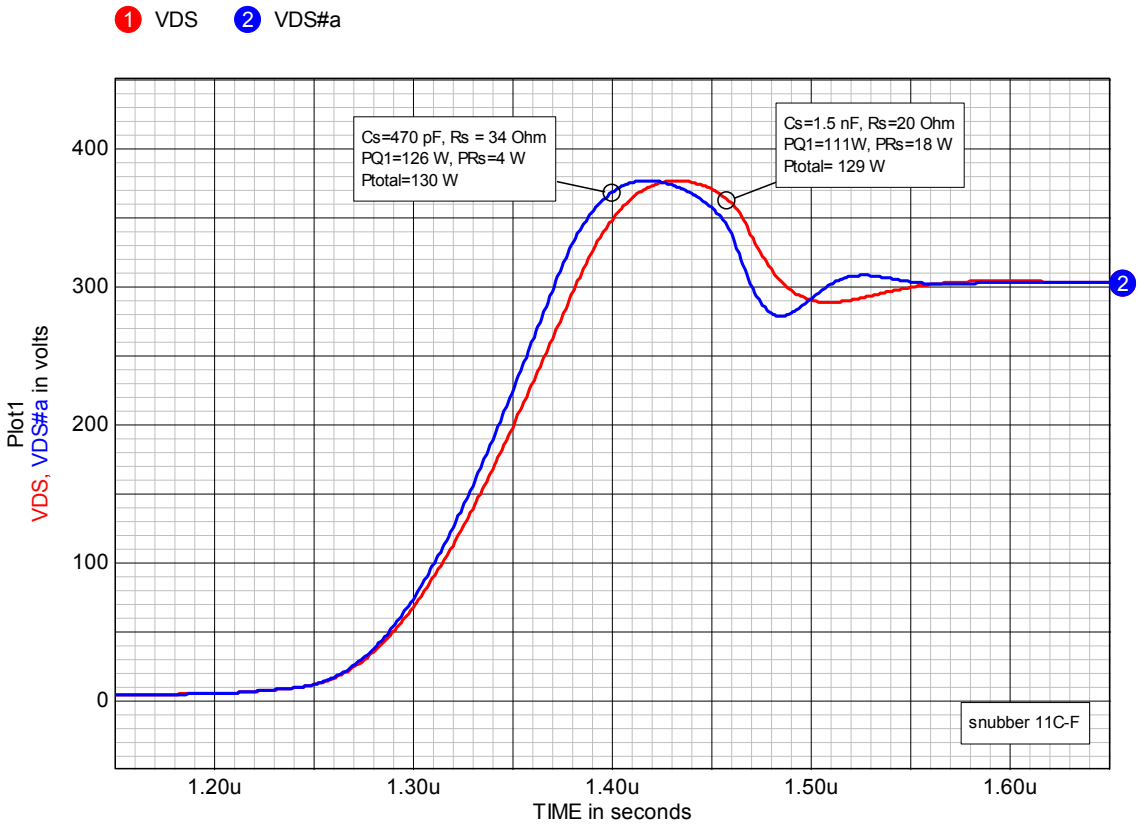


Figure 7-11, comparison of Vds at Q1 turn-off, for two different RC-snubber values.

We will set Cs1=1.5 nF for the rest of this discussion. A 500 V, dipped mica capacitor would be suitable for this application. See chapter 6 for more details on capacitor selection.

The value for the snubber resistor (Rs1) is based on the impedance (Zo) of the LC network (L parasitic and Coss+Cs1):

$$Z_o = \sqrt{\frac{L_{parasitic}}{Coss + Cs1}} = \sqrt{\frac{317nH}{1.65nF}}$$

$$Z_o = 13.9\,Ohm$$

A good starting place is to set Rs1=1.5Zo. In this case that would be 21.7 Ohms. A convenient standard value is 20 Ohm. We'll go with that because the performance of the snubber is not strongly affected by small changes in resistor value.

The RC-snubber is now designed as shown in figure 7-10. The Q1 Vds and Ids waveforms with the snubber are shown in figure 7-12.

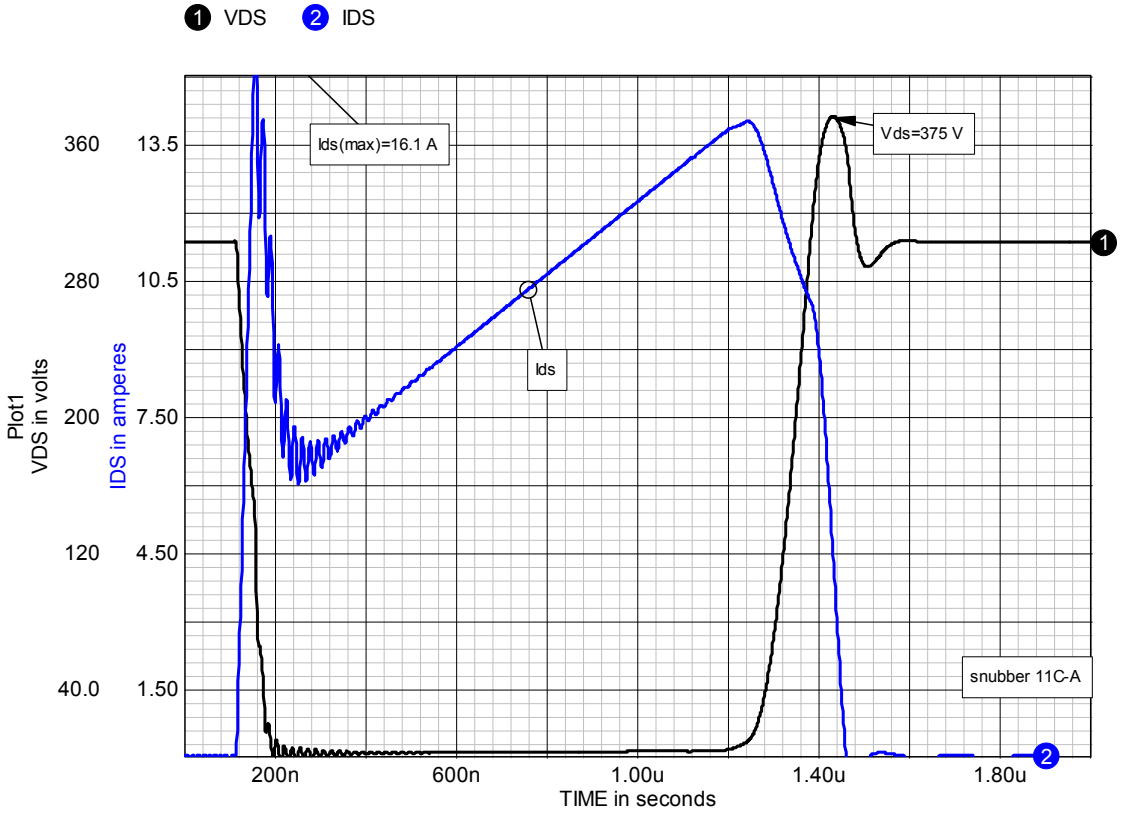


Figure 7-12, Q1 Vds and Ids waveforms with an RC-snubber from drain-to-source.

Compared to the waveforms in figure 7-4 (no snubber) Vds at Q1 turn-off is much improved. The ringing is nicely damped although the peak value for Vds has increased slightly from 369 to 375 V. This is due to the presence of Cs1. We can also see that Ids at turn-off has improved: i.e. Ids now starts to fall before Vds rises. This is also due to the presence of Cs1. However, there is downside to the addition of the snubber. The peak value for Ids at Q1 turn-on has risen from 11.7 to 16.1 A. This is due to the discharge of Cs1 through Rs1 and Q1 at Q1 turn-on.

The changes in switch power dissipation can be seen by comparing figures 7-6 and 7-13.

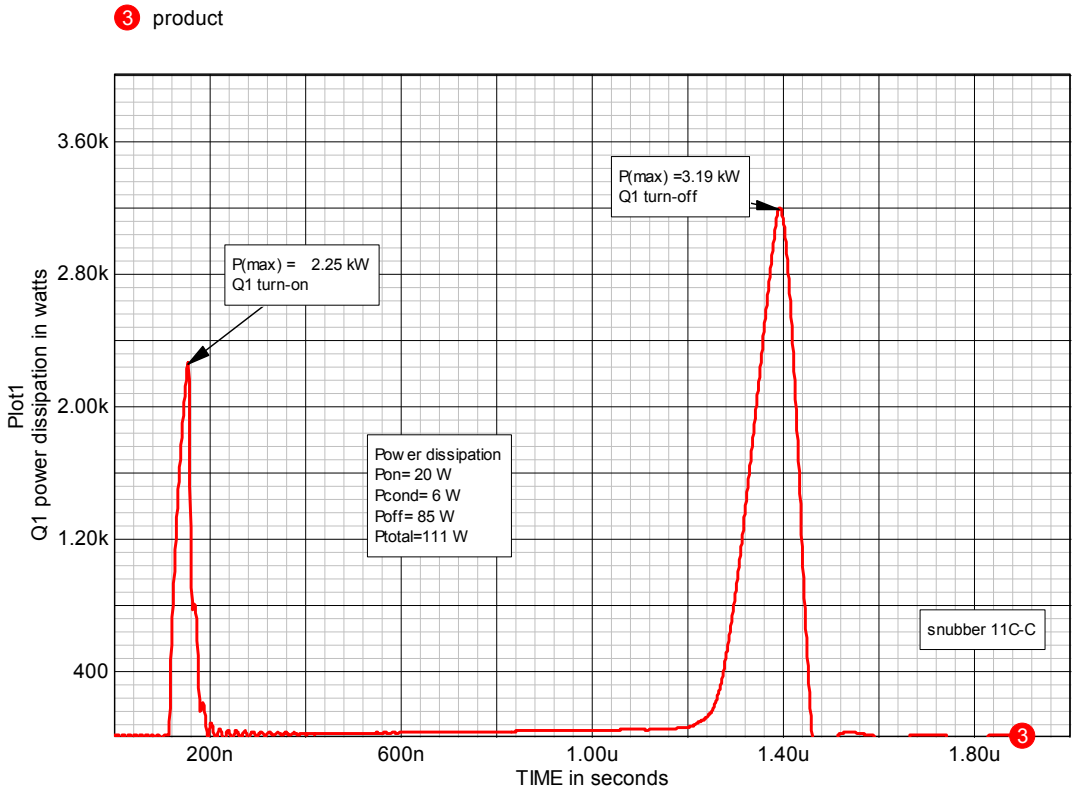


Figure 7-13, power dissipation in Q1 with the RC-snubber from drain-to-source.

At Q1 turn-off the peak power has been reduced from 4.7 kW to 3.2 kW but at turn-on the peak power has been increased from 1.6 kW to 2.3 kW. The price for using the snubber is an increase in power loss at Q1 turn-on. As indicated on the graph, the total power dissipation in Q1 has been reduced from 126 W to 111 W, almost 13%.

Certainly worthwhile. However, we will now have 18 W of power dissipation in Rs1 (obtained from the current waveform in Rs1) which increases the total circuit loss from 126 to 129 W. While we have reduced the switch stress the overall circuit loss has changed little. Given the 18 W of dissipation in Rs1, a non-inductive resistor with a rating of 30 W or more should be selected for Rs1. See chapter 6 for a discussion on resistor selection.

Example 1 summary:

Cs1= 1.5 nF, 500 V, dipped mica capacitor, ICs1 = 0.94 A
Rs1= 20 Ohm, 30 W, non-inductive resistor

Example 2, another RC-snubber design

Let's now see what can be done with an RC-snubber across D1 as shown in figure 7-14.

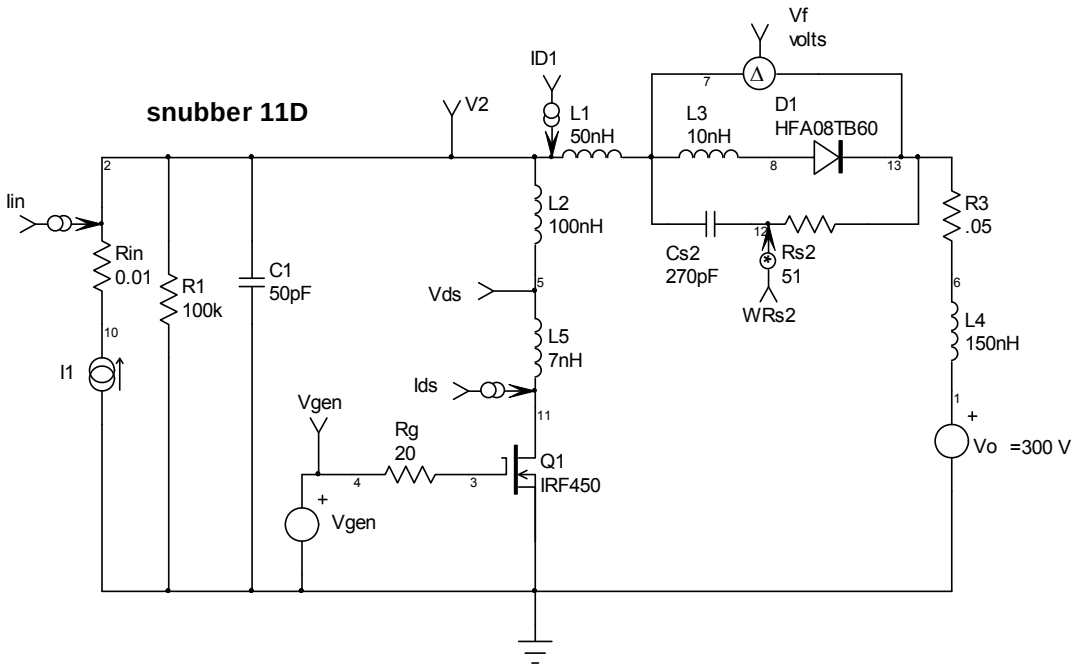


Figure 7-14, adding an RC-snubber (Rs2 and Cs2) across D1.

As shown earlier, the effective series capacitance when D1 is off is about 23 pF. 10 X 23 = 230 pF. The nearest standard values are 220 pF and 270 pF. In this case we will set Cs2=270 pF because

that will give somewhat better damping and in any case the power loss in this snubber is much smaller than that for Q1.

Rs2 = 1.5 Zo = 1.5*SQRT(317/.270) =51 Ohm.

These are the values shown in figure 7-13. The voltage waveform across D1 is shown in figure 7-15.

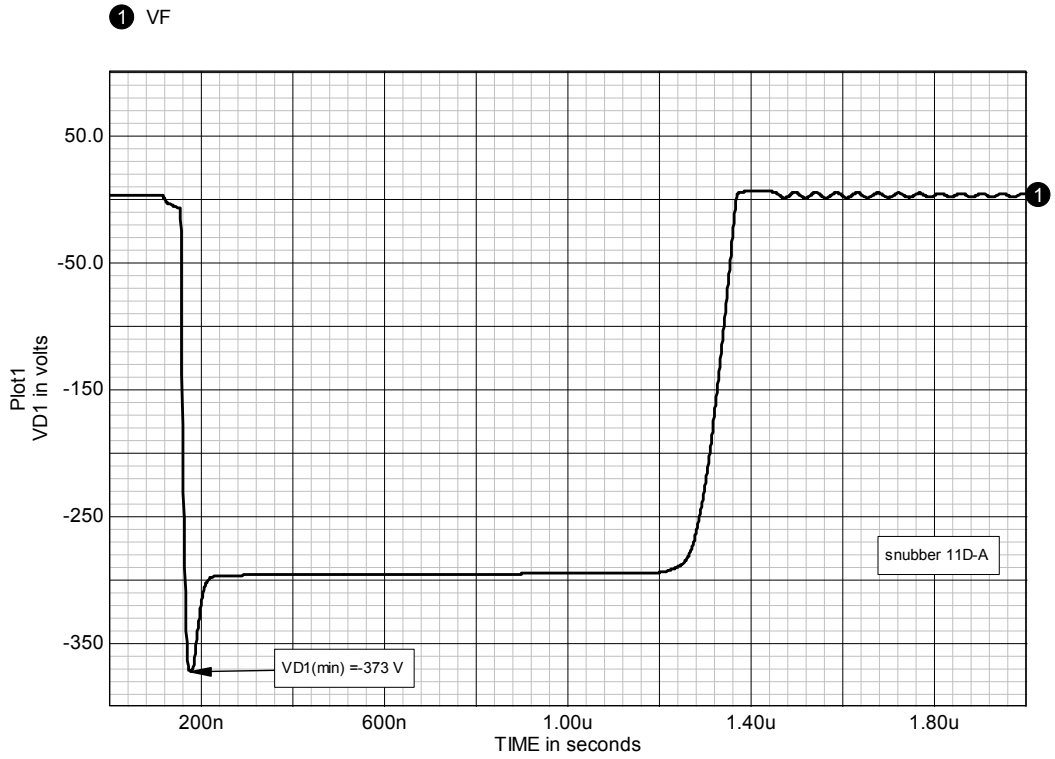


Figure 7-15, voltage waveform across D1 with the RC-snubber across it.

Comparing figures 7-8 and 7-15, we see that with the snubber the ringing is now damped and the reverse voltage spike has been reduced from -453 V to -373 V, a substantial improvement. If more reduction in the reverse voltage spike is needed then the value for Cs2 would need to be increased.

However, Cs2 will have to be charged through Q1 but the additional current is relatively small. The power dissipation in Rs2= 4 W.

Example 2 summary:

Cs2 = 270 pF, 500 V, dipped mica capacitor, ICs2=280 mA rms
Rs2 = 51 Ohm, 10 W, non-inductive resistor

Example 3, more RC-snubber

To clean up the waveforms on both Q1 and D1 we will have to use an RC-snubber across both as shown in figure 7-16.

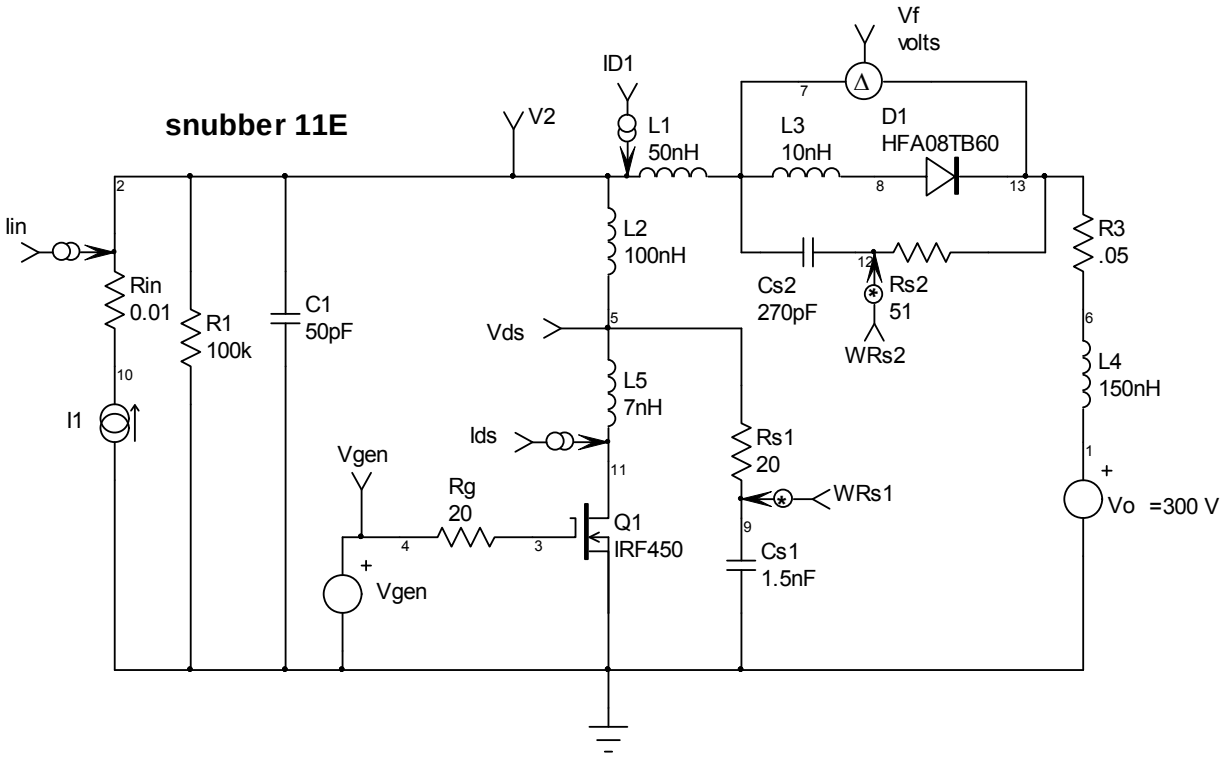


Figure 7-16, circuit with RC-snubbers across both Q1 and D1.

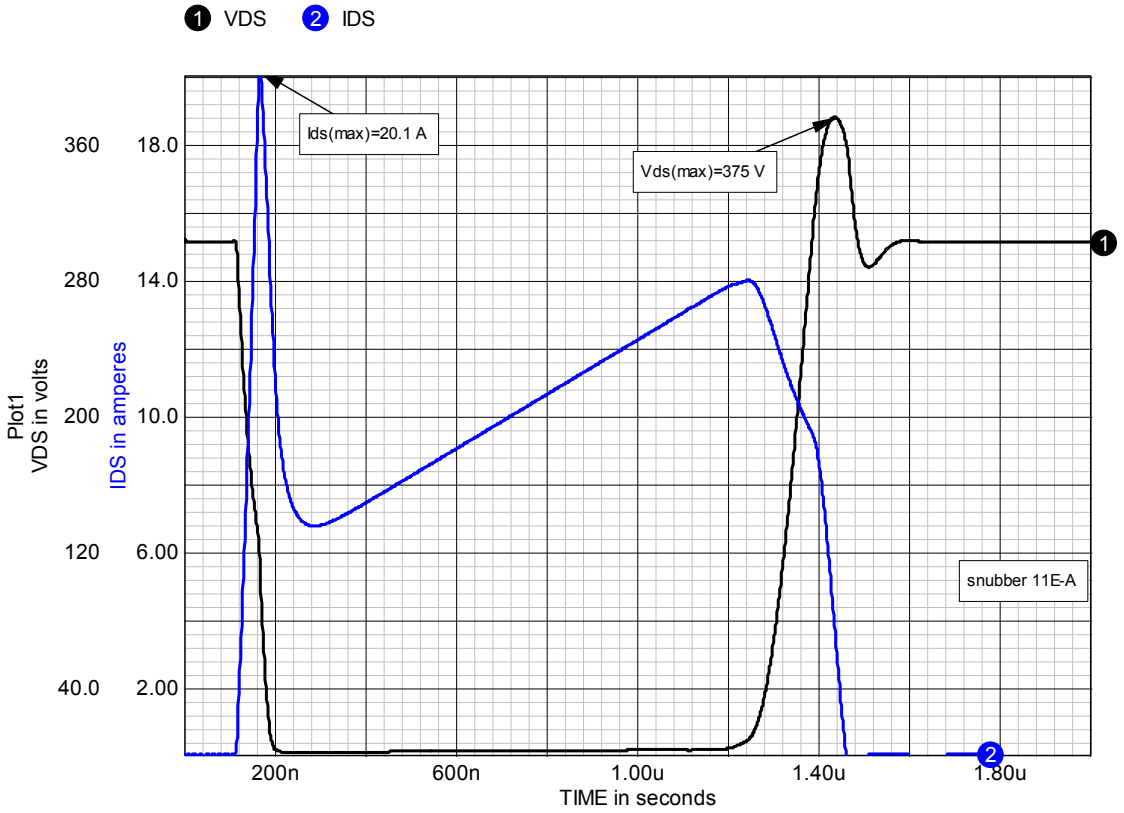


Figure 7-17, Vds and Ids for Q1 with both snubbers present.

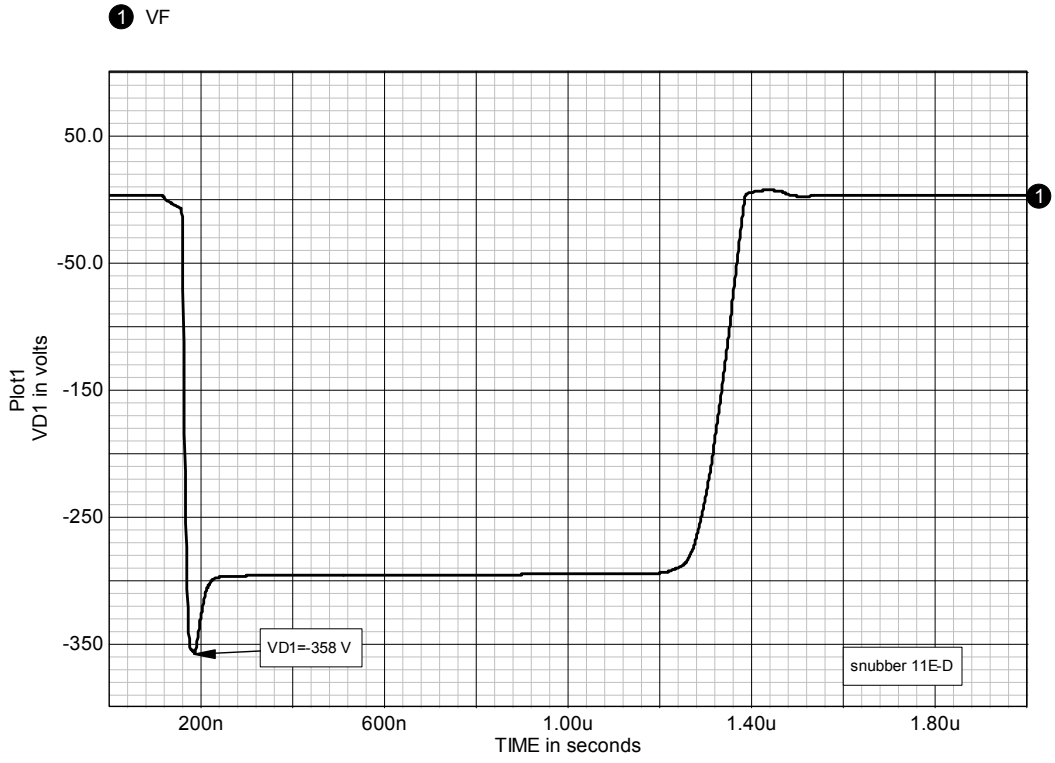


Figure 7-18, voltage across D1 with both snubbers present.

The Q1 waveforms with these snubbers are shown in figure 7-17 and the voltage waveform across D1 is given in figure 7-18. The load-line for Q1 is shown in figure 7-19.

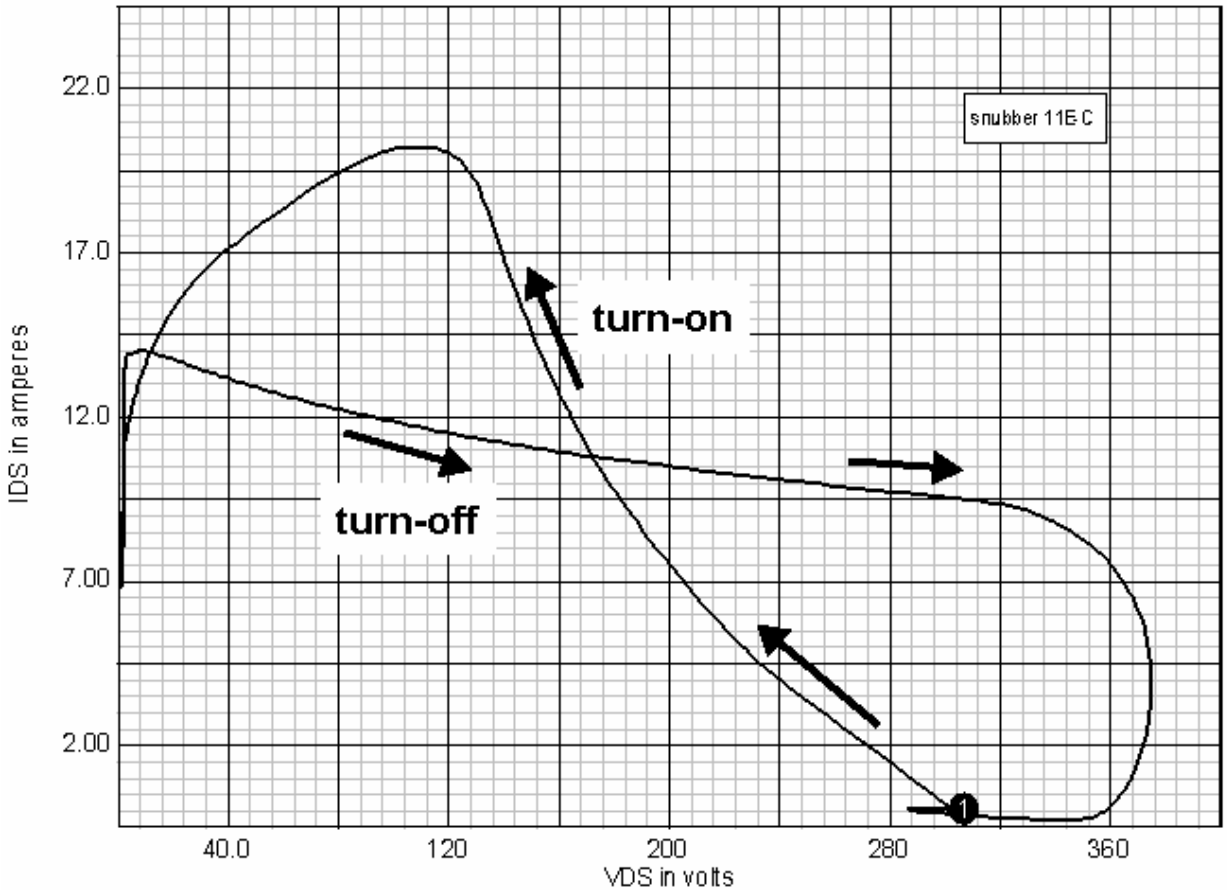


Figure 7-19, Q1 load-line with both snubbers present.

Comparing these figures to figures 7-4, 7-5 and 7-8, we see that the waveforms are much cleaner and the ringing is well damped. However, the peak Ids current spike at Q1 turn-on is much higher due to the need to charge or discharge the snubber capacitors.

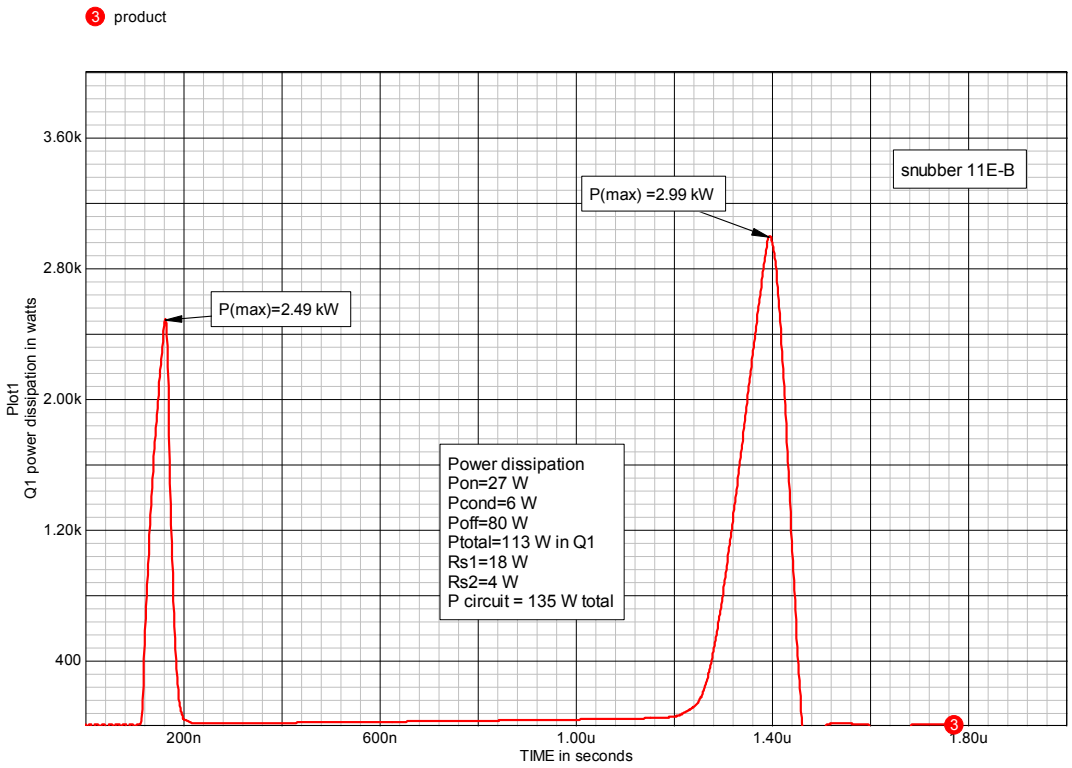


Figure 7-20, power dissipation in Q1 (product of Vds X Ids).

The power dissipation in Q1 is shown in figure 7-20. In exchange for damping the waveform ringing and reducing the dissipation in Q1 by 10%, the total circuit loss has increased 9 W (about 0.5%) and the Ids peak in Q1 has increased. This illustrates the point made earlier that snubbers have both advantages and disadvantages. While reducing some stresses others may be increased.

Example 3 summary:

Cs1= 1.5 nF, 500 V, dipped mica capacitor, ICs1=0.9 A rms
Cs2 = 270 pF, 500 V, dipped mica capacitor, ICs2=280 mA rms
Rs1= 20 Ohm, 30 W, non-inductive resistor
Rs2 = 51 Ohm, 10 W, non-inductive resistor

Example 4,a turn-off RC-diode snubber

The previous RC-snubber examples did reduce the power dissipation in Q1 but only by 10% or so. If we wish to substantially reduce the dissipation in Q1 and perhaps reduce the overall circuit loss we will

have to use another type of snubber. A suitable candidate is the RC-diode turn-off snubber shown in figure 7-21 (Rs, Cs and Ds).

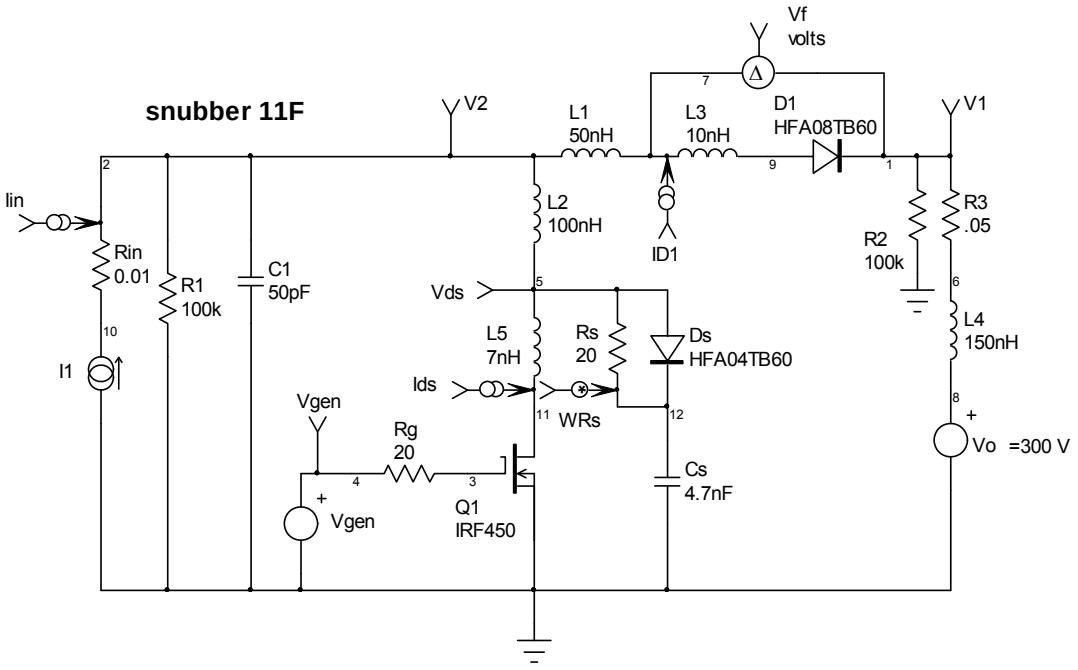


Figure 7-21, adding an RC-diode turn-off snubber (Rs, Cs and Ds) to the circuit.

From McMurray[290] (see also chapter 4 discussion) the initial value for Cs is typically chosen from:

$$Cs = \frac{Ids \bullet t_{s-off}}{2Vo}$$

From figure 7-4 we see that Ids = 14.7 A and $t_{s\text{-}off}$ = 200 ns. We also know that Vo = 300 V. Therefore Cs = 4.9 nF. The closest standard value is 4.7 nF, again in a dipped mica capacitor. let Cs = 4.7 nF.

In this snubber Rs is chosen in a way very different from the RC-snubber. The function of Rs is to discharge Cs at Q1 turn-on. We need a value for Rs which allows Cs to be almost completely discharged during the minimum on-time of Q1. In this case we set the minimum on-time to: ton-min = 500 ns. To properly discharge Cs

we will need five time-constants (τ=RsCs) so that τ = ton-min/5 =100 ns:

$$Rs = \frac{t_{on-\min}}{5Cs} = 21\,Ohm$$

We will chose the nearest standard value, Rs = 20 Ohm. It is just a coincidence that this value for Rs is same as in the previous RC-snubber examples. There is no relationship between the two.

Q1 waveforms for the circuit using the RC-diode snubber are shown in figure 7-22.

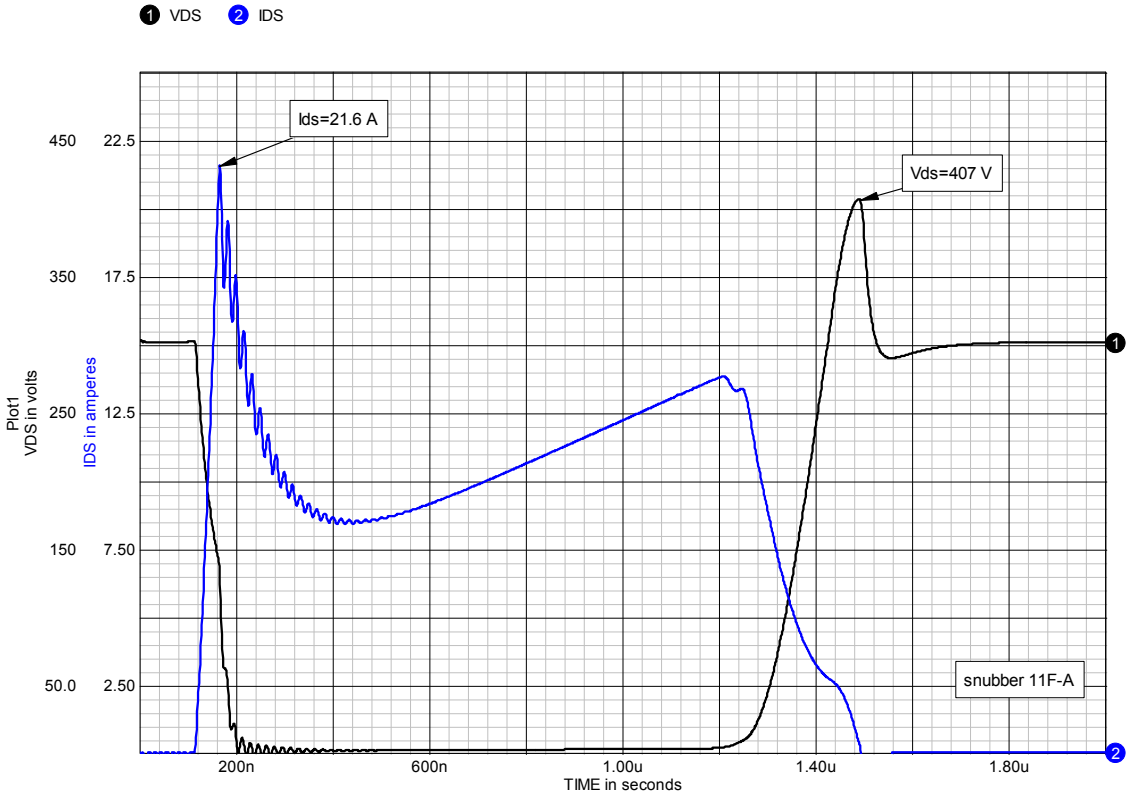


Figure 7-22, Q1 Vds and Ids waveforms using the RC-diode snubber.

Compared to the waveforms in figure 7-4, at Q1 turn-off, Ids starts to fall well ahead of the rise in Vds, this will mean much lower turn-off stress and loss in Q1. In addition, the Vds ringing associated with Q1 turn-off has been eliminated. On the downside however, we see that the introduction of Cs has allowed the peak value for Vds at turn-off,

to rise from 369 V to 407 V, which pushes us over the 400 V derated limit for Vds given earlier. We also see that due to the discharge of Cs through Rs, the current spike on Q1 Ids at turn-on is now quite large, almost 22 A. In addition we can infer from the ringing on Ids that the ringing across D1 has not been eliminated. To fix that problem we will have to retain the RC-snubber across D1 as shown in figure 7-23.

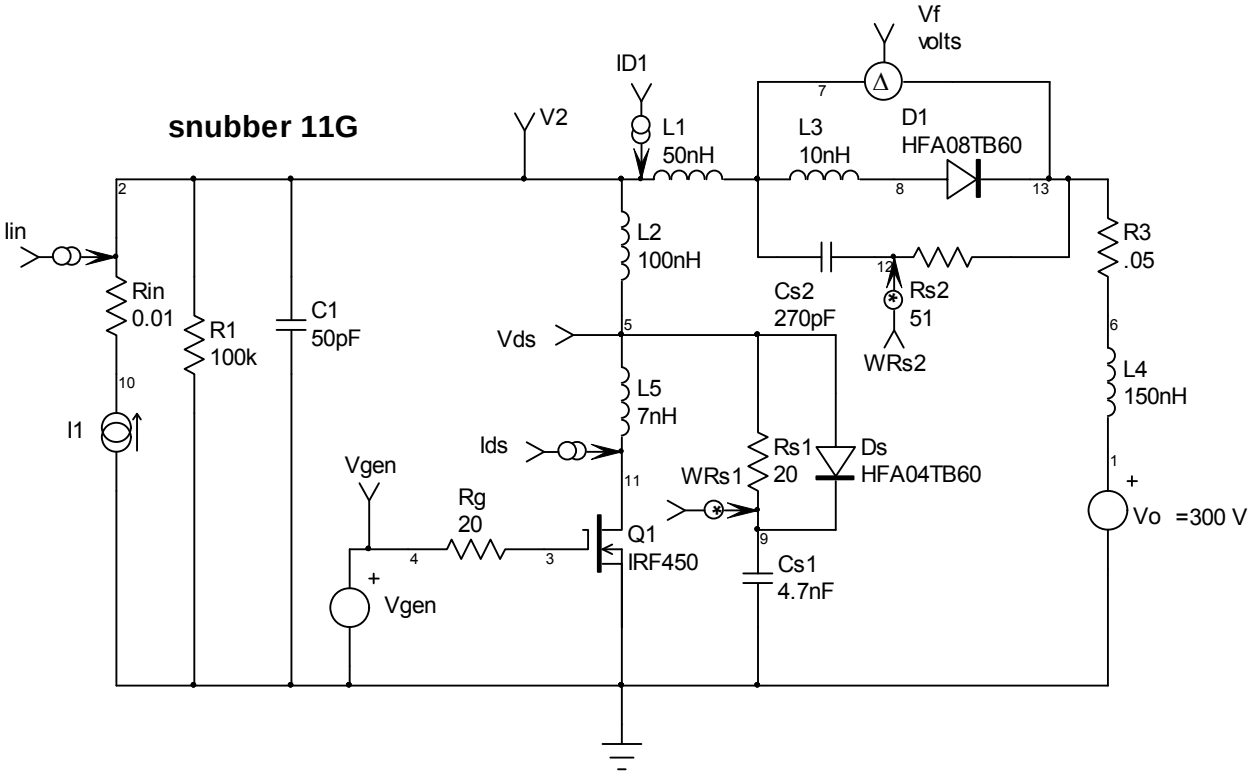


Figure 7-23, circuit with both snubbers present.

The waveforms using both snubbers are shown in figure 7-24. The waveforms are now very clean and the Vds voltage spike at Q1 turn-off has been reduced slightly to 404 V. The Q1 load-line, shown in figure 7-25, is also much nicer, compared to figure 7-5, with the exception that the turn-on current spike is much larger. The voltage waveform across D1, shown in figure 7-26, is now well damped with only a 43 V spike added to the normal -300 V reverse voltage.

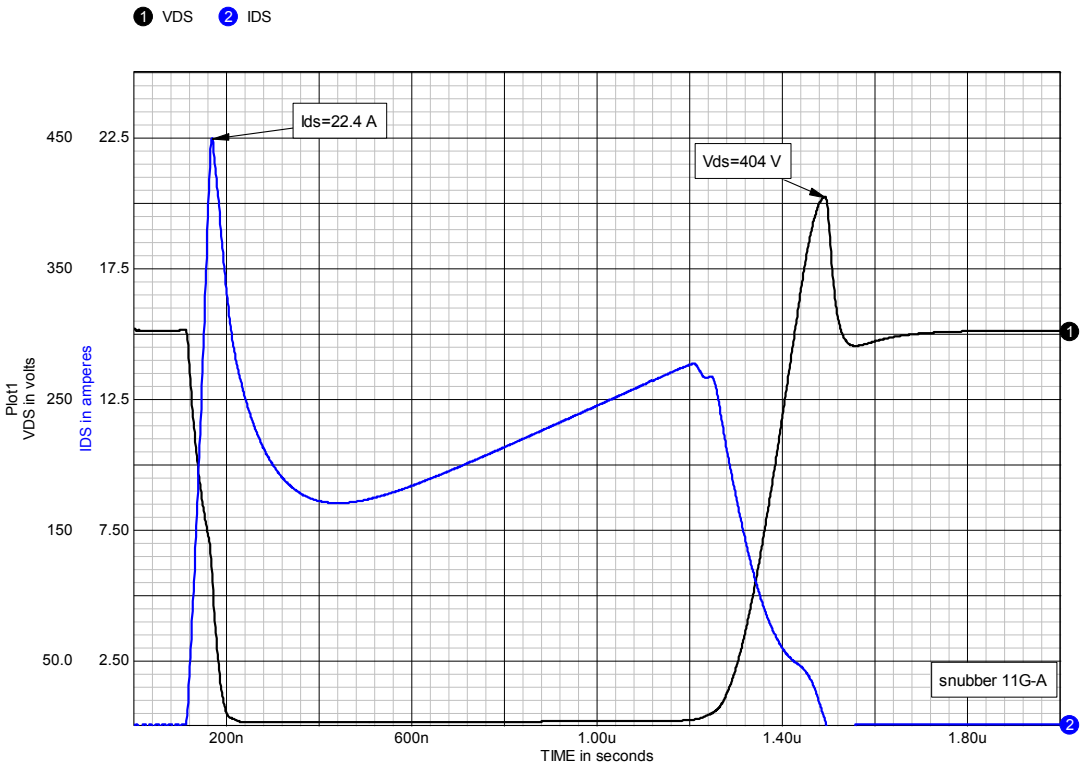


Figure 7-24, Q1 Ids and Vds with both snubbers present.

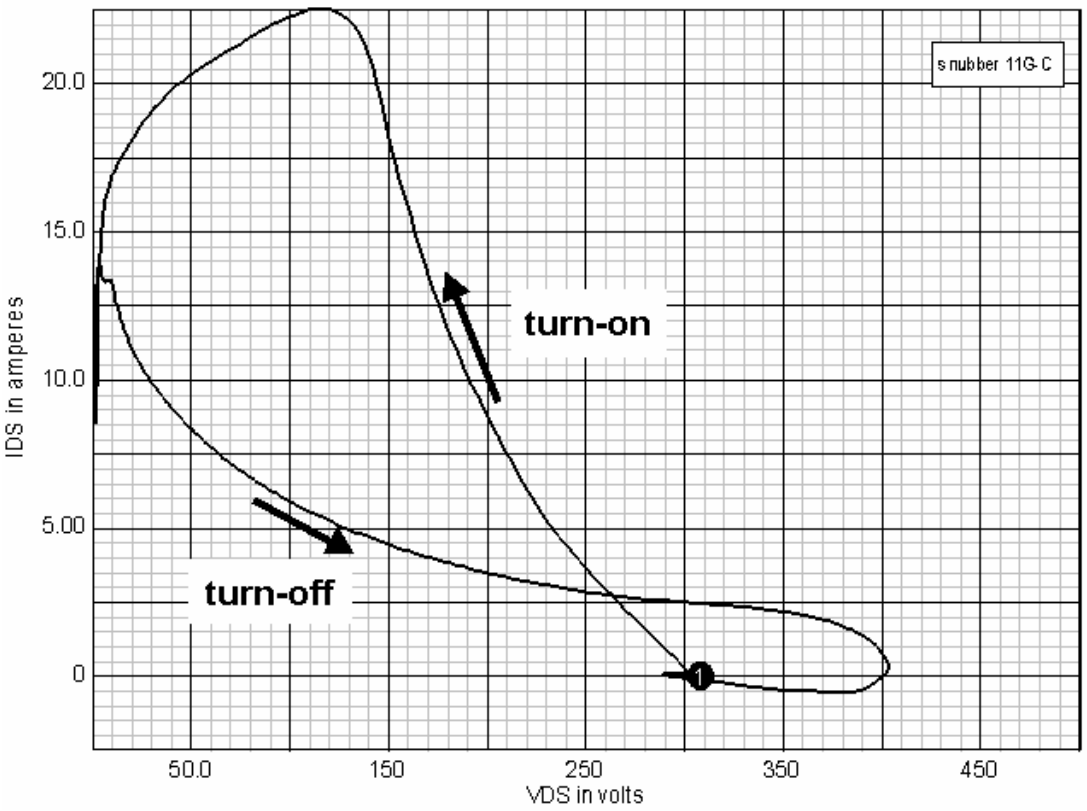


Figure 7-25, Q1 load-line with both snubbers in the circuit.

The power dissipations in Q1, Rs1 and Rs2 are given in figure 7-27, along with the peak power in Q1. It is clear that the turn-off snubber is very effective in reducing power dissipation at turn-off. Comparing figure 7-27 to figure 7-6, the case without a snubber, we see that the peak power at Q1 turn-off has gone from 4.7 kW down to 0.7 kW and the total dissipation in Q1 has dropped from 126 W to 71 W. A 45% reduction. The overall circuit loss has also dropped by 6 W. However, due to the need to discharge the snubber energy through Q1, the turn-on peak power has increased from 1.6 to 3 kW which keeps the total dissipation in Q1 from falling further. It is clear that greater reductions in Q1 dissipation will require a more complex snubber.

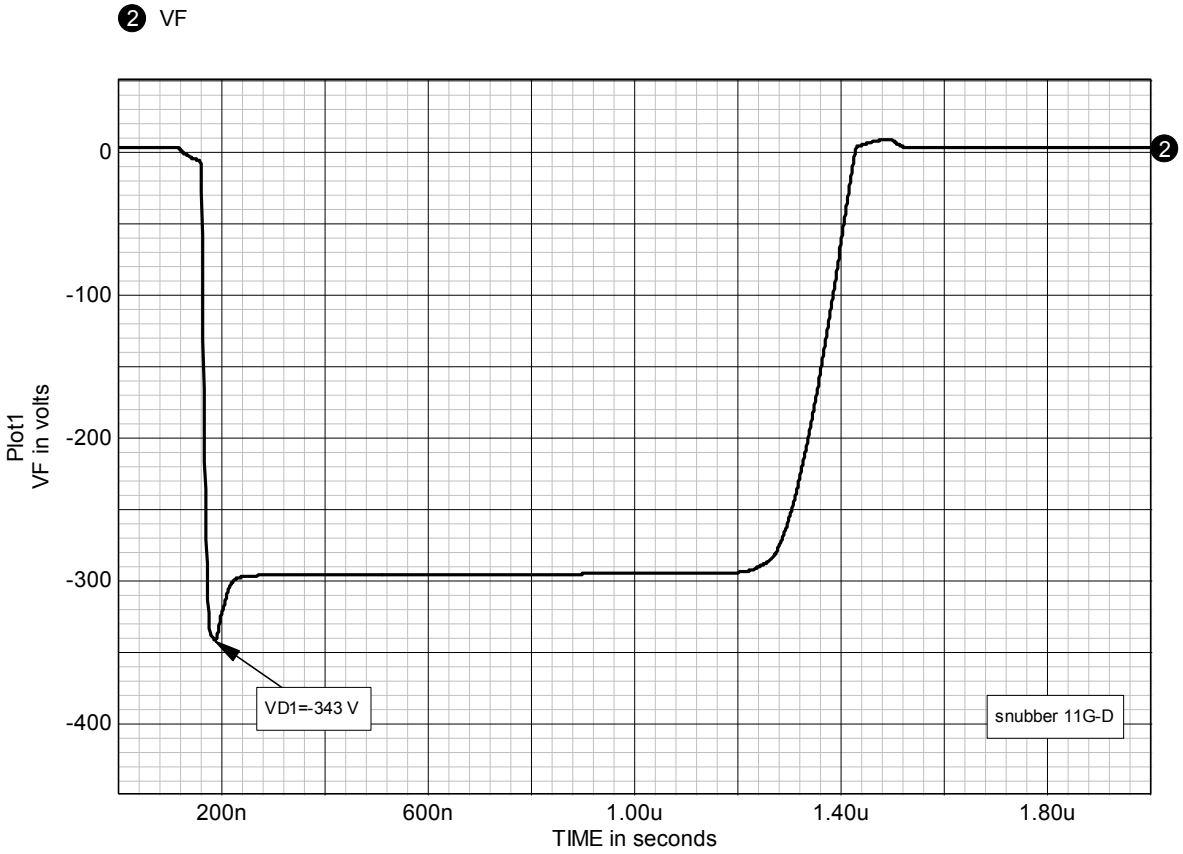


Figure 7-26, voltage waveform across D1.

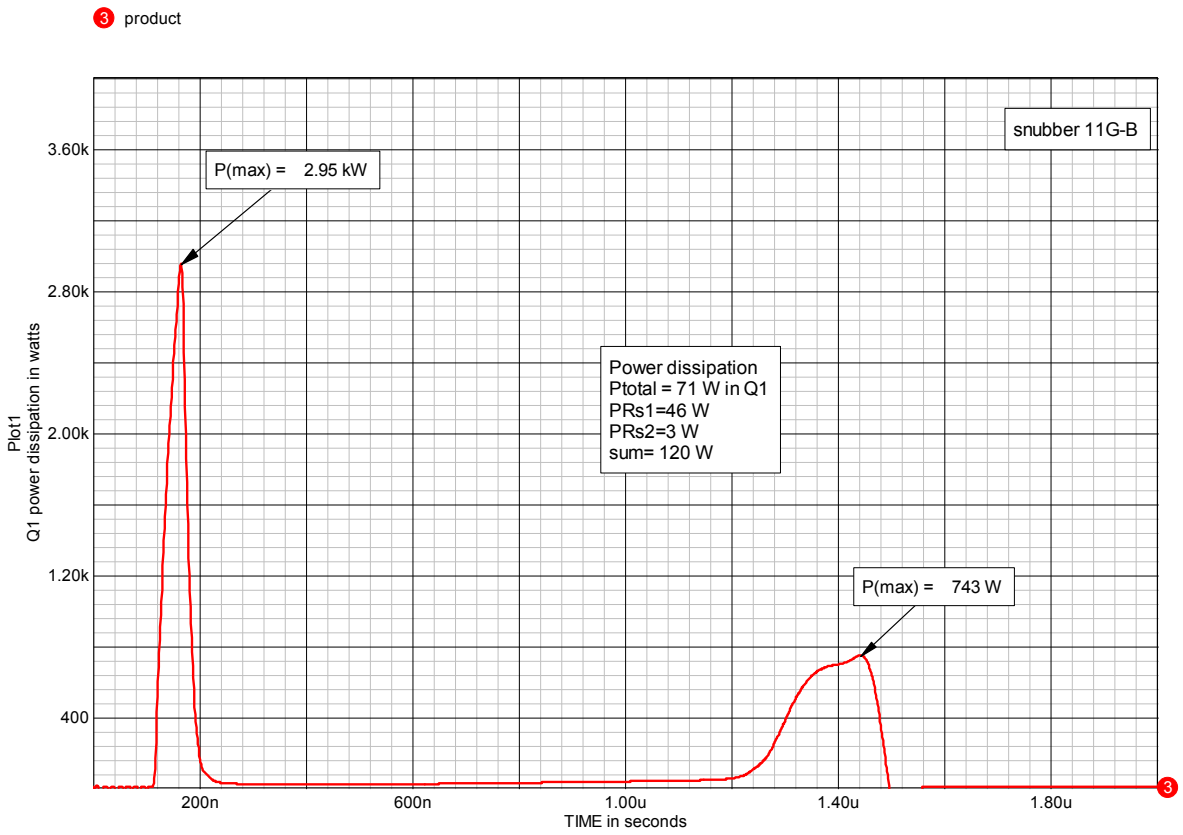


Figure 7-27, power dissipation in Q1 with both snubbers present.

The dissipation in Rs1 (in figure 7-23) is about 46 W, this indicates the use of a resistor rated for 75 to 100 W. A wire-wound power resistor of this size can have 15 uH or more of series inductance (ESL). Adding inductance in series with Rs1 to the model will show that there is a delay in the rise of Ids at turn-on because the inductor delays the discharge of Cs1. This can reduce the turn-on power loss in Q1. However, it will also introduce a new source of ringing on Vds at Q1 turn-off which will require another RC-snubber to damp. You might be better off to use a non-inductive resistor for Rs1 and introduce a discrete inductor in series with Rs1 if you want to play this game.

The diode used in this snubber (Ds) does not have to be particularly fast recovery. A careful examination of D1 waveforms will show that in normal operation, Cs will be fully charged long before Q1 turns on again and the current through D1 is very small at the time reverse voltage is applied across it. A diode with t_{rr} of 200 to 400 ns would be fine in this application.

Example 4 summary:

Rs1=20 Ohm, 75 W, non-inductive resistor
Cs1=4.7 nF, 500 V, dipped mica capacitor, ICs1=2.6 A rms
Ds1 is a 4 A, 600 V diode with t_{rr} < 400 ns
Cs2 = 270 pF, 500 V, dipped mica capacitor, ICs2=250 mA rms
Rs2 = 51 Ohm, 10 W, non-inductive resistor

Example 5, a combination turn-on and turn-off snubber

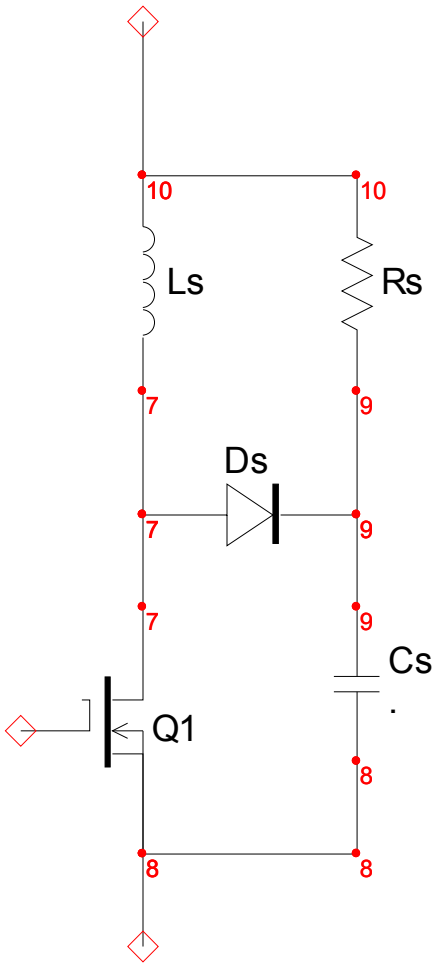


Figure 7-28, a simple combination turn-on, turn-off snubber.

To reduce both turn-on and turn-off losses in Q1 we will need to use a combination snubber that performs both functions. An example of a simple form of combination snubber is given in figure 7-28. In this

snubber a series snubber inductor (Ls) has been added to the RC-diode turn-off snubber and the connection for Rs moved to the top of Ls. This allows Rs to discharge the energy in both Ls and Cs.

This is without a doubt the most common form of combination snubber seen in practice however, I do not recommend using it. The problem lies in the value chosen for Rs. To minimize the turn-on current spike you would like Rs to be large but to minimize the turn-off voltage spike associated with Ls discharge, you would like to make Rs small. The problem is you can't have both simultaneously and, as shown in chapter 4, there is no real optimum, just compromise values for Rs.

The snubber circuit shown in figure 7-29 will allow us to independently optimize performance at turn-on and turn-off. The price is a more complex snubber, with an additional diode and resistor.

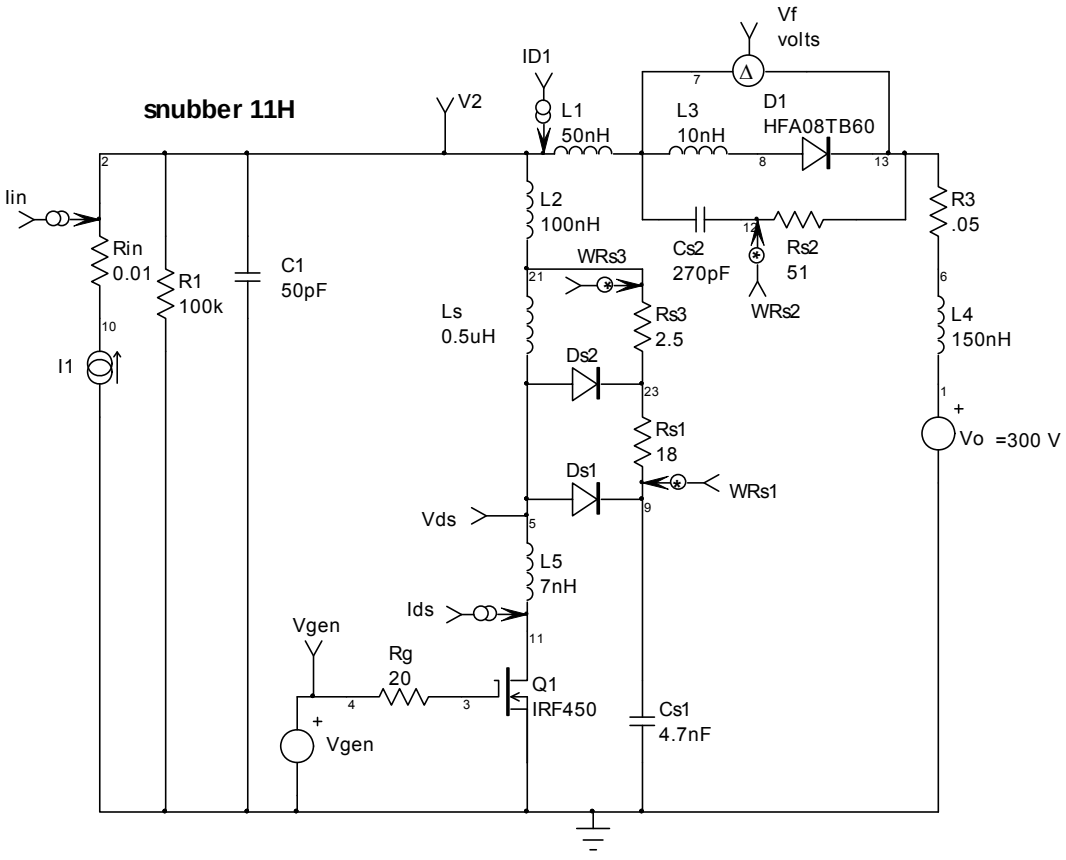


figure 7-29, a better combination snubber.

To determine an appropriate value for Ls we can again turn to McMurray[290]:

$$Ls = \frac{Vo \bullet t_{s-on}}{2Ids}$$

Where Vo is the voltage across Q1 while in the off-state, Ids is the current at the point where Q1 is fully on and $t_{s\text{-}on}$ is the total turn-on time. If we were going to add a RL-diode snubber to the basic circuit as shown in figure 7-4, then we would use the turn-on time shown, $t_{s\text{-}on}$ = 78 ns. But in this example we are adding the RL-diode turn-on snubber to a circuit which already contains an RC-diode turn-off snubber, so we have to use the turn-on waveform from figure 7-23 which is shown expanded in figure 7-30, where $t_{s\text{-}on}$ = 83 ns, Vo = 300 V and Ids = 22 A. From this, Ls=569 nH. For simplicity we will use Ls=500 nH.

Rs3 provides the discharge path for the energy in Ls at Q1 turn-off. The limit on the value for Rs3 is the time available for discharge, which is the minimum off-time for Q1 during normal circuit operation. In this example we will assume that the minimum off-time = 1 us. Nearly complete energy discharge will take about five time-constants so we will set the L/R time constant to be 1/5 us = 200 ns. for Ls= 500 nH and τ=200 ns, Rs3= 2.5 Ohm.

Notice that the discharge resistor for Cs1 (Rs1) has been connected so that it discharges through both Rs3 and Ls. This is done to allow Ls to slow down the discharge pulse rise time while Vds is falling. This helps in reducing turn-on loss. But because Rs3 is now in series with Rs1, it's value is reduced by 2 Ohms to 18 Ohms to keep the time constants essentially the same as in the previous example. Note that the RC-snubber across D1 has been retained.

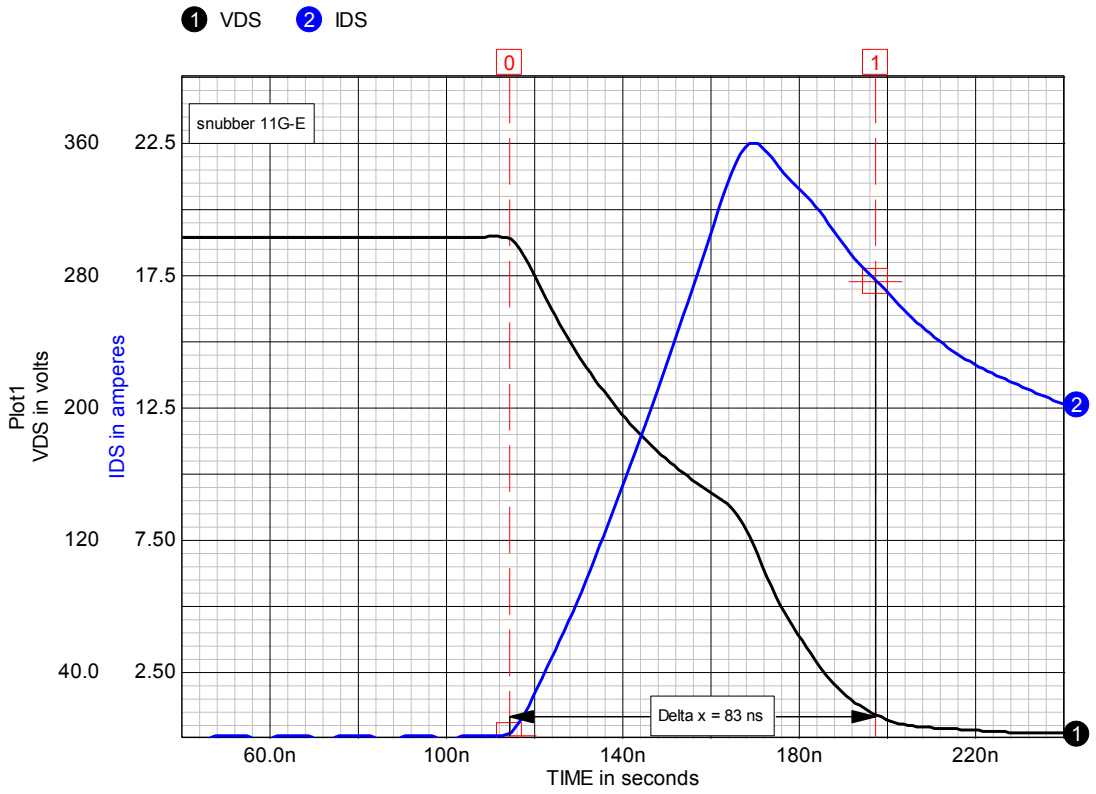


Figure 7-30, expanded turn-on waveforms from figure 7-23.

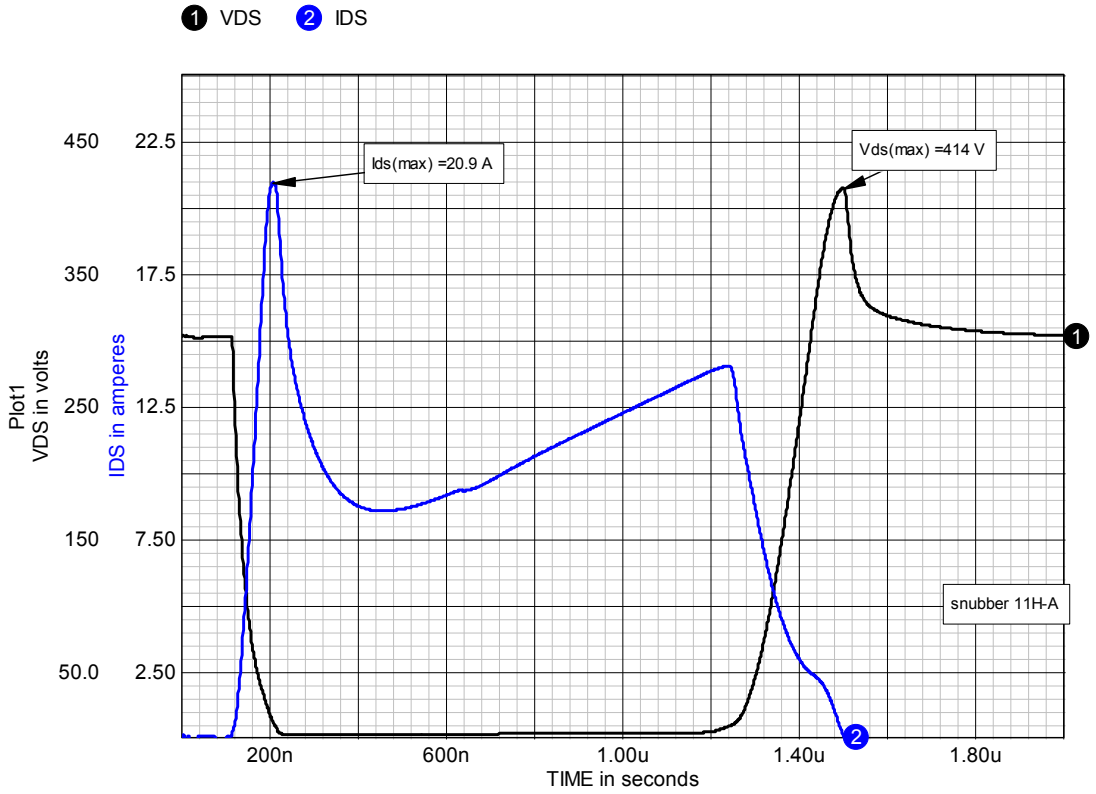


Figure 7-31, Vds and Ids waveforms for the combination snubber.

The power dissipation and load-lines associated with these waveforms are shown in figures 7-32 and 7-33.

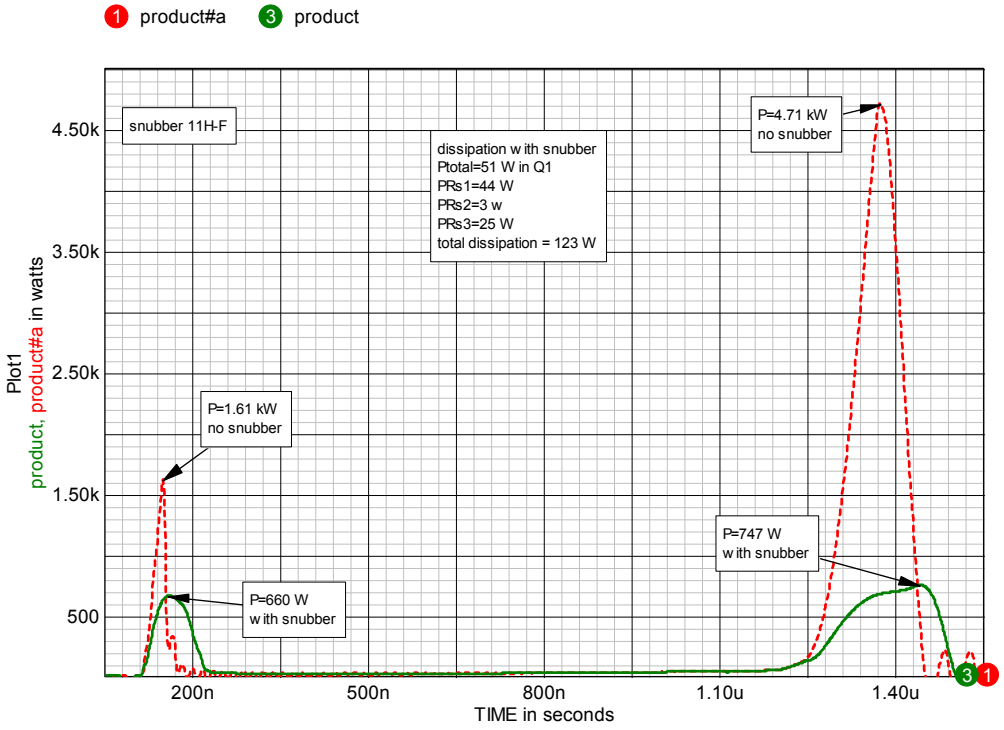


Figure 7-32, power dissipation in Q1 with and without snubber.

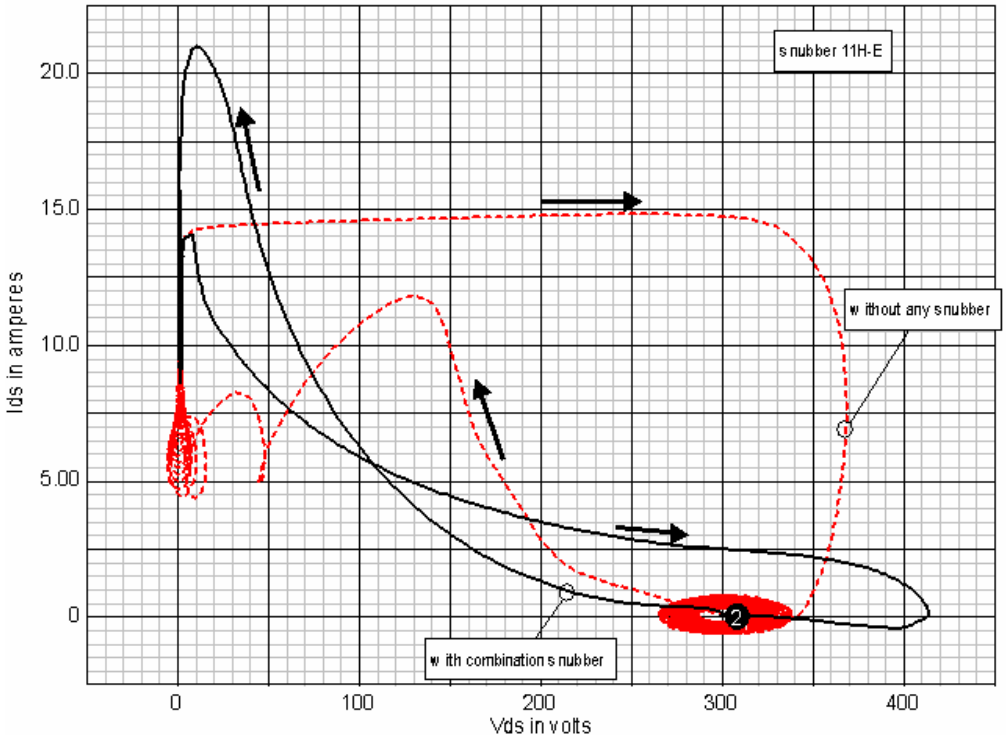


Figure 7-33, Q1 load-line with and without snubber.

Figure 7-32 compares Q1 switch dissipation with and without the combination snubber. With the snubber the peak powers are greatly reduced, especially at turn-off. The average power dissipation in Q1 has dropped from 123 W to 51 W, a 60% reduction. However, the overall circuit dissipation has dropped only slightly due to the dissipation in the snubber resistors.

The load-lines with and without the combination snubber are compared in figure 7-33. In most respects the load-line with the snubber is a significant improvement and Q1 power dissipation is much lower. The price of this improvement is the addition of a current spike at turn-on and a voltage spike at turn-off. These are the undesired side effects of this class of snubber. In addition the overall circuit loss has not improved significantly. If we want to save or recycle the power lost in the snubber resistors then a more complex snubber employing energy recovery will be needed.

Example 5 summary:

Rs1 =18 Ohm, 75 W, non-inductive resistor
Rs2 = 51 Ohm, 10 W, non-inductive resistor
Rs3 = 2.5 Ohm, 50 W, non-inductive resistor
Ds1 and Ds2 are 4 A, 600 V diodes with t_{rr} < 400 ns
Cs1= 4.7 nF, 500 V, dipped mica capacitor, ICs1=2.6 A rms
Cs2 = 270 pF, 500 V, dipped mica capacitor, ICs2=250 mA rms
Ls = 500 nH, I peak = 21 A

Example 6, an energy recovery snubber

There are a host of schemes for energy recovery snubbers, several of which are described in chapter 5 and many more in the bibliography. For this example we will chose one which is in common use and described in detail in chapter 5.

As shown in figures 7-34 and 7-35, this example is a simple combination snubber where the dissipative resistor replaced with an energy recovery circuit.

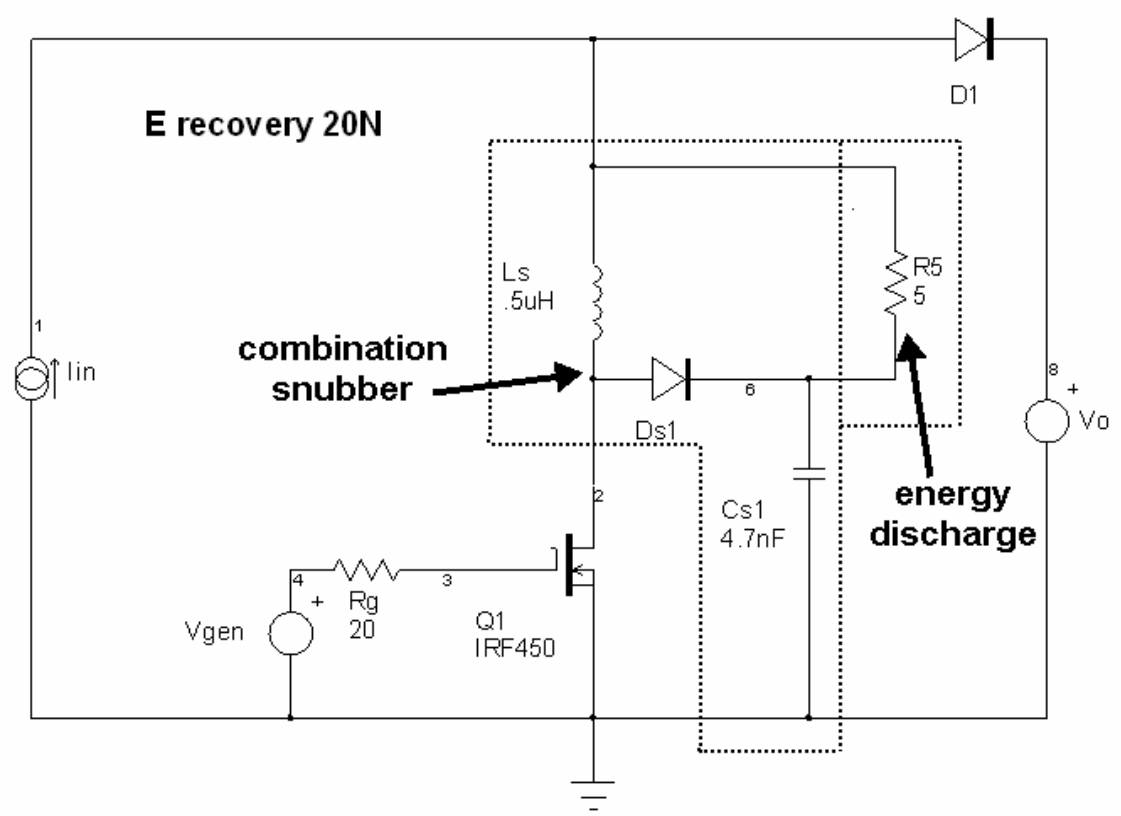


Figure 7-34, a turn-on, turn-off snubber with energy dissipation.

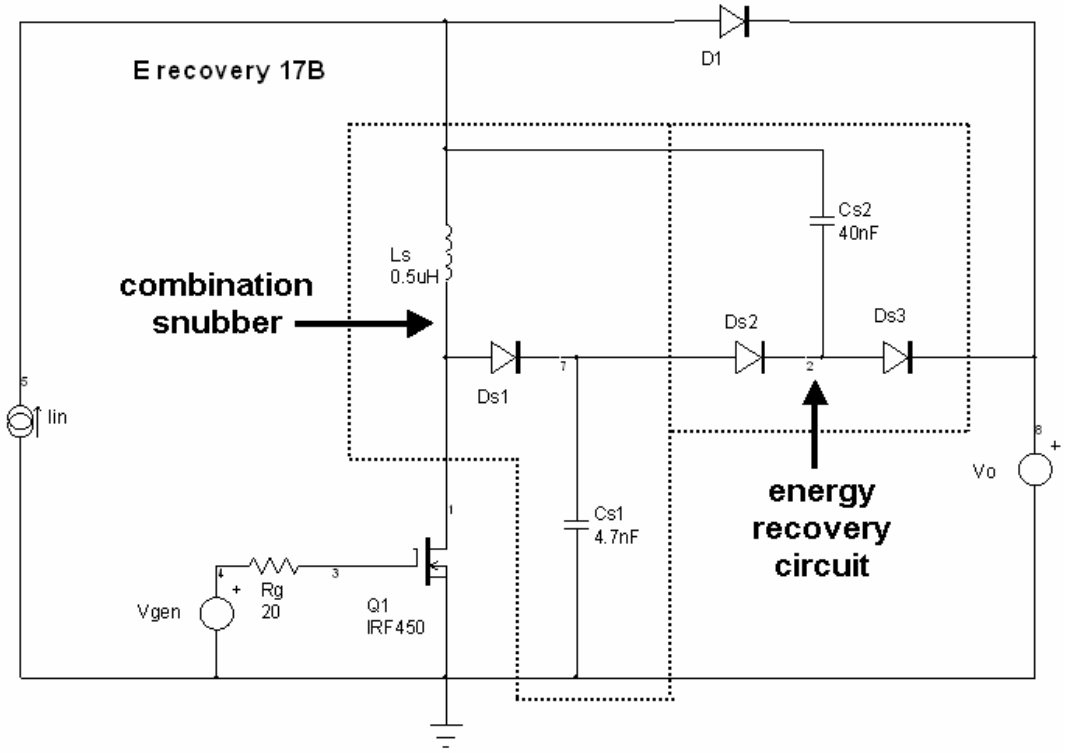


Figure 7-35, a turn-on, turn-off snubber with energy recovery.

Rs is replaced with an energy recovery network consisting of two diodes (Ds2 and Ds2) and an energy storage capacitor (Cs2). As far as the snubbing action on Q1, both circuits are similar so we have retained the original values for Ls and Cs1. The details of the energy transfer in this are discussed at length in chapter 5.

Vds and Ids waveforms associated with this snubber are shown in figure 7-36.

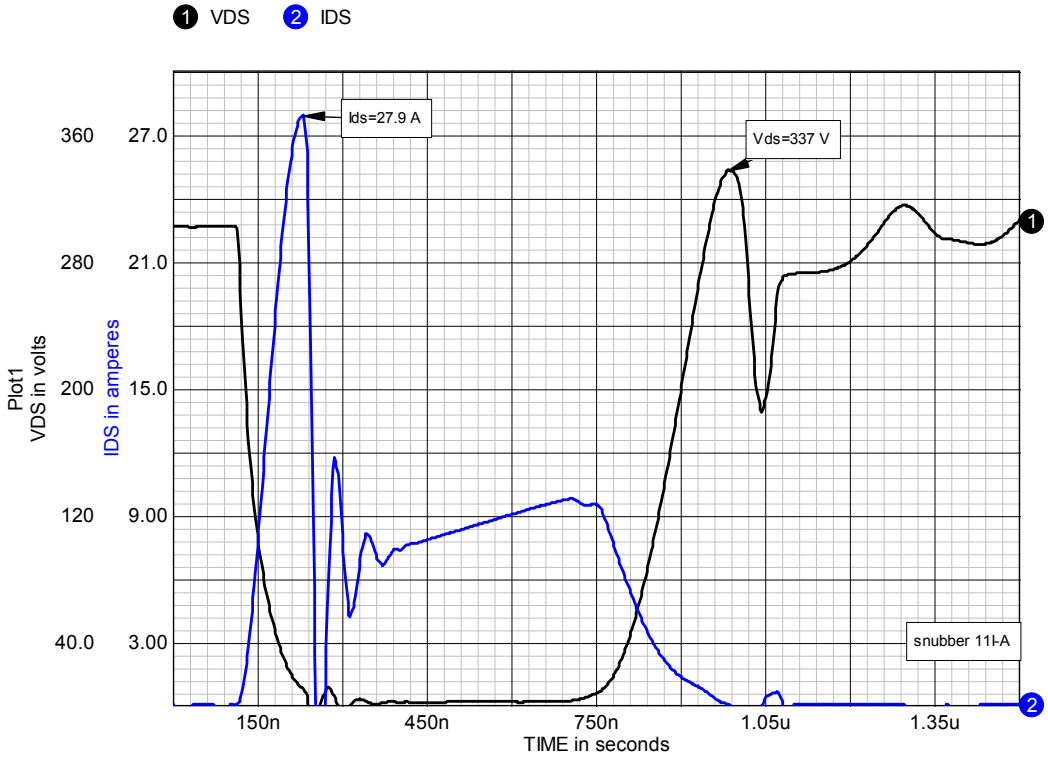


Figure 7-36, waveforms for the energy recovery snubber.

Both voltage and current waveforms display undesirable ringing. This is typical of energy recovery snubbers because they usually minimize resistive loss elements (that might provide damping) to maximize efficiency. As a practical matter, it is usually necessary add some dissipative damping to energy recovery snubbers. The damping arrangements will vary with the circuit and the parasitic inductances present. Usually some trial and error is needed to arrive at suitable damping.

The Ids ringing is due to the resonance between Ls and Cs1 at the end of Cs1 discharge. We can reduce this ringing by adding a small

amount of resistance (Rs1=1 Ohm) in series with Cs1 as shown in figure 7-37.

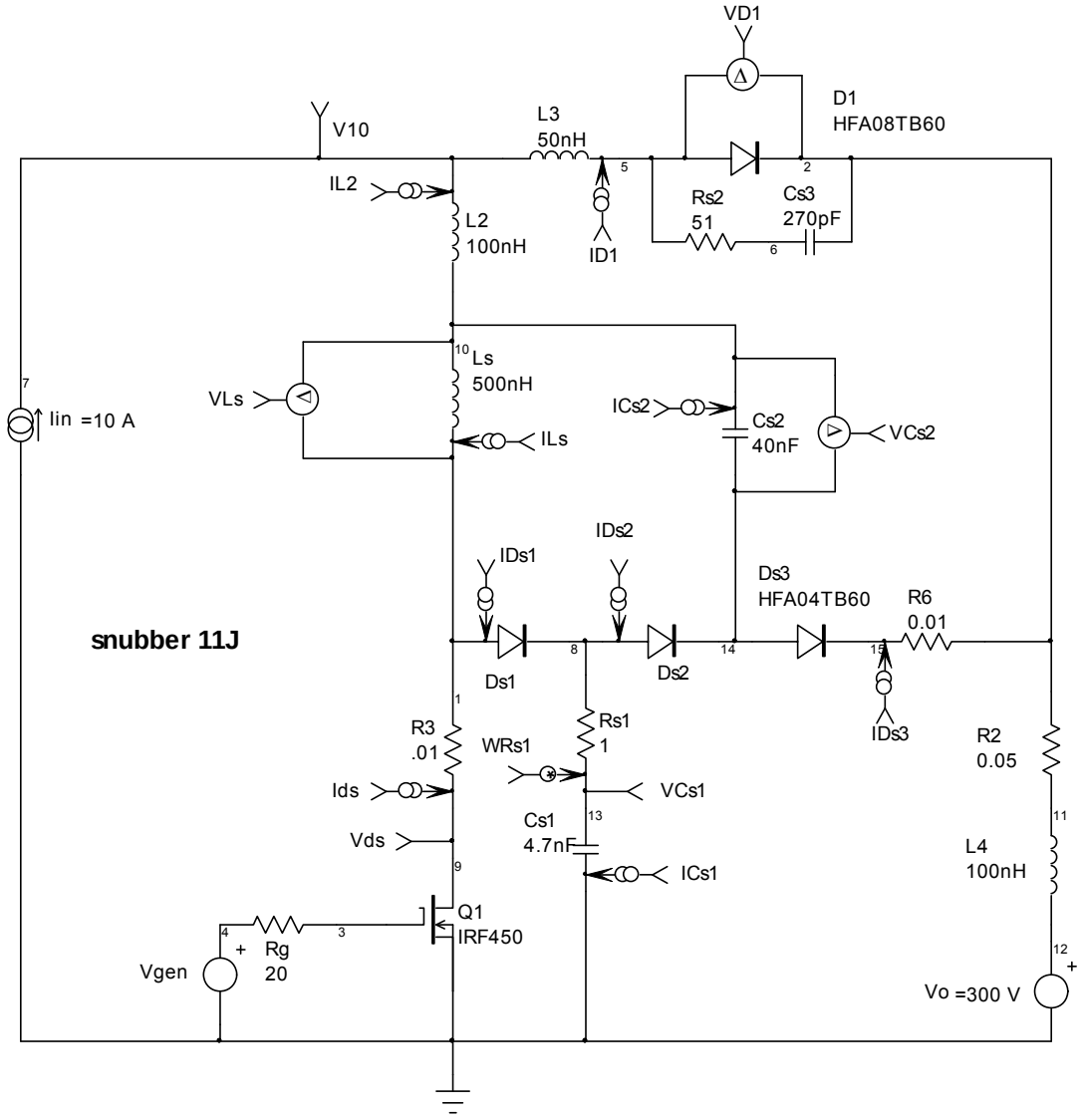


Figure 7-37, adding Rs1 in series with Cs1.

The Vds and Ids waveforms with Rs1 added to the circuit are shown in figure 7-38. The Ids ringing is now well damped but the Vds ringing at turn-off is somewhat worse. In addition if we look at the voltage across D1 we see that adding Rs1 has introduced voltage ringing on D1 that was not present without Rs1 (the two waveforms are compared in figure 7-39). We can attack this problem by putting the RC-snubber (Rs2 and Cs3) back in the circuit as shown in figure

7-37. The new waveform for VD1 is shown in figure 7-40. VD1 is now well damped.

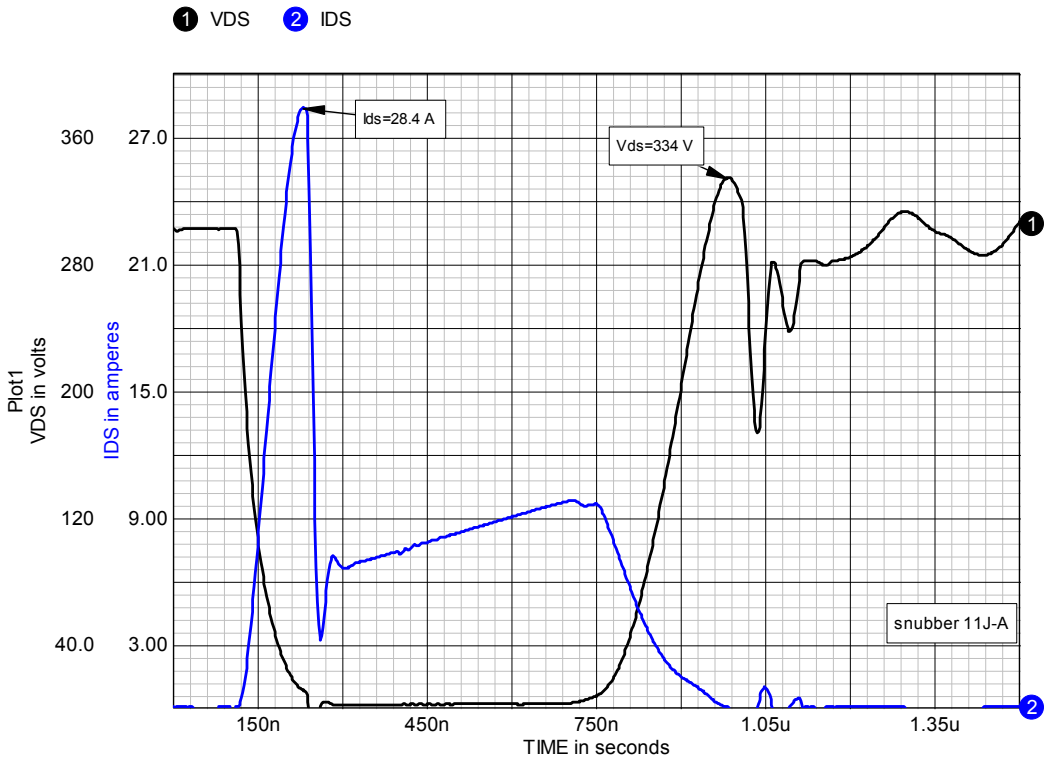


Figure 7-38, Vds and Ids with Rs1 added in series with Cs1.

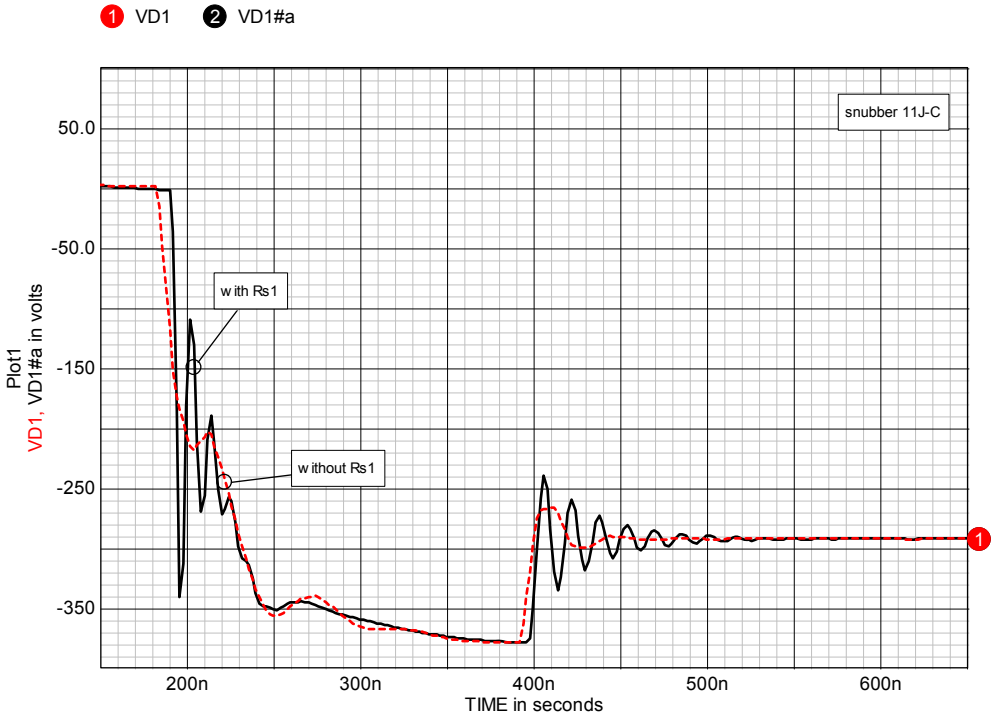


Figure 7-39, voltage waveform across D1 with and without Rs1.

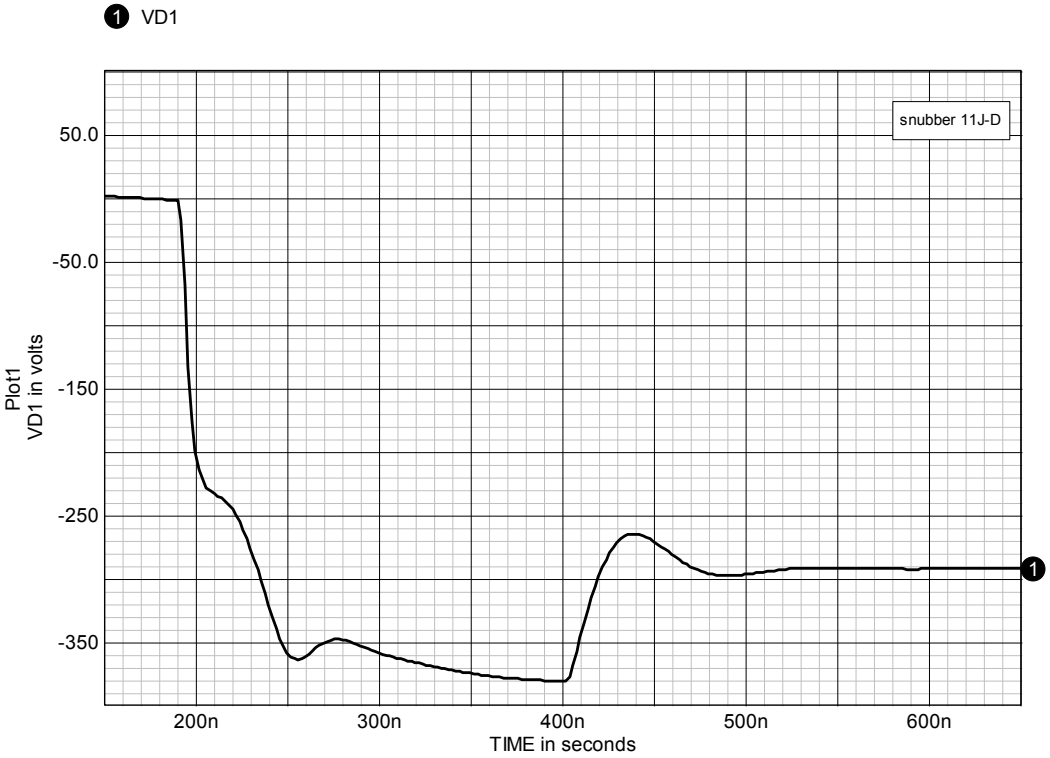


Figure 7-40, voltage across D1 with both Rs1 and the RC-snubber across D1 added to the circuit.

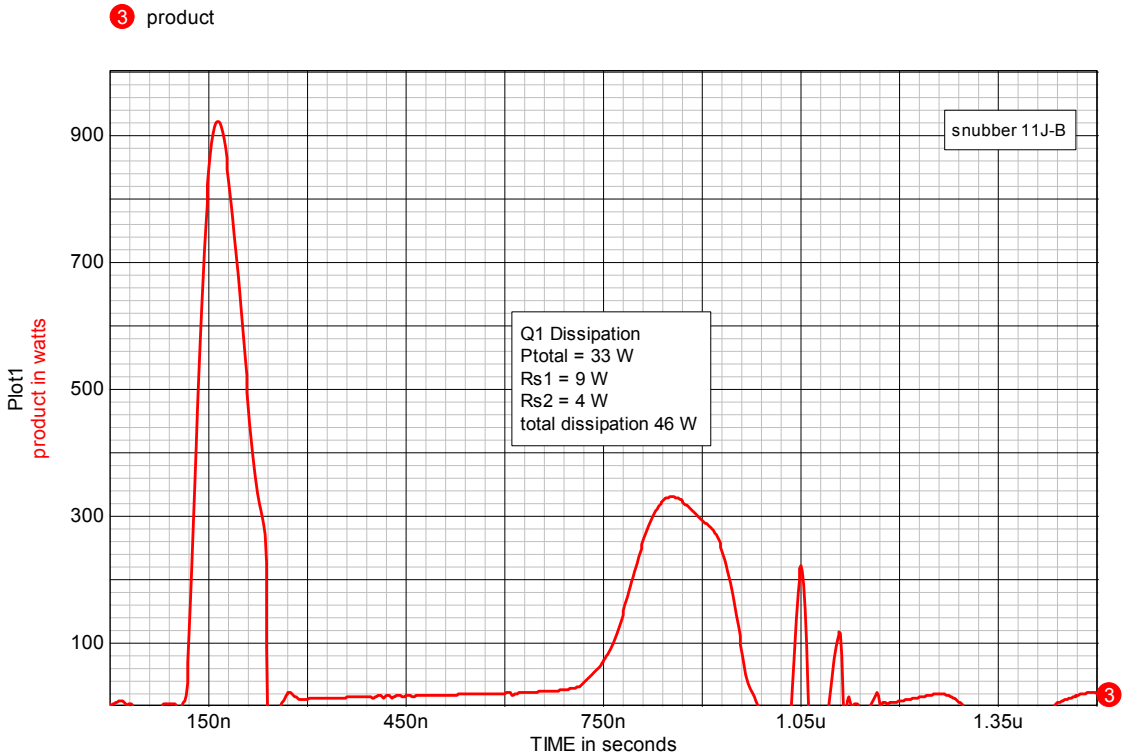


Figure 7-41, power dissipation in Q1, Rs1 and Rs2.

Now it's time to see if we have gained anything over the dissipative combination snubber. Figure 7-41 shows the instantaneous and average power dissipations for Q1 and the average power loss in Rs1 and Rs2. The total power dissipation in Q1 is now down to 33 W from 126 W without a snubber and 44 W with the combination snubber. The total power dissipation in Rs1 and Rs2 is 13 W, which is the price of adding damping to the circuit. The overall circuit loss has now been reduced from 126 W to 46 W, which is a 63% reduction. This amounts to an improvement of overall efficiency of about 3% for a 2 kW output load. In many applications this would be a worthwhile improvement.

The values for Cs1 and Ls were chosen to be the same as for the earlier dissipative snubbers and do provide good performance. However, the large Ids current spike at Q1 turn-on due to Cs1 discharge could be reduced by using a larger value for Ls. Figure 7-42 shows Vds and Ids waveforms with Ls = 1 uH. Ids peak is reduced to 24 A and Q1 total loss reduced another 12 W to 21 W.

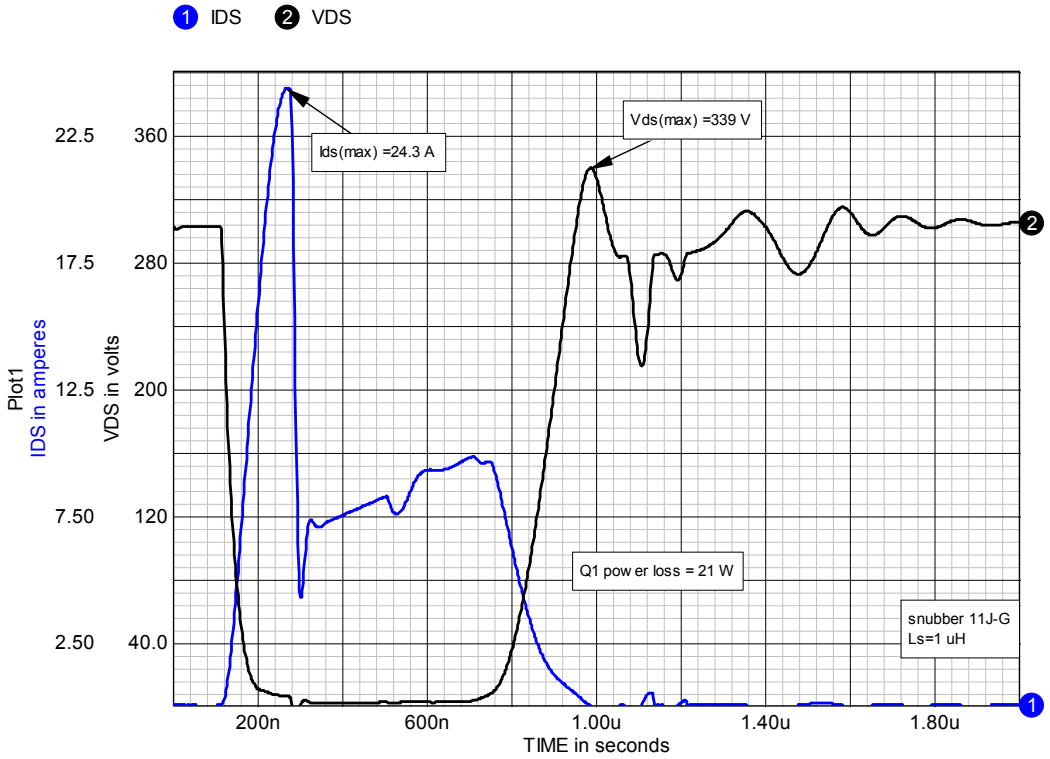


Figure 7-42, Vds and Ids waveforms for Ls = 1 uH.

The load-line for Q1 with Ls = 1 uH is shown in figure 7-43.

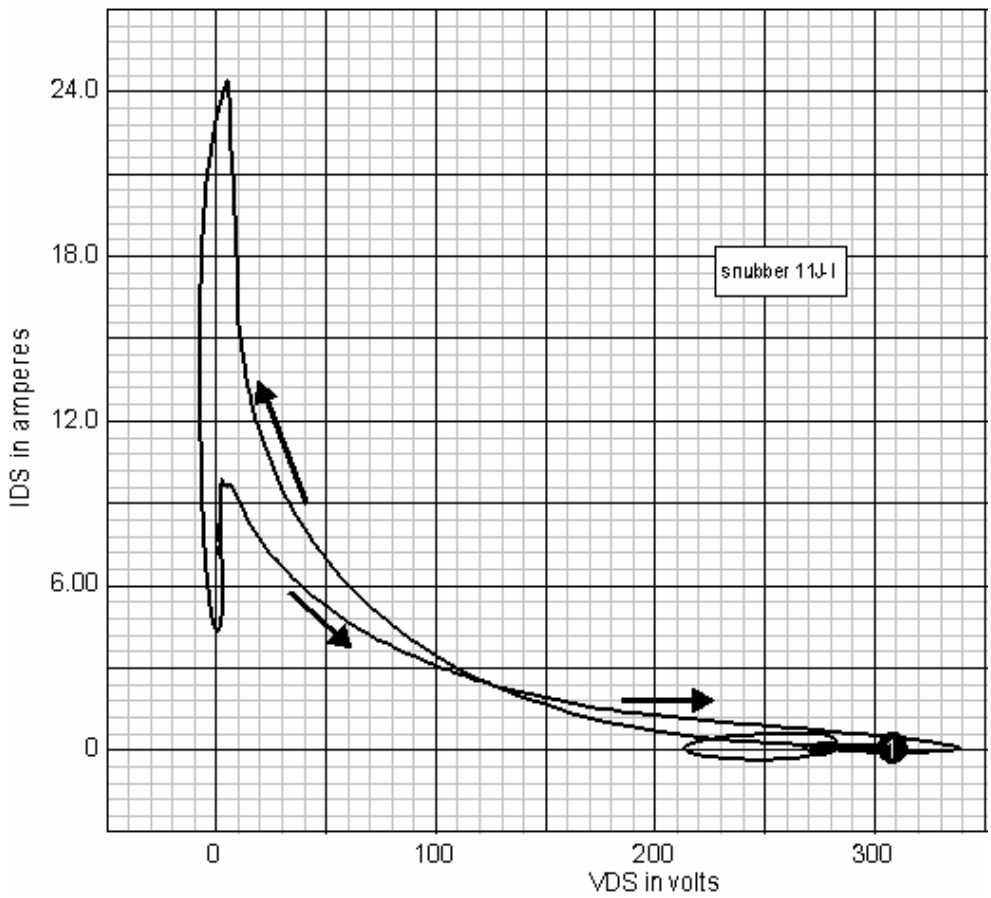


Figure 7-43, load-line for Q1 with Ls = 1 uH

Overall this is a very soft load-line, with minimal stress on Q1. There is still some ringing at turn-off which you may elect to damp further but it does not appear to be serious. The far left side of the load-line goes negative about 15 V. This is due to the interaction of the rapid negative d(Ids)/dt at the end of Cs1 discharge and the package inductance (L=8 nH included in the IRF450 model). The transition is very rapid (20 A in roughly 10 ns) and is not clamped by the internal body-drain diode. This appears on the Vds waveform in figure 7-42 as a small negative bump coincident with the rapid fall of Ids.

Component values

In this snubber the initial values for Ls and Cs1 are usually chosen in the same manner as for the combination snubber, although, as shown above, due to the Ids current spike introduced by the reset of Cs1, a larger value for Ls is often employed.

Some care must be taken in the design of Ls due to the nature of the current waveform in it. The ILs waveform is shown in figure 7-43.

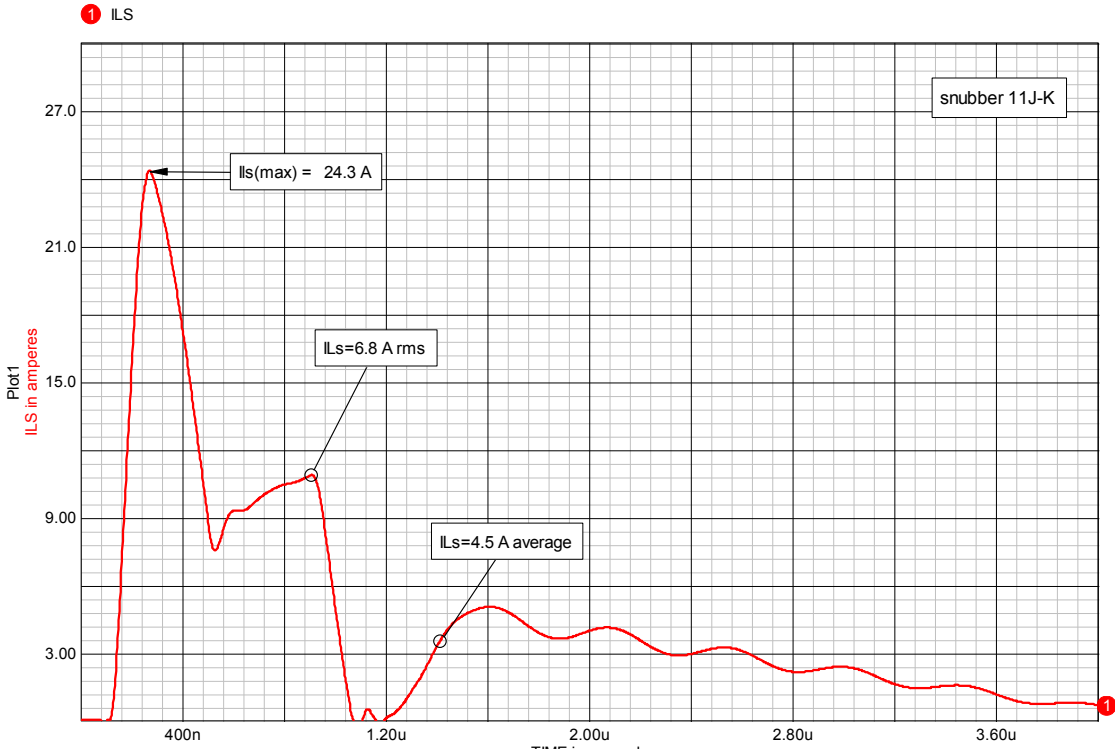


Figure 7-43, Ls current waveform.

ILs has a peak value of 24.3 A, a DC (average) value of 4.5 A and an rms value of 6.8 A.

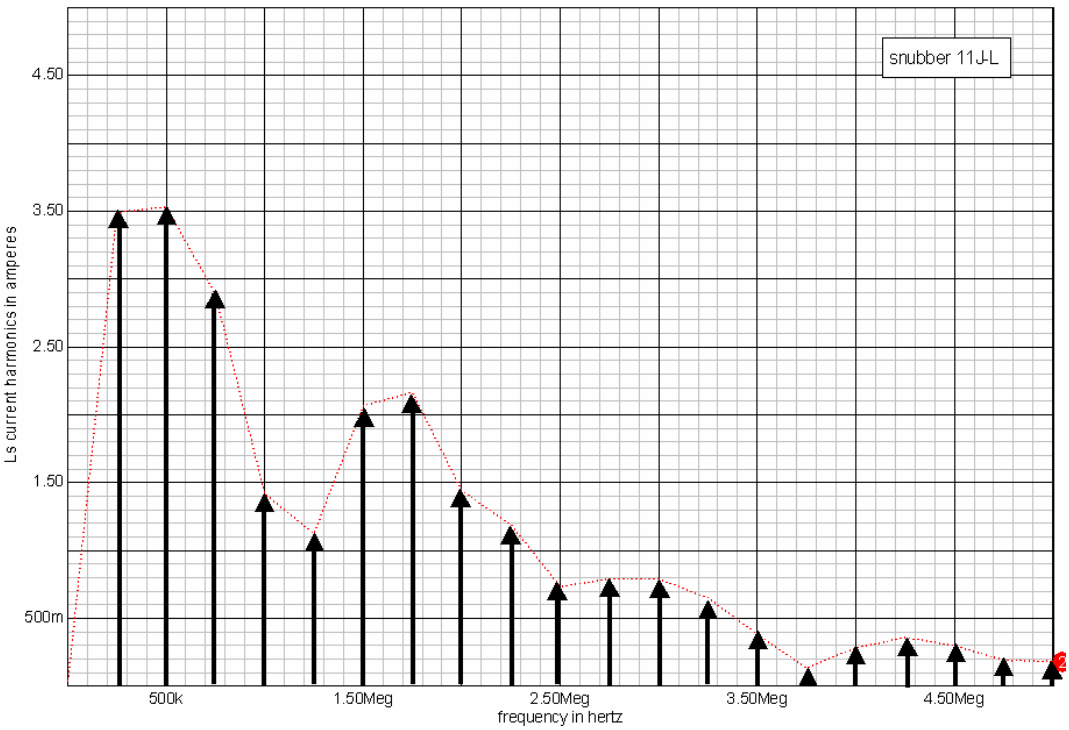


Figure 7-44, frequency spectrum of Ls current.

The spectrum of the current waveform in Ls is shown in figure 7-44. Clearly there is substantial harmonic current.

In this snubber, Cs2 is usually chosen to be 8-10X Cs1. In figure 7-37 Cs2=40 nF, which is approximately 8X Cs1. The value is not critical. Further discussion on the choice of value is provided in chapter 5. Cs3 is the same as in the earlier RC-snubber examples across D1.

Example 6 summary:

Cs1 = 4.7 nF, 500 V, dipped silver-mica capacitor, I = 2.9 A rms (note: this current level is near the maximum for this type of capacitor, parallel smaller capacitors or a polypropylene-foil capacitor may be needed)
Cs2 = 40 nF, 500 V, polypropylene-foil capacitor, I = 5.4 A rms
Cs3 = 270 pF, 500 V, dipped silver-mica capacitor, I = 250 mA rms
Ls = 1 uH, ILs peak = 25 A, 6.8 A rms and 4.5 A average.
Rs1 = 1 Ohm, 20 W, non-inductive
Rs2= 50 Ohm, 10 W, non-inductive
Ds1, Ds2 and Ds2 = 4 A, 600 V diodes with t_{rr} < 400 ns

Summary

This completes the "bare bones" discussion on snubber design and, as advertised, it was a very quick tour. This chapter may be just what you need when in a crunch but to prepare for the next project, you would do well to read the more complete explanations given in other chapters. Reading those chapters will give you a much better understanding of the reasons for the rules of thumb used in this chapter and also provide many additional options for your next design.

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