

A NEW CURRENT-FED CONVERTER TOPOLOGY

Rudolf P. Severns

Intersil, Inc.

Abstract

A current-fed regulating converter using a new topology is described. The circuit uses a novel switching scheme to increase the line voltage operating range. The converter circuit is shown to be one member of a family of circuits, each a little different from the others but sharing common characteristics.

1. INTRODUCTION

In recent years, a number of new current-fed converter circuits have been presented^[1-8]. These circuits have been well received because they provide significant advantages over more conventional circuits in many applications. As would be expected, the present family of current-fed converters have disadvantages, as well as advantages. Some of the circuits display poorly controlled inrush current at turn-on or designed in upper and lower limits on line voltage, others require the use of multiple winding chokes for multiple outputs or complex tapped chokes and transformers. A few circuits have two or more switches in series, which reduce the conversion efficiency in low voltage applications. The circuits described here are an attempt to overcome these problems while retaining the advantages of earlier current-fed converters. The topology chosen for this discussion is not necessarily the best or most useful member of the family, however, it is neither patented (to the best of the author's knowledge) nor proprietary and so is available for unrestricted use by designers.

2. CIRCUIT DESCRIPTION

The circuit is shown in Figure 1. Switches S1 and S3 are pulse width modulated while switches S2 and S4 conduct alternately with a 50% duty cycle. The pulse width modulated switches have two modes of

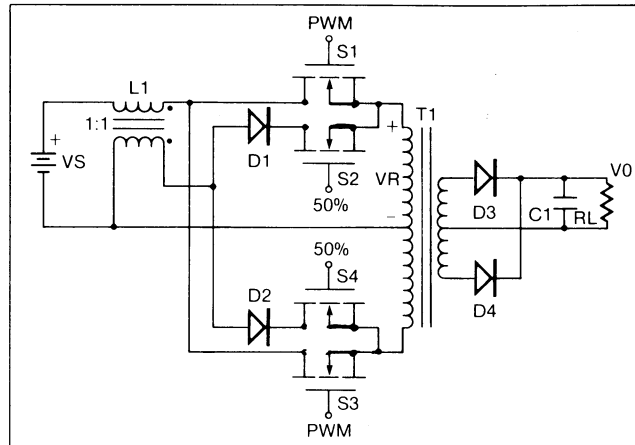


Figure 1

operation:

- A) The duty cycle of S1 and S3 is less than 50% (individually) or
- B) The duty cycle of S1 and S3 is greater than 50%. This is the case where S1 and S3 are deliberately in simultaneous conduction.

Mode A operation prevails when V_S is greater than V_R . The conduction for this mode is shown in Figure 2. At the beginning of the cycle, S1 and S2 are closed and current flows from the source through L1, S1, and the primary of T1. The current in the primary of T1 is reflected into the secondary to charge C1. In state I, energy is being delivered to the load and stored in L1. Note that S2 takes no active part in state I because D1 is reverse biased and S2 need not be driven. However, it is usually simpler to drive S2 (and S4) with a 50% duty cycle rather than to develop a four phase drive to turn on the switches individually.

At the end of state I, S1 is opened and the energy stored in L1 is discharged through S2 and coupled

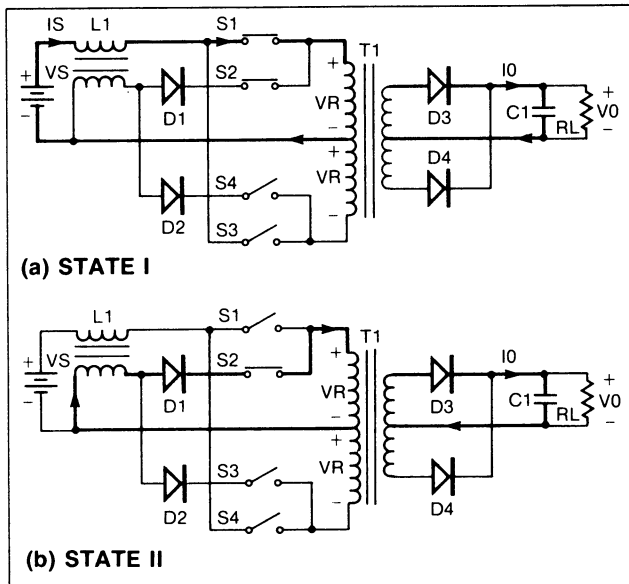


Figure 2, Mode A Operation

to the secondary by T1. States I and II are then repeated by S3 and S4 to complete the cycle. During mode A operation, the circuit displays buck regulator like properties in that the output current is continuous and the input current is discontinuous. In addition, like a buck regulator, the turn-on inrush current is completely controlled by the conduction time of S1 and S3 so that no inrush spike need exist at turn-on. Figure 3 shows the mode A waveforms for $V_R = 25V$ and $V_S = 30V$.

Mode B prevails when V_S is less V_R . The conduction sequence for this mode is shown in Figure 4. At the beginning of the cycle, S1 and S3 are closed (the state of S2 and S4 is irrelevant) effectively short circuiting the primary of T1. Essentially, the entire supply voltage appears across L1 which begins storing energy. At the end of state I, S3 is opened and L1 discharges through S1 and the primary of T1, delivering current to the secondary and C1. The roles of S1 and S3 are interchanged and states I and II repeated to complete the operating cycle. During the entire mode B cycle, D1 and D2 are reverse biased so that S2 and S3 play no part in the circuit operation. For mode B, the circuit may be simplified to that shown in Figure 5, in which V_R is always greater than V_S and regulation is achieved by varying the conduction overlap of S1 and S2. This circuit displays characteristics like a boost

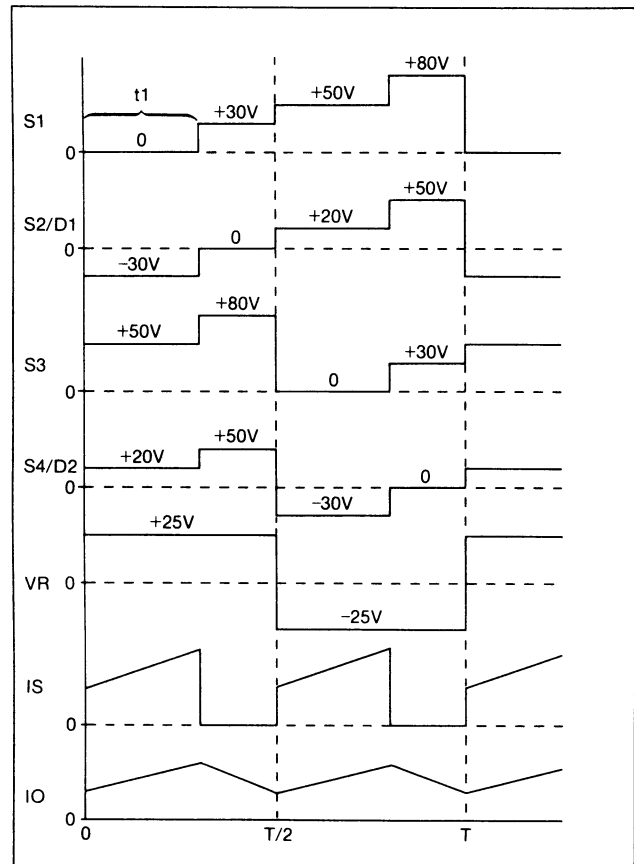


Figure 3, Mode A Waveforms

regulator, the input current is continuous and the output is discontinuous. As in the case of the boost regulator, at turn on, there will be a current inrush transient until $V_R = V_S$.

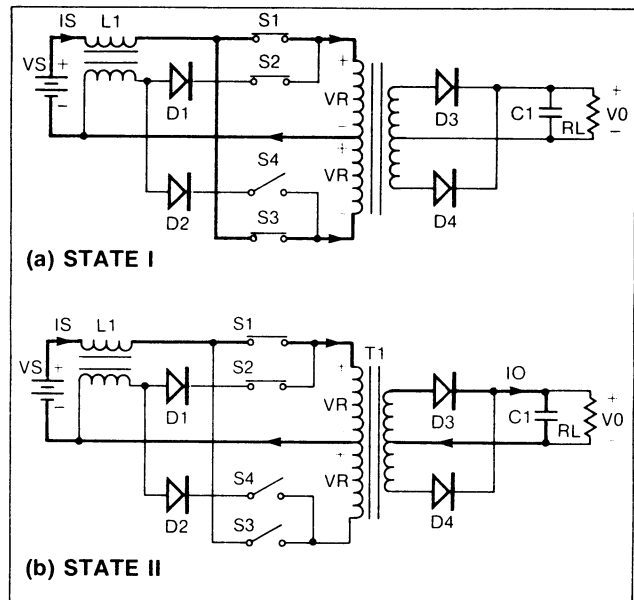


Figure 4, Mode B Operation

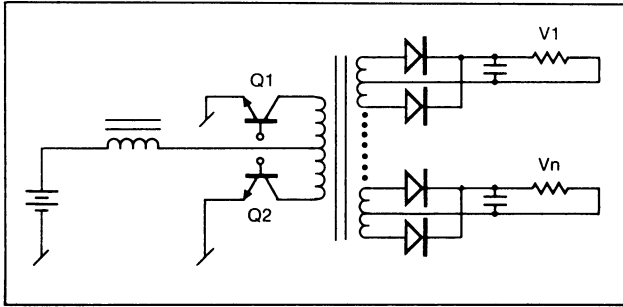


Figure 5, Boost Converter

The current and voltage wave forms for Mode B operation, are shown in Figure 6 for $V_S=20V$ and $V_R=25V$.

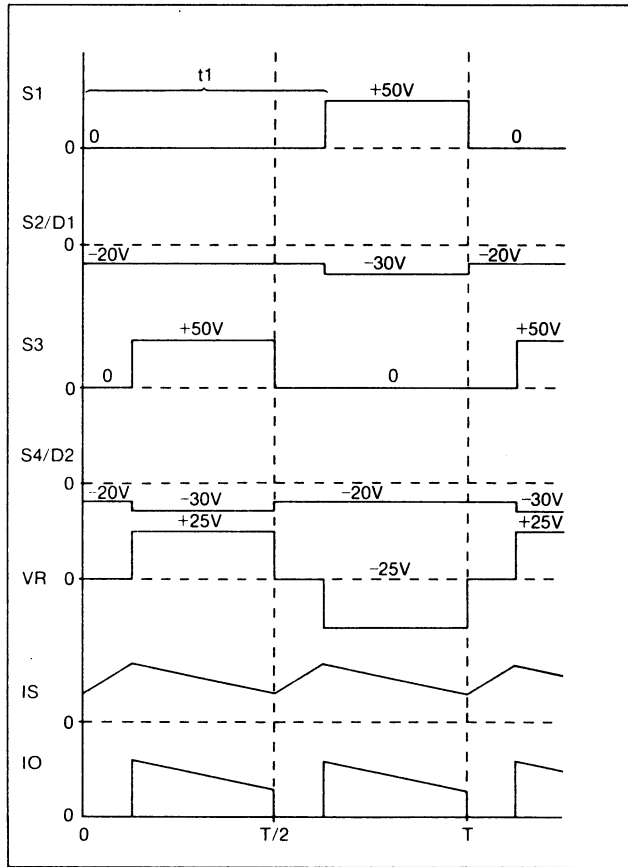


Figure 6, Mode B Waveforms

3. CIRCUIT PROPERTIES

To make this paper reasonably readable, the derivation of the circuit equations have been omitted. The following discussion should serve to illuminate the circuit properties. The comments are for the continuous inductor current case, with V_O , R_L and C_L reflected to the primary.

3.1 DUTY CYCLE

The switch states for modes A and B are shown in Figures 7 and 8. If one defines the duty cycle, D as:

$$D = \frac{t_1}{T} \quad (1)$$

Then the duty cycle, as a function of V_S and V_O , can be shown to be:

$$\text{Mode A, } D = \frac{V_R}{2 V_S} \quad (2)$$

$$\text{Mode B, } D = \frac{2 V_R - V_S}{2 V_R} \quad (3)$$

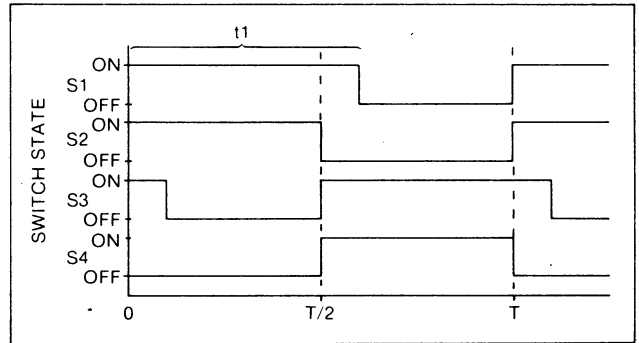


Figure 7, Mode B Switch States

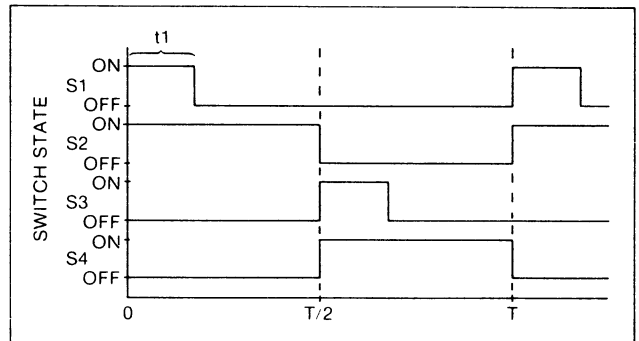


Figure 8, Mode A Switch States

For simplicity, this derivation has ignored the switch and diode voltage drops. However, in a high efficiency converter, this is not an important error.

3.2 CRITICAL INDUCTANCE

In order to maintain continuous inductor current, a minimum value for L_L , L_C , is required. The value can be shown to be:

$$\text{for Mode A, } L_C = \frac{V_R(V_S - V_R)T}{4 P_L} \quad (4)$$

$$\text{for Mode B, } L_C = \frac{V_S^2(V_R - V_S)T}{4 P_L V_R} \quad (5)$$

Where PL is the minimum load power. Again, for simplicity, the circuit losses have been omitted. An inspection of equation (4) shows that the largest value of LC occurs at the maximum value for VS. By differentiating equation (5), the maximum value for LC in mode B can be shown to be at:

$$VS = \frac{2VR}{3} \quad (6)$$

If both mode A and B operation is desired, then the designer should calculate the values for LC in both modes and choose the larger of the two.

3.3 TRANSFER FUNCTIONS

By using the modeling techniques developed by Wester and Middlebrook^[10] the circuit transfer functions are readily derived. These are summarized in Table I using the same conventions as Wester and Middlebrook:

Table I

	Mode A	Mode B
A_{so}	2D	1/2D'
A_{co}	VS	$\left[\frac{(2D')^2 RL' - 2(D-D') RL'}{(2D')^2 RL' + RL} \right] \frac{VS}{(2D')^2}$
G_{fo}	$\frac{RL'}{RL' + RL}$	$\frac{RL'}{RL' + RL / (2D')^2}$
w_o	$\frac{1}{\sqrt{LIC'}} \sqrt{\frac{RL' + RL}{RL' + RC'}}$	$\frac{1}{\sqrt{LIC'}} \sqrt{\frac{(2D')^2 RL' + RL}{RL' + RC'}}$
w_z	1/RC C1	1/RC C1
w_a	∞	$\frac{(2D')^2 RL' - RL}{LL}$

The equations in Table I include the effect of the inductor series loss resistance, RL, and the output capacitor ESR, RC. These equations differ only slightly from those derived by Wester and Middlebrook for the buck (Mode A) and boost (Mode B) converters. The differences are due to the differences in defining the duty cycle and the need to reflect the secondary circuit impedances into the primary where:

$$RL' = \left(\frac{n_p}{n_s} \right)^2 RL,$$

$$RC' = \left(\frac{n_p}{n_s} \right)^2 RC,$$

$$\text{and } C' = \left(\frac{n_s}{n_p} \right)^2 C1$$

3.4 OVERLAPPING CONDUCTION

The use of deliberate switch overlap is not particularly common in switchmode converters but, as the foregoing example has shown, very interesting circuit performance can be achieved by its use. By using a control loop that provides a 0 to 90-95% duty cycle drive for S1 and S3, one has a converter that is a boost regulator at low line and a buck regulator at high line with no built-in restrictions on line voltage range other than the current and voltage limitations of the components.

It appears that the use of overlapping and non-overlapping conduction (depending on the input line voltage) is generally applicable to most current-fed switchmode converters and by no means restricted to this particular topology. This could be very useful in converters that have relatively restricted nominal line excursions but are subjected to large transients such as are common in space and military applications. For this type of application, the designer would make VR close to the nominal low line voltage so that transients below nominal line would be handled with mode B operation. Mode B operation does have higher output ripple but most loads will tolerate this during transients.

3.5 TURN-ON INRUSH CURRENT

At initial turn-on, VR is zero, presuming the control loop reference is ramped up slowly the converter will come on in mode A and stay in that mode until (and if) VR exceeds VS when mode B operation will begin. The result can be a total absence of turn-on inrush current overshoot above the nominal current corresponding to the load power.

3.6 EFFICIENCY

In practice, breadboard versions of the circuit have proven to be very efficient, especially when used for high voltage converters. The reasons for this are fairly obvious. At low line, very little energy is stored in L1 and most of the input ener-

gy is passed directly to the secondary. As V_S rises, D1 and D2 begin to conduct and the efficiency decreases but this loss remains relatively small due to the small conduction duty cycle of D1 and D2 for the usual nominal line variations. The continuous current nature of the waveforms in the windings of T1 minimizes the RMS value of the currents so the copper utilization is excellent. The continuous current also minimizes the losses in D3 and D4 and the ESR loss in C1. The absence of current spikes during switch transitions also contributes materially to lower losses. The net result of these effects is very high efficiency.

4.0 BREADBOARD CIRCUIT

To verify the circuit operation, a breadboard 300 kHz, 80 W converter was built. The circuit arrangements are shown in Figures 9 and 10 where

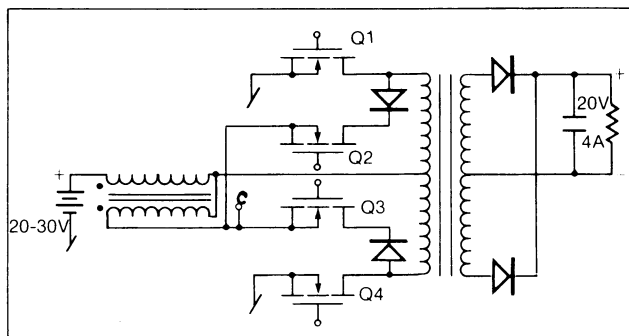


Figure 9, Test Converter

for convenience a circuit variation allowing Q1 and Q3 to be referenced to ground was used. The circuit functioned as predicted with the only problem oc-

curing in the overlapping conduction mode due to the primary to secondary leakage inductance. During overlap, the current in the leakage inductance is interrupted and when one switch is opened cannot be instantaneously re-established. The result is a voltage spike that must be clamped by some form of snubber network. The leakage inductance between the primary windings is also the source of a voltage spike at the end of overlap which must be snubbed. In HV applications, a current spike due the winding capacity can occur. At 20 kHz, these effects need not be serious but at 300 kHz, very careful attention to coupling within T1 is required.

5. CIRCUIT VARIATIONS

As was stated in the introduction, the circuit that has been discussed is only one member of a family of circuits all of which behave alike electrically but which have topology variations that separate them. The following is a brief discussion of some of the other members of the family. Either bipolar or power MOS switches may be used.

5.1 SINGLE WINDING CHOKE

It is not necessary to use a dual winding choke as the circuit on Figure 11(a) shows. By moving the connection point of Q1 and Q3, the circuit in Figure 11(b) is obtained. This circuit can be reduced to the TRW converter topology^[3] but in this form divides the dissipation equally in two devices without any special effort and easily provides for 100% on time with transformer isolated base drive. In this circuit (b) two of the switches see only

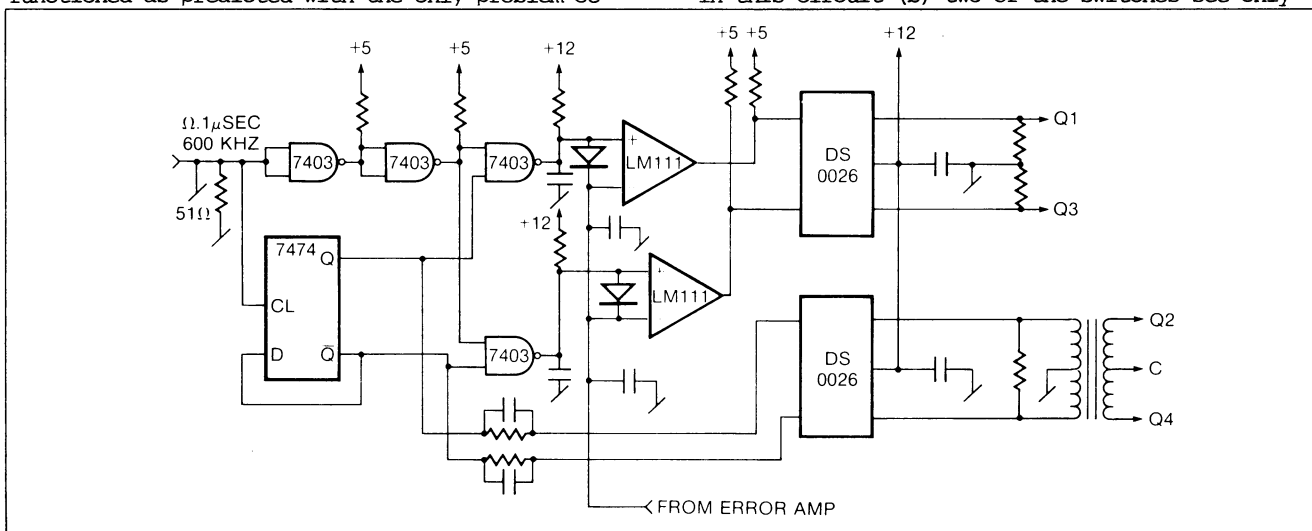


Figure 10, Gate Drive Circuit and Pulse Width Modulator

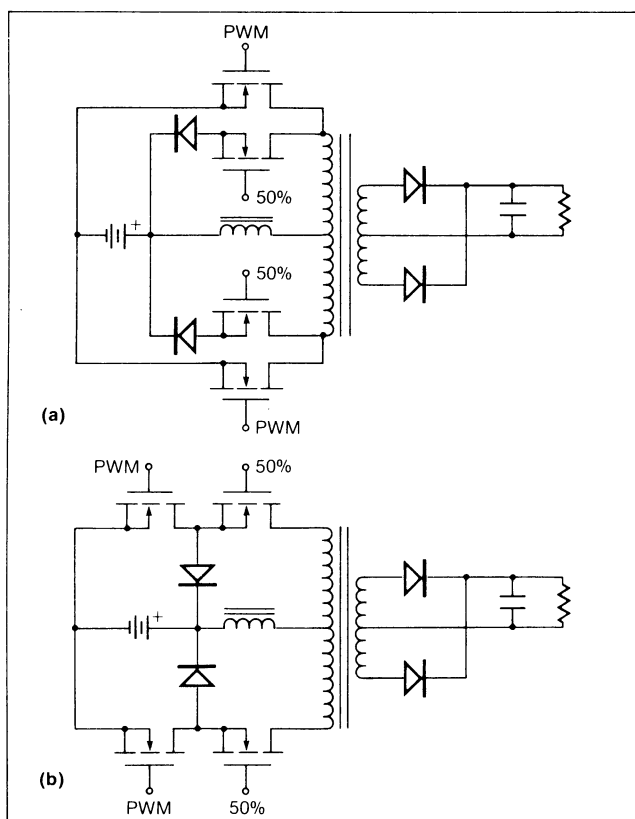


Figure 11

see only the line voltage and the other two see $2V_R$. This circuit should be superior to the quasi-squarewave bridge converter for most applications, however it is patented^[9].

5.2 DUAL WINDING CHOKE BRIDGE CONNECTIONS

Bridge versions of the split choke topology are also possible as shown in Figures 12 and 13. The circuit in Figure 12 will provide performance equal to that of Figure 11(b) but at the price of a more complex choke.

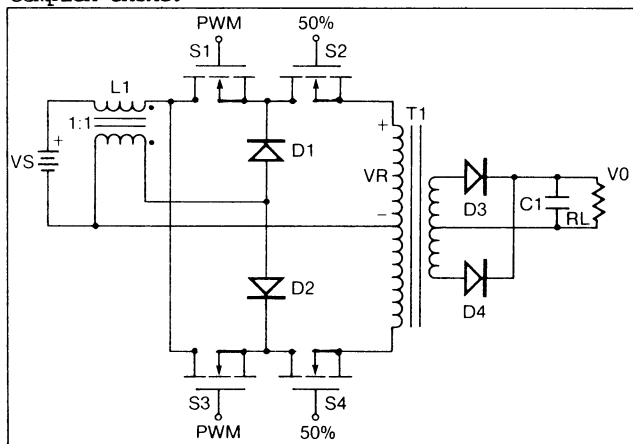


Figure 12

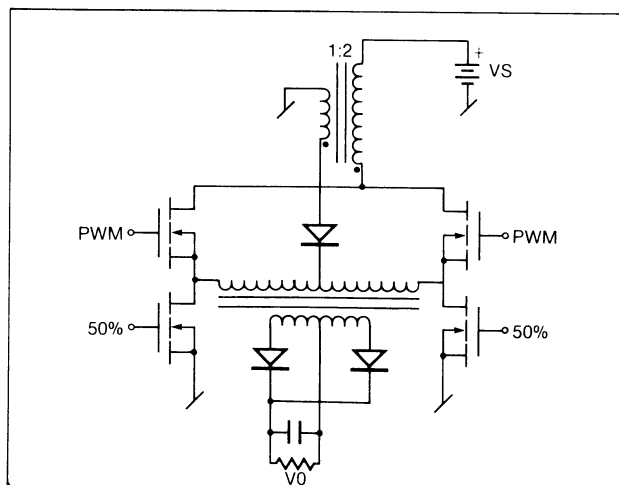


Figure 13

The circuit in Figure 13 has no special utility but is presented here for the sake of completeness.

5.3 HIGH EFFICIENCY VARIATION

If the utmost in conversion efficiency is required the circuit in Figure 14 can be used. The choke and the transformer are tapped to reduce the diode current and losses during the choke discharge interval. The circuit bears a resemblance to the Hughes converter^[1,2] but it is fundamentally different in that it is buck rather than boost derived. As such, it has no inrush current problem, the maximum line voltage is not limited by the tap ratio and the duty cycle variation over full line is greatly reduced.

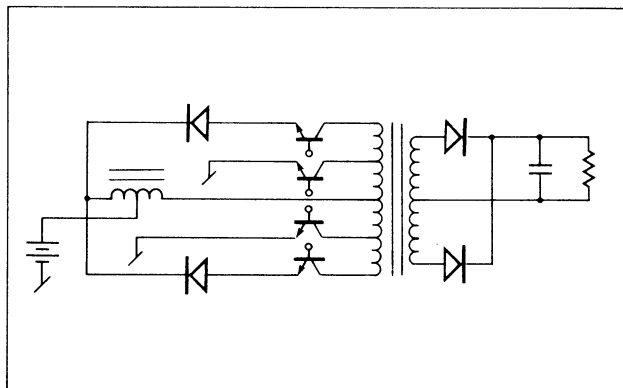


Figure 14

5.4 OTHER VARIATIONS

Figures 15, 16 and 17 show some other members of the family. For the most part they have no real advantages except that they are probably not yet

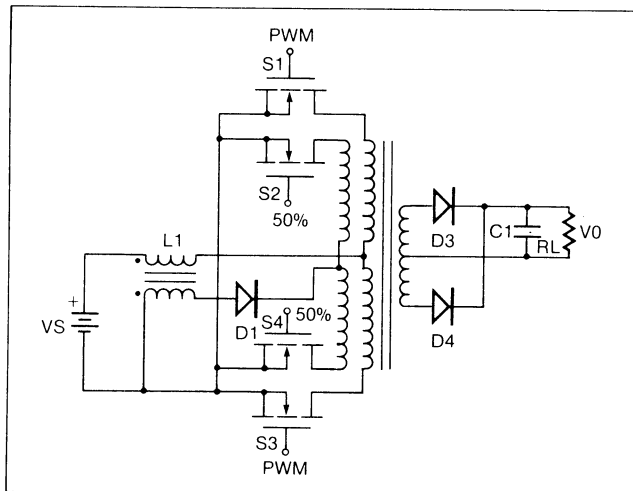


Figure 15

patented(?). The circuit in Figure 15 does provide a means for having all the switches referenced to ground at the expense of complicating the primary of T1. This may be useful in some applications.

The circuit in Figure 16 is a bridge version of the circuit given in Figure 5 which could be useful for off line applications.

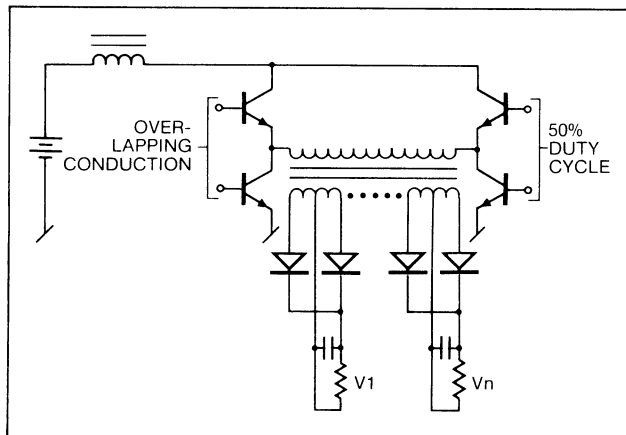


Figure 16

6. SUMMARY

A family of current-fed converter topologies have been presented. This group of circuits provides a means to have the advantages of the early current-fed converters without their disadvantages. A few of the circuits may very well replace some of the topologies presently in use.

7. BIBLIOGRAPHY

1. R. Hayner, T. Phelps and J. Collins, "The Venable Converter: A New Approach to Power Processing," IEEE 1976 Power Electronics Specialists Conference Record, pages 92 to 103.

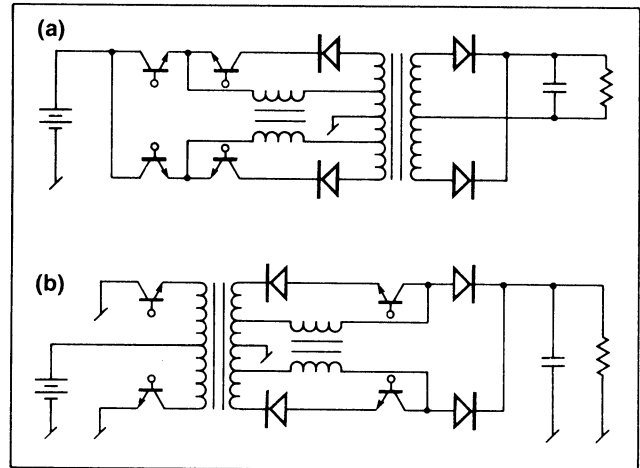


Figure 17

2. A. Rostad, C. McCown and D. Lawrence, "Application of the Venable Converter to a Series of Satellite TWT Power Processors," IEEE 1976 Power Electronics Specialists Conference Record, pages 104-111.
3. B. Farber, D. Goldin and F. Gourash, "A High Power TWT Power Processing System," IEEE Power Electronics Specialists Conference Record, June 1974.
4. B. F. Farber, A. D. Schoenfeld and P. A. Thollot, "Power Processing System for a 200W Communication Satellite Transmitter," International Conference on Satellite Communication Systems Technology, 7-10 April 1975.
5. A. H. Weinberg, "A Boost Regulator with a New Energy Transfer Principle," Proceedings of the Spacecraft Power Conversion Electronics Seminar, September 1974, ESRO Publication SP-103.
6. J. Biess, D. Cronin and W. Dudley, "Power Processing Module for a Military Digital Equipment Power Subsystem," IEEE Power Electronics Specialists Conference Record, June 1976.
7. E. Caulkin and B. Hamilton, "A Conceptually New Approach for Regulated DC-to-DC Converters Employing Transistor Switches and Pulse Width Control," IEEE Industry Applications Society Annual Meeting Record, 1972, pages 485-494.
8. S. Lindena, "The Current-Fed Inverter," 20th Annual Proceedings of the Power Sources Conference, Atlantic City, NJ, May 1966, pages A-23 to A-26.
9. H. Higachi and L. Trubell, "A Regulating Electric Power Circuit Arrangement," U.S. Patent #4,025,863, 24 May 1977.
10. R. Middlebrook and G. Wester, "Low-Frequency Characterization of Switched DC-DC Converters," IEEE Power Electronics Specialists Conference Record, June 1972.